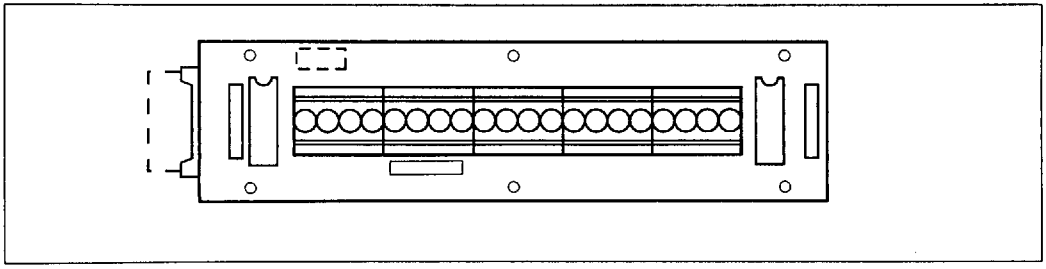
SIEMENS

16 CHARACTER IDA3416-16
20 CHARACTER IDA3416-20
32 CHARACTER IDA3416-32

.225" Red, 17 Segment
DL3416 Intelligent Display® Assembly



FEATURES

- .225" Magnified Monolithic Character
- Wide Viewing Angle ±40°
- Complete Alphanumeric Display Assembly Using the DL3416
  - Built-in Multiplex and LED Drive Circuitry
  - Built-in Memory
  - Built-in Character Generator
- 64 Character ASCII Set
- Direct Access to Each Digit Independently
- Display Blank Function
- Memory Clear Function
- Cursor Function
- 16, 20, or 32 Character Display Length Custom Lengths (Increments of 4 Characters) by Request
- Single 5.0 Volt Power Supply
- TTL Compatible
- Easily Interfaced to a Microprocessor
- Schmitt Trigger Inputs on Data and Write Lines

DESCRIPTION

The IDA3416-16/-20/-32 assembly is an extension of the DL3416 Intelligent Display. This assembly provides the designer with circuitry for display maintenance. It also minimizes interaction and interface normally required between the user's system and a multiplexed alphanumeric display.

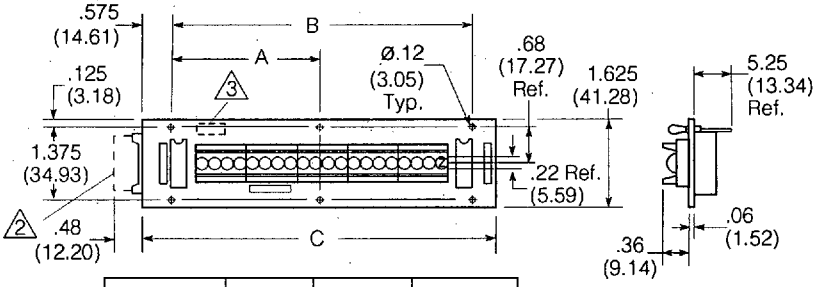
The assembly consists of four/five/eight DL3416s in a single row, together with decoder and interface buffers on a single printed circuit board. Each DL3416 provides its own memory, ASCII ROM character decoder, multiplexing circuitry, and drivers for the four 17-segment LEDs.

Intelligent Display Assemblies can be used for applications such as data terminals, controllers, instruments, and other products which require an alphanumeric display.

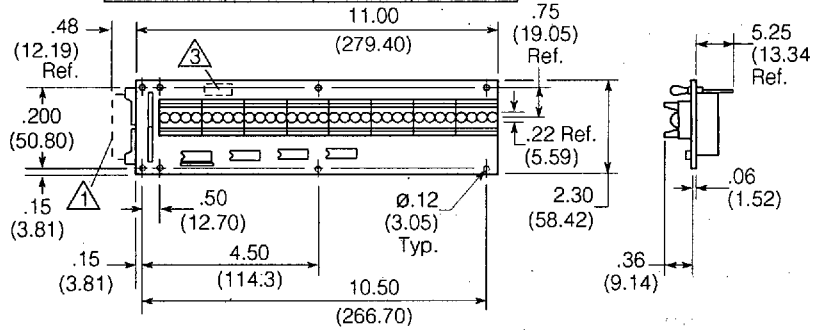
Maximum Ratings

V_{cc}	6.0 V
Voltage, Applied to Any Input	−0.5 to Vcc +0.5 Vdc
Operating Temperature	0°C to +65°C
Storage Temperature	−20°C to +70°C

Package Dimensions in Inches (mm)



Part No.	A	B	C
IDA3416-16	3.00 (76.20)	6.00 (152.40)	6.95 (176.58)
IDA3416-20	3.65 (92.71)	7.30 (185.42)	8.25 (209.55)



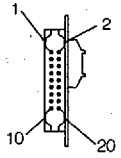
IDA3416-16, -20

Pin	Function
J2-1	D6 Data Line
J2-2	BL Blanking
J2-3	D5 Data Line
J2-4	Unused
J2-5	D4 Data Line
J2-6	A1 Address Line
J2-7	D3 Data Line
J2-8	A0 Address Line
J2-9	D2 Data Line
J2-10	CLR Clear
J2-11	D1 Data Line
J2-12	CE2 Chip Enable
J2-13	D0 Data Line
J2-14	CU Cursor Select
J2-15	WR Write
J2-16	Cue Cursor Enable
J2-17	A3 Address Line
J2-18	Unused
J2-19	A4 Address Line
J2-20	A2 Address Line
J3-1	GND
J3-2	V_{cc}
J3-3	V_{cc}
J3-4	GND

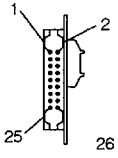
IDA3416-32

Pin	Function
J2-1	A2 Address Line
J2-2	DE4 Display Enable
J2-3	A3 Address Line
J2-4	DE3 Display Enable
J2-5	A4 Address Line
J2-6	DE1 Display Enable
J2-7	No Connection
J2-8	DE2 Display Enable
J2-9	D0 Data Line
J2-10	No Connection
J2-11	D1 Data Line
J2-12	No Connection
J2-13	D2 Data Line
J2-14	No Connection
J2-15	D6 Data Line
J2-16	No Connection
J2-17	D4 Data Line
J2-18	Cue Cursor Enable
J2-19	D5 Data Line
J2-20	CU Cursor Select
J2-21	A0 Address Line
J2-22	CLR Clear
J2-23	A1 Address Line
J2-24	WR Write
J2-25	D3 Data Line
J2-26	BL Blanking
J3-1	GND
J3-2	V_{cc}
J3-3	V_{cc}
J3-4	GND

IDA3416-16, -20



IDA3416-32



Recommended Mating Connector

Connector	Function	Type	Suggested Manufacturer
J2	Control/Data	20 Pin Ribbon	Berg P/N 65496-007
J2	Control/Data	26 Pin Ribbon	Berg P/N 65484-011
J3	Power	Amp	Pin P/N 87026-2 Housing P/N 1-87025-3

OPTOELECTRONIC CHARACTERISTICS at 25°C

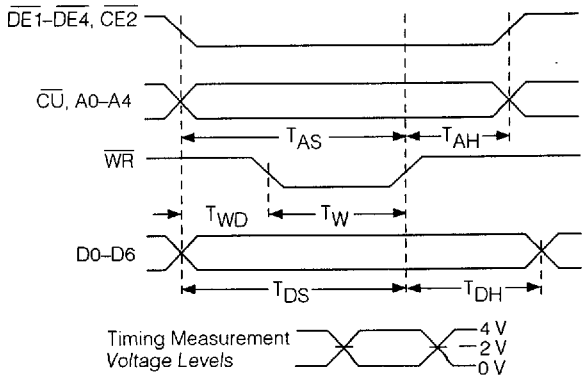
Parameter	Symbol	Min.	Typ.	Max	Units	Conditions
Supply Voltage	V_{CC}	4.75	5.00	5.25	V	
Supply Current/Digit	I_{CC}		25		mA	V_{CC} = 5 V, 8 segments/digit
Supply Current/Digit	I_{CC}			6	mA	V_{CC} = 5 V, display blank VIN = 0 V, $\overline{WR}$ = 5 V
Total–IDA3416-16	I_{CC}			850	mA	V_{CC} = 5 V, all segments/digit[1]
Total–IDA3416-20	I_{CC}			1050	mA	V_{CC} = 5 V, all segments/digit[1]
Total–IDA3416-32	I_{CC}			1680	mA	V_{CC} = 5 V, all segments/digit[1]
Input Voltage–High, all inputs Input Voltage–Low, all inputs	V_{IH} V_{IL}	3.5		 0.8	V V	V_{CC} = 5 V, ±0.25 V V_{CC} = 5 V
Input Current–High, all inputs	I_{IH}			40	µA	V_{CC} = 5.25 V, V_I = 2.4 V
Input Current–Low, all inputs	I_{IL}			6.4	mA	V_{CC} = 5.25 V, V_I = 0.4 V
Luminous Intensity, Average/Digit	I_V		0.8		mcd	V_{CC} = 5 V, 8 segments/digit
Peak Emission Wavelength	λpeak		660		mm	
Viewing Angle			±40		Deg.	Vertical and horizontal from normal to display plane

SWITCHING CHARACTERISTICS @ 5 V

Parameter @ +25°C	Symbol	(min.)	Unit
Write Pulse	T_W	350	nS
Data Set Up Time	T_{DS}	550	nS
Data Hold Time	T_{DH}	75	nS
Address/DE Setup Time	T_{AS}	550	nS
Address/DE Hold Time	T_{AH}	75	nS
Write Set Up Time	T_{WD}	200	nS
Clear Time	T_{CLR}	15	mS

Note: Cursor should not be on longer than 60 seconds.

TIMING CHARACTERISTICS



System Overview

The IDA3416-16/-32, Intelligent Display Assembly, has 16, 20, or 32 alphanumeric characters and operates from just a +5 V supply. Based on the the DL3416, four character Intelligent Display, the IDA3416 adds all the support logic required for direct connection to most microprocessor buses. The system interface takes place through a 20 or 26 pin connector that has data address lines as well as the control signals needed. One additional connector is included on the IDA3416 and is used for power and ground connections.

System Power Requirements

Operating from a single +5 volt power supply, the IDA3416 requires a typical operating current of 30 mA with eight of the segments lit on each character. For the 32 character display, the current increases to 850 mA, typical. For the worst case condition with all segments lit, the current is 52 mA per digit. With the display blanked, the current is 6 mA per digit.

Display Interface

The display interface on the 20 or 26 pin connector consists of seven data lines (D0 to D6), five address lines (A0 to A4), and various control signals. All address, data, control lines have either pull-up or pull-down 1K ohm resistors.

$\overline{BL}$ (Blanking, active low): When this line is pulled low, it causes the entire IDA display to go blank without affecting the contents of the display memory on the DL3416s. $\overline{BL}$ is active regardless of address or display enable lines. A flashing display can be achieved by pulsing this line.

$\overline{WR}$ (Write, active low): To store a character in the display memory, this line must be pulsed low for a minimum write time. See Timing Diagram for timing and relationships to other signals.

CUE (Cursor Enable, active high): When high, this line permits the cursor to be displayed[1], and when brought low, it disables the cursor function without affecting the stored value. CUE is active regardless of address or display enable lines. A flashing cursor can be created by pulsing the CUE line low.

$\overline{CU}$ (Cursor Select, active low): The cursor function (character with all segments lit) is loaded by selecting the digit address and holding $\overline{CU}$ true. A "1" on D0 inserts the cursor. A "0" on D0 removes the cursor. The change occurs during the next write pulse per the Timing Diagram.

$\overline{CLR}$ (Clear, active low): When held low for one display multiplex cycle (see DL 3416 data sheet for more information) of 15 ms, this line will cause all stored characters in the display, except for the cursor, to be cleared. $\overline{CLR}$ is active regardless of address or display enable lines.

CE2 (Chip Enable, active low): To store character in the display memory, this line must be held low at least 550 nS preceding the leading edge of the $\overline{WR}$ pulse.

Address lines A0 to A4 are set up so that the rightmost character is the lowest address. The left-most character is the highest address. Data lines are set up so that D0 is the least significant bit and D6 is the most significant bit.

Using the Display Interface

Through the use of memory-mapped 1/0 techniques, the IDA can be treated almost like a memory location—supply the data, address and proper control signals and the characters appear, with each character location independently addressable. The basic signal flow sequence to load a character would start with the address lines going to the desired address while the $\overline{CLR}$ and $\overline{BL}$ lines are high to permit the data to be loaded in and displayed. After the address has stabilized, the data can change to the desired values (including the cursor). After the data has stabilized, the $\overline{WR}$ pulse is started and must remain low for at least 350 ns. Signals must be held stable for 75 ns, minimum, after the rising edge of the $\overline{WR}$ pulse to ensure correct loading, while the addresses must be stable for 650 ns preceding the same rising edge of the $\overline{WR}$ pulse. See the Timing Diagram.

Notes:

1. CMOS handling precaution, see Appnote 18.
2. Cleaning agents–NO alcohol.