Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS ECL STATIC RAM 4K (1K x 4-BIT) SRAM

PRELIMINARY
IDT10474, IDT10A474
IDT100474, IDT100A474
IDT101474, IDT101A474

FEATURES:

- 1024-words x 4-bit organization
- Address access time: 2.7/3/3.5/4/4.5/5/7/8/10/15 ns
- Low power dissipation: 1000mW (typ.)
- Guaranteed Output Hold time
- Fully compatible with ECL logic levels
- Separate data input and output
- Corner and Center power pin pinouts
- Standard through-hole and surface mount packages
- Guaranteed-performance die available for MCMs/hybrids
- MIL-STD-883, Class B product available

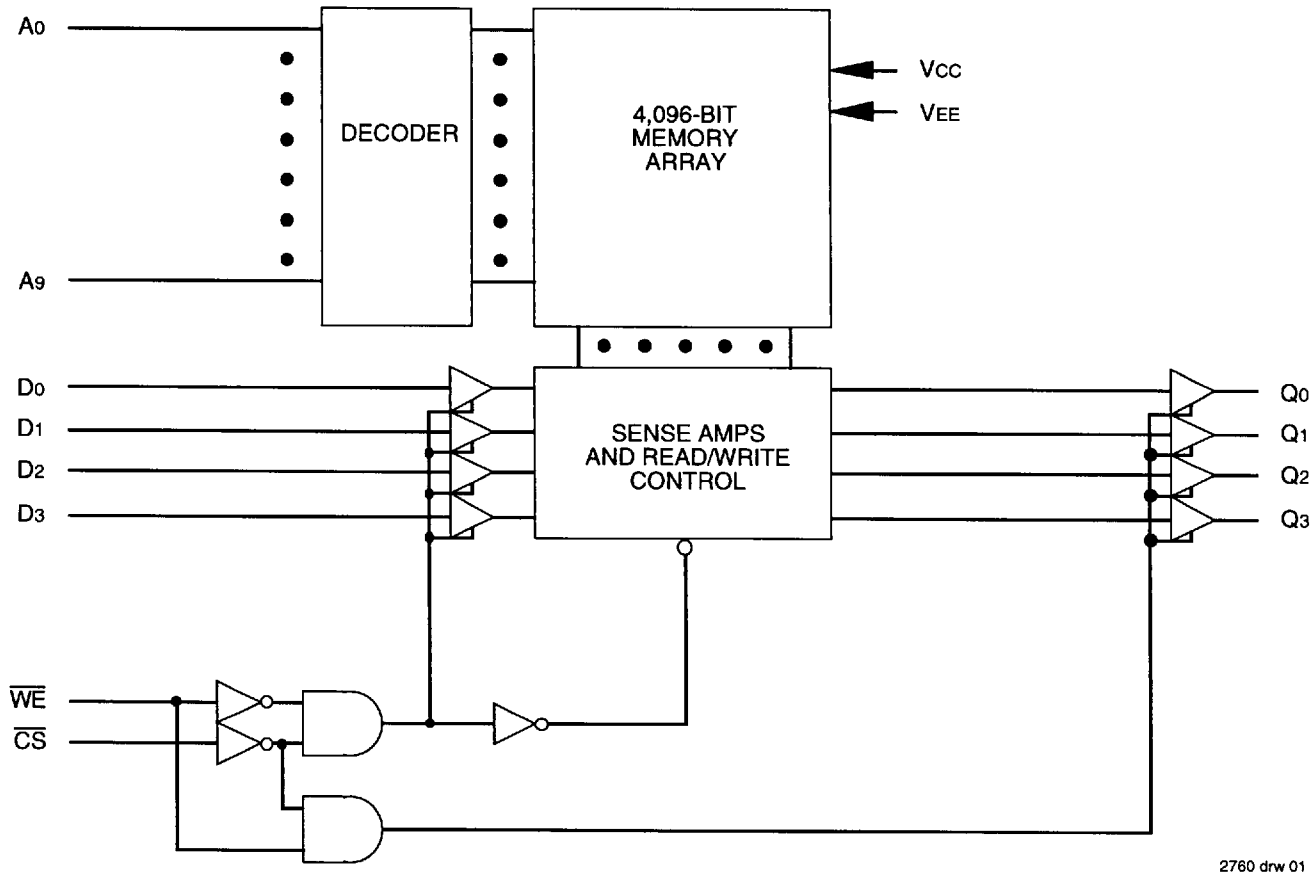
DESCRIPTION:

The IDT10474(10A474), IDT100474(100A474) and IDT101474(101A474) are 4,096-bit high-speed BiCMOS ECL static random access memories organized as 1Kx4, with separate data inputs and outputs. All I/Os are fully compatible with ECL levels.

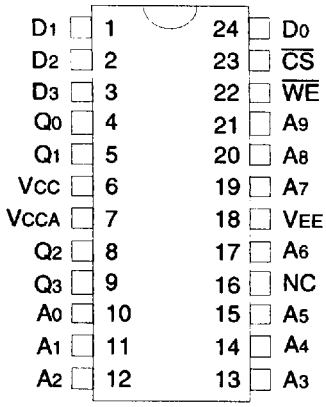
These devices are part of a family of asynchronous four-bit-wide ECL SRAMs. This device is available in both the traditional corner-power pinout, and "revolutionary" center-power pin configurations. Because they are manufactured in BiCMOS technology, power dissipation is greatly reduced over equivalent bipolar devices. Low power operation provides higher system reliability and makes possible the use of the plastic SOJ package for high-density surface mount assembly.

The fast access time and guaranteed Output Hold time allow greater margin for system timing variation. DataIN setup time specified with respect to the trailing edge of Write Pulse eases write timing allowing balanced Read and Write cycle times.

FUNCTIONAL BLOCK DIAGRAM

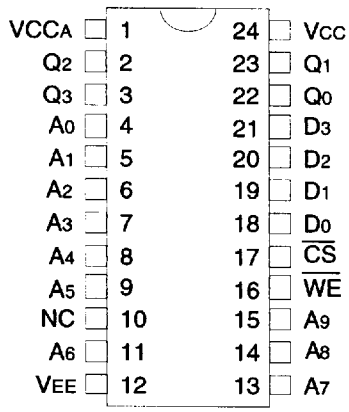


PIN CONFIGURATIONS



Center Power
"A"
Top View

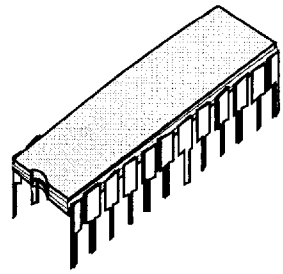
2760 drw 02a



Corner Power
"Non-A"
Top View

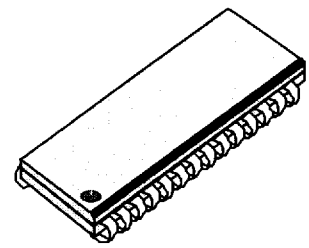
2760 drw 02b

PACKAGES



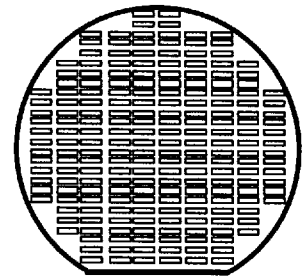
400-Mil-Wide
CERDIP PACKAGE
D24-3

2760 drw 03



300-Mil-Wide
PLASTIC SOJ PACKAGE
SO24-4

2760 drw 04



Hi-Rel Die
For Hybrid and MCM
Applications

2760 drw 05

PIN DESCRIPTIONS

Symbol	Pin Name
A0 through A9	Address Inputs
D0 through D3	Data Inputs
Q0 through Q3	Data Outputs
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input (Internal pull down)
VEE	More Negative Supply Voltage
VCC	Less Negative Supply Voltage

2760 tbl 01

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	DIP Typ.	DIP Max.	SOJ Typ.	SOJ Max.	Unit
CIN	Input Capacitance	4	—	3	—	pF
COUT	Output Capacitance	6	—	3	—	pF

2760 tbl 02

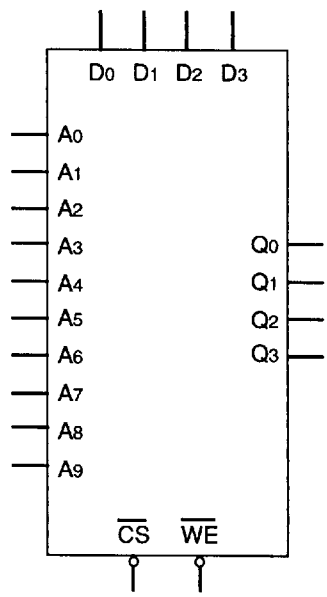
TRUTH TABLE(1)

$\overline{CS}$	$\overline{WE}$	DataOUT	Function
H	X	L	Deselected
L	H	RAM Data	Read
L	L	L	Write

NOTE:
1. H = HIGH, L = LOW, X = Don't Care

2760 tbl 03

LOGIC SYMBOL



2760 drw 06

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating		Value	Unit
VTERM	Terminal Voltage With Respect to GND		+0.5 to –7.0	V
TA	Operating Temperature	10K 100K 101K	0 to +75 0 to +85 0 to +75	°C
TBIAS	Temperature Under Bias		–55 to +125	°C
TSTG	Storage Temperatuure	Ceramic Plastic	–65 to +150 –55 to +125	°C
PT	Power Dissipation		1.5	W
IOUT	DC Output Current (Output High)		–50	mA

NOTE:

2760 tbl 04

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

AC/DC ELECTRICAL OPERATING RANGES

I/O	VEE	TA
10K	–5.2V ± 5%	0 to +75°C, air flow exceeding 2 m/sec
100K	–4.5V ± 5%	0 to +85°C, air flow exceeding 2 m/sec
101K	–4.75V to –5.46V	0 to +75°C, air flow exceeding 2 m/sec

2760 tbl 05

DC ELECTRICAL CHARACTERISTICS (1)

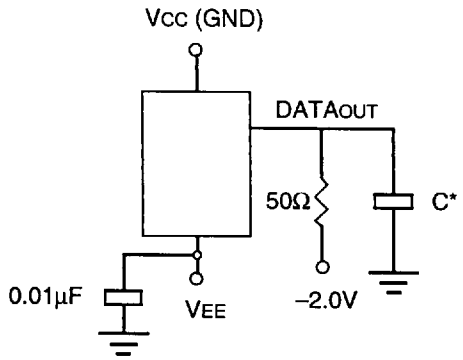
Symbol	Parameter		10K Min.	10K Max.	10K TA	100K/101K Min.	100K/101K Max.	Unit
VOH	Output HIGH Voltage (VIN= VIH(Max) or VIL(Min))		–1000 –960 –900	–840 –810 –720	0°C 25°C 75°C	–1025	–880	mV
VOL	Output LOW Voltage (VIN= VIH(Max) or VIL(Min))		–1870 –1850 –1830	–1665 –1650 –1625	0°C 25°C 75°C	–1810	–1620	mV
VOHC	Output Threshold HIGH Voltage (VIN= VIH(Min) or VIL(Max))		–1020 –980 –920	— — —	0°C 25°C 75°C	–1035	—	mV
VOLC	Output Threshold LOW Voltage (VIN= VIH(Min) or VIL(Max))		— — —	–1645 –1630 –1605	0°C 25°C 75°C	—	–1610	mV
VIH	Input HIGH Voltage (Guaranteed Input Voltage High for All Inputs)		–1145 –1105 –1045	–840 –810 –720	0°C 25°C 75°C	–1165	–880	mV
VIL	Input LOW Voltage (Guaranteed Input Voltage Low for All Inputs)		–1870 –1850 –1830	–1490 –1475 –1450	0°C 25°C 75°C	–1810	–1475	mV
IIH	Input HIGH Current							
	VIN= VIH(Max)	CS	—	220	—	—	220	µA
		Others	—	110	—	—	110	µA
IIL	Input LOW Current							
	VIN= VIL(Min)	CS	0.5	170	—	0.5	170	µA
		Others	–50	90	—	–50	90	µA
IEE	Supply Current		–210	—	—	–190 (100K) –210 (101K)	— —	mA

NOTE:

1. RL = 50Ω to -2V, air flow exceeding 2 m/sec.

2760 tbl 05

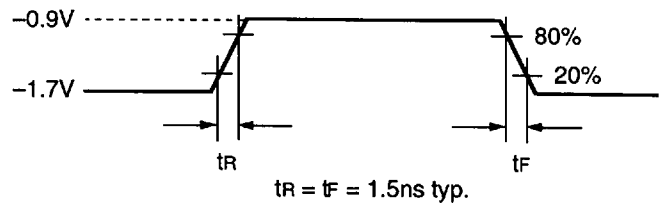
AC TEST LOAD CONDITION



*Includes probe and jig capacitance.
C < 5pF (2.7,3.0, 3.5nS speed grades)
C < 30pF (all other speed grades)

2760 drw 07

AC TEST INPUT PULSE



tR = tF = 1.5ns typ.

Note: All timing measurements are referenced to 50% input levels.

2760 drw 08

RISE/FALL TIME

Symbol	Parameter	Min.	Typ.	Max.	Unit
tR	Output Rise Time	—	1.5	—	ns
tF	Output Fall Time	—	1.5	—	ns

2760 tbl 06

FUNCTIONAL DESCRIPTION

The IDT10474(10A474), IDT100474(100A474), and IDT101474(101A474) BiCEMOS ECL static RAMs provide high speed with low power dissipation typical of BiCMOS ECL. These devices are available in both the traditional corner-power pinout and the "revolutionary" center-power pinout for reduced noise and improved system performance.

READ TIMING

The read timing on these asynchronous devices is straightforward. DataOUT is held LOW until the device is selected by Chip Select (CS). The Address (ADDR) settles and data appears on the output after time tAA. Note that DataOUT is held for a short time (tOH) after the address begins to change for the next access, then ambiguous data is on the bus until a new time tAA.

WRITE TIMING

To write data to the device, a Write Pulse need be formed on the Write Enable input (WE) to control the write to the SRAM array. While CS and ADDR must be set-up when WE goes low, DataIN can settle after the falling edge of WE, giving the data path extra margin. Data is written to the memory cell at the end of the Write Pulse, and addresses and Chip Select must be held after the rising edge of the Write Pulse to ensure satisfactory completion of the cycle.

DataOUT is disabled (held LOW) during the Write Cycle. If CS is held LOW (active) and addresses remain unchanged, the Data OUT pins will output the written data after "Write Recovery time" (tWR).

Because of the very short Write Pulse requirement, these devices can be cycled as quickly for Writes as for Reads.

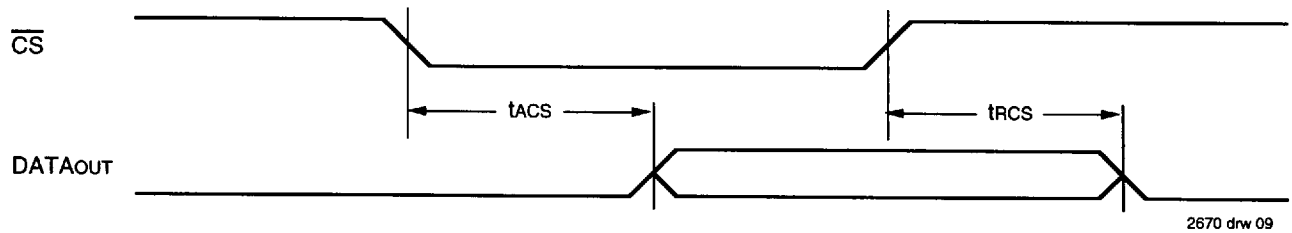
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	S2.7		S3		S3.5		S4		S4.5		S5		S7,8,10,15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle																
tACS	Chip Select Access Time	—	2.0	—	2.0	—	2.5	—	2.5	—	2.5	—	3.0	—	3.5	ns
tRCS	Chip Select Recovery Time	—	2.0	—	2.0	—	2.5	—	2.5	—	2.5	—	3.0	—	3.5	ns
tAA	Address Access Time	—	2.7	—	3.0	—	3.5	—	4.0	—	4.5	—	5.0	—	7.0	ns
tOH	Data Hold from Address Change	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	ns

NOTE:
2760 tbl 07

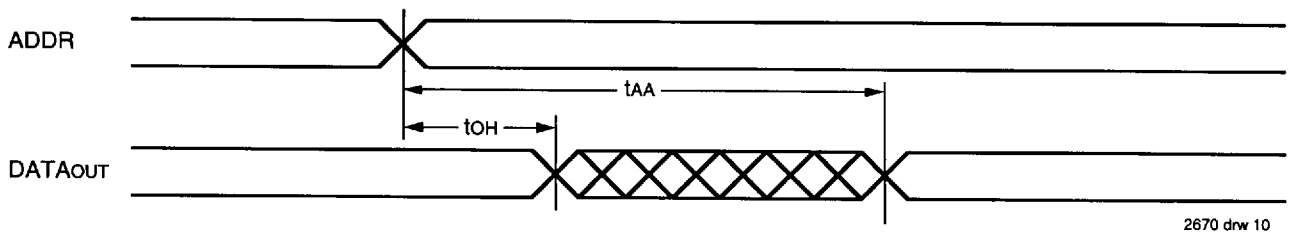
1. Input and Output reference level is 50% point of waveform.
2. Output load capacitance, C < 5pF (2.7, 3.0, 3.5ns speed grades only), see "AC Test Load Condition" on previous page.

READ CYCLE GATED BY CHIP SELECT (1, 2)



2670 drw 09

READ CYCLE GATED BY ADDRESS (1, 3)



2670 drw 10

NOTE:
1. WE is HIGH for read cycle.
2. Address valid prior to or minimum tAA-tACS before CS active.
3. CS active prior to or minimum tAA-tACS after address valid.

AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

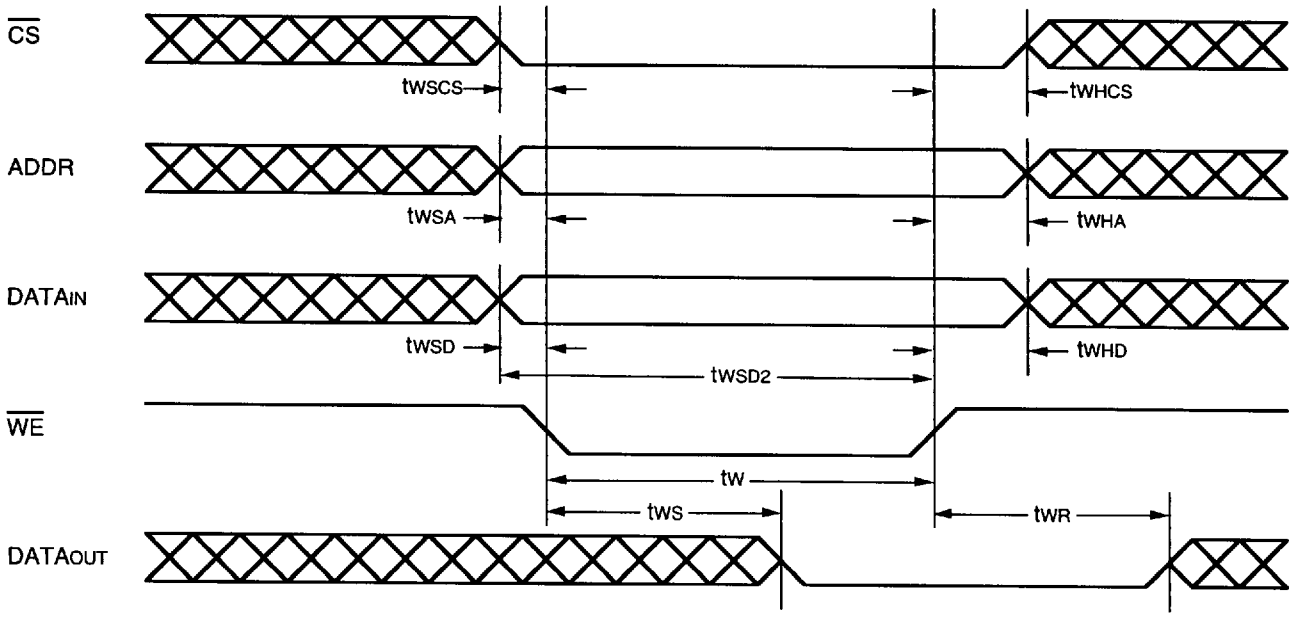
Symbol	Parameter[1]	S2.7		S3.0		S3.5		S4		S4.5		S5		S7,8,10,15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle																
tW	Write Pulse Width (tWSA = minimum)	2.5	—	2.5	—	3.0	—	3.0	—	3.5	—	4.0	—	6.0	—	ns
tWSD	Data Set-up Time	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
tWSD2[2]	Data Set-up Time to WE HIGH	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	3.0	—	5.0	—	ns
tWSA	Address Set-up Time (tW = minimum)	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
tWSCS	Chip Select Set-up Time	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
tWHD	Data Hold Time	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	ns
tWHA	Address Hold Time	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	ns
tWHCS	Chip Select Hold Time	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	ns
tWS	Write Disable Time	—	2.7	—	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	5.0	ns
tWR[3]	Write Recovery Time	—	2.7	—	3.0	—	3.0	—	3.0	—	3.0	—	3.0	—	5.0	ns

NOTE:

2760 tbl 08

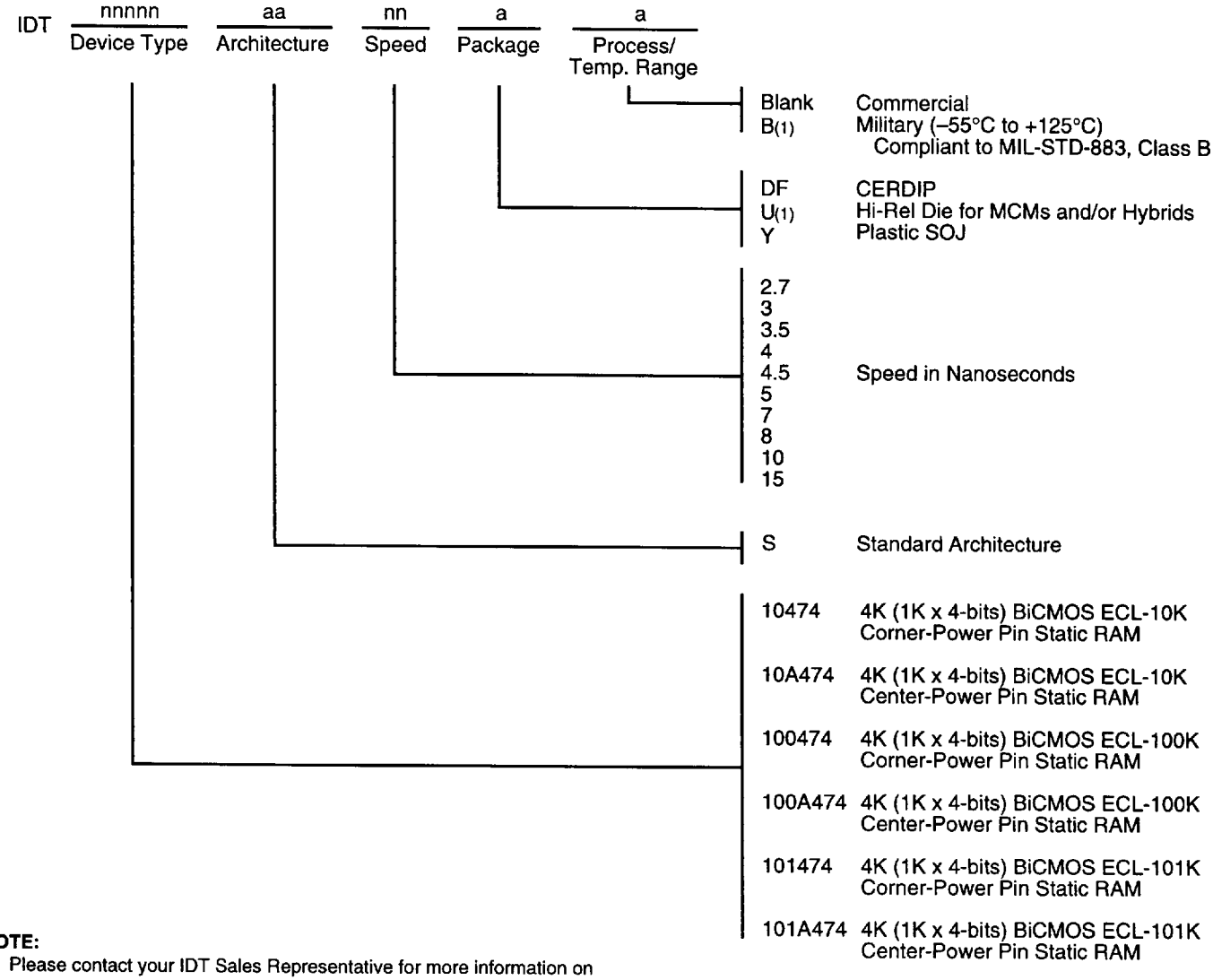
1. Input and Output reference level is 50% point of waveform.
2. tWSD is specified with respect to the falling edge of WE for compatibility with bipolar part specifications, but this device actually only requires tWSD2 with respect to rising edge of WE.
3. tWR is defined as the time to reflect the newly written data on the Data Outputs (Q0 to Q3) when no new Address Transition occurs.

WRITE CYCLE TIMING DIAGRAM



2670 drw 11

ORDERING INFORMATION



NOTE:
1. Please contact your IDT Sales Representative for more information on specifications and availability of Military and Die products.

2760 drw 12

Integrated Device Technology, Inc.

2975 Stender Way, Santa Clara, CA 95054-3090 Telephone: (408) 727-6116 FAX 408-492-8674

PACKAGE DIAGRAM OUTLINES

CERDIP (Continued)

REV	DCN	DESCRIPTION	DATE	APPROVED
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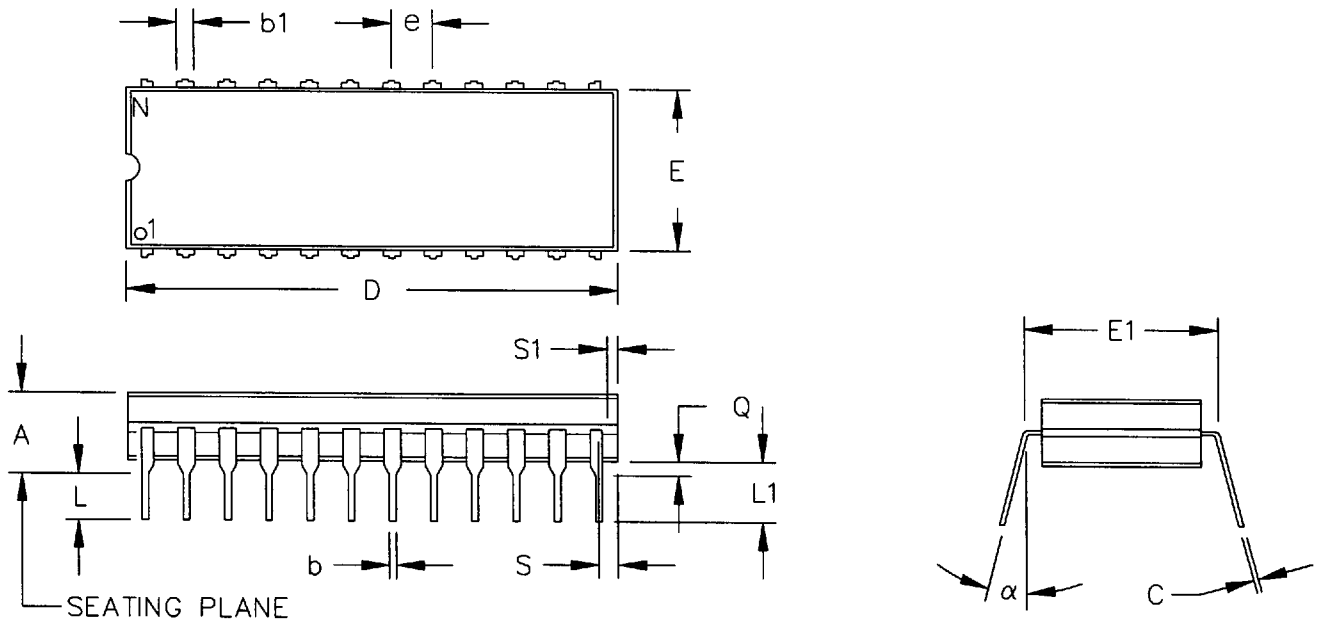


NOTES: (UNLESS OTHERWISE SPECIFIED)
1. ALL DIMENSIONS ARE IN INCHES.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "N" REPRESENTS THE NUMBER OF LEADS.

DWG #	D24-3	
SYMBOL	MIN	MAX
A	.130	.175
b	.015	.021
b1	.045	.065
C	.009	.014
D	1.180	1.250
E	.350	.410
E1	.380	.420
e	.100 BSC	
L	.125	.175
L1	.150	–
Q	.015	.060
S	.030	.070
S1	.005	–
α	0°	15°
N	24	

CONFIGURATION	EXCEPTIONS
MIL-M-38510	D-11	NONE
JEDEC	NOT REGISTERED	

TOLERANCES UNLESS OTHERWISE SPECIFIED
FRAC ± – DEC ± – ANGLES ± –

APPROVALS	DATE
DRAWN AA	04/91
CHECKED	

Integrated Device Technology, Inc.
3236 Scott Blvd., Santa Clara, CA 95051
(408) 727-6116 FAX: (408) 727-2328

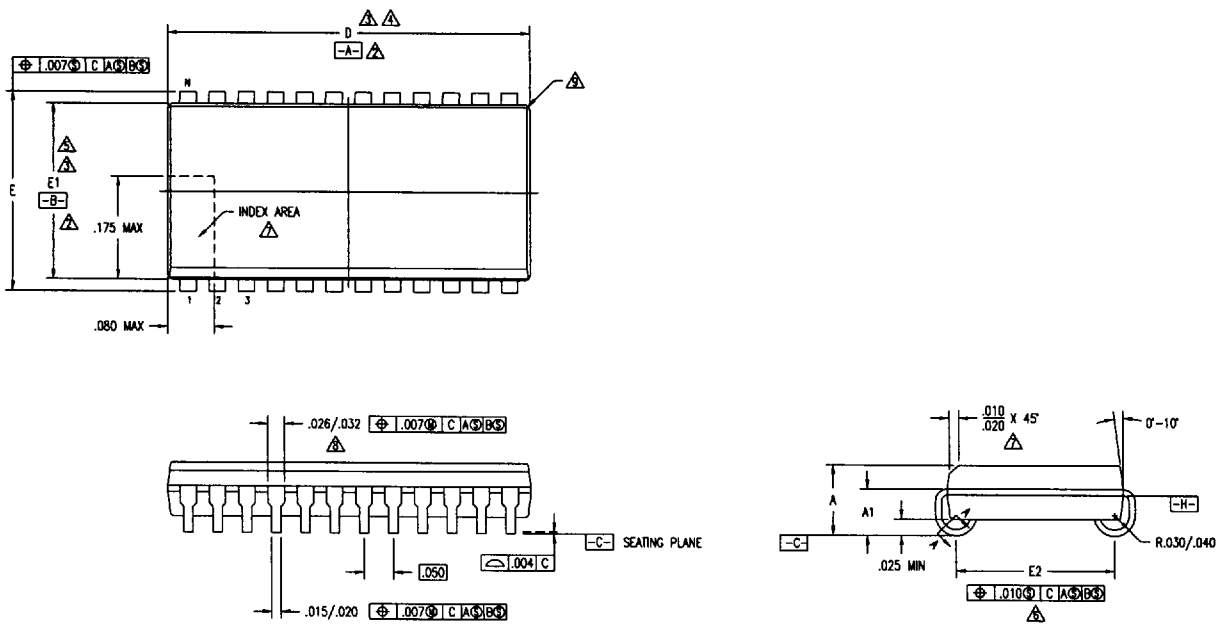
24 LD CERDIP MKT DWG (400 MIL)

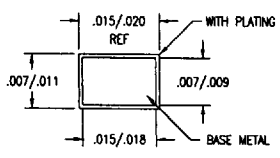
SCALE	SIZE	DRAWING NO.	REV
N/A	A	PSC-2095	00

DO NOT SCALE DRAWING | SHEET 68

SOJ (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27656	00	MOVE FROM PSC-4024 REDRAW TO JEDEC FORMAT	03/15/95	





SECTION A-A

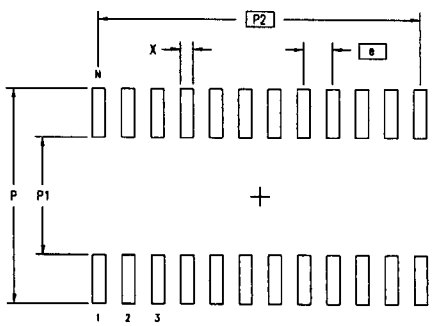
TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070
DECIMAL ANGULAR XX± ± XXX± XXXX±		
APPROVALS	DATE	TITLE PJ 24 PACKAGE OUTLINE .300" BODY WIDTH SOJ .050" PITCH
DRAWN JPJ	03/15/95	
CHECKED		SIZE C · DRAWING No. PSC-4048 · REV 00
		DO NOT SCALE DRAWING

SOJ (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27656	00	MOVE FROM PSC-4024 REDRAW TO JEDEC FORMAT	03/15/95	

DWG #		SO24-4		
SYMBOL	JEDEC VARIATION AA			NOTE
	MIN	NOM	MAX	
A	.130	.139	.148	
A1	.082	.088	.095	
D	.620	.625	.630	3,4
E	.335	.340	.345	
E1	.295	.300	.305	3,5
E2	.260	.270	.280	6
N	24			

LAND PATTERN DIMENSIONS



	MIN	MAX
P	.362	.370
P1	.196	.204
P2	.550 BSC	
X	.018	.026
e	.050 BSC	
N	24	

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE -H-
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 PER SIDE
5. DIMENSION E1 DO NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006 PER SIDE
6. DIMENSION E2 TO BE DETERMINED AT SEATING PLANE -C- CONTACT POINT
7. THE CHAMFER ON THE PACKAGE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE ZONE INDICATED
8. LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .005 IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION
9. EXACT SHAPE OF EACH CORNER IS OPTIONAL
10. ALL DIMENSIONS ARE IN INCHES
11. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-065, VARIATION AA

TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc.
DECIMAL	ANGULAR	2975 Stender Way, Santa Clara, CA 95054
XX±	±	PHONE: (408) 727-6116
XXX±		FAX: (408) 492-8674 TWX: 910-338-2070
XXXX±		

APPROVALS	DATE	TITLE	PJ 24 PACKAGE OUTLINE .300" BODY WIDTH SOJ .050" PITCH	
DRAWN SJV	03/15/95			
CHECKED		SIZE	DRAWING No.	REV
		C	PSC-4048	00
		DO NOT SCALE DRAWING		