Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS ECL STATIC RAM 16K (4K x 4-BIT) SRAM

PRELIMINARY
IDT10484, IDT10A484
IDT100484, IDT100A484
IDT101484, IDT101A484

FEATURES:

- 4096-words x 4-bit organization
- Address access time: 4/4.5/5/7/8/10/15 ns
- Low power dissipation: 900mW (typ.)
- Guaranteed Output Hold time
- Fully compatible with ECL logic levels
- Separate data input and output
- Corner and Center power pin pinouts
- Standard through-hole and surface mount packages
- Guaranteed-performance die available for MCMs/hybrids
- MIL-STD-883, Class B product available

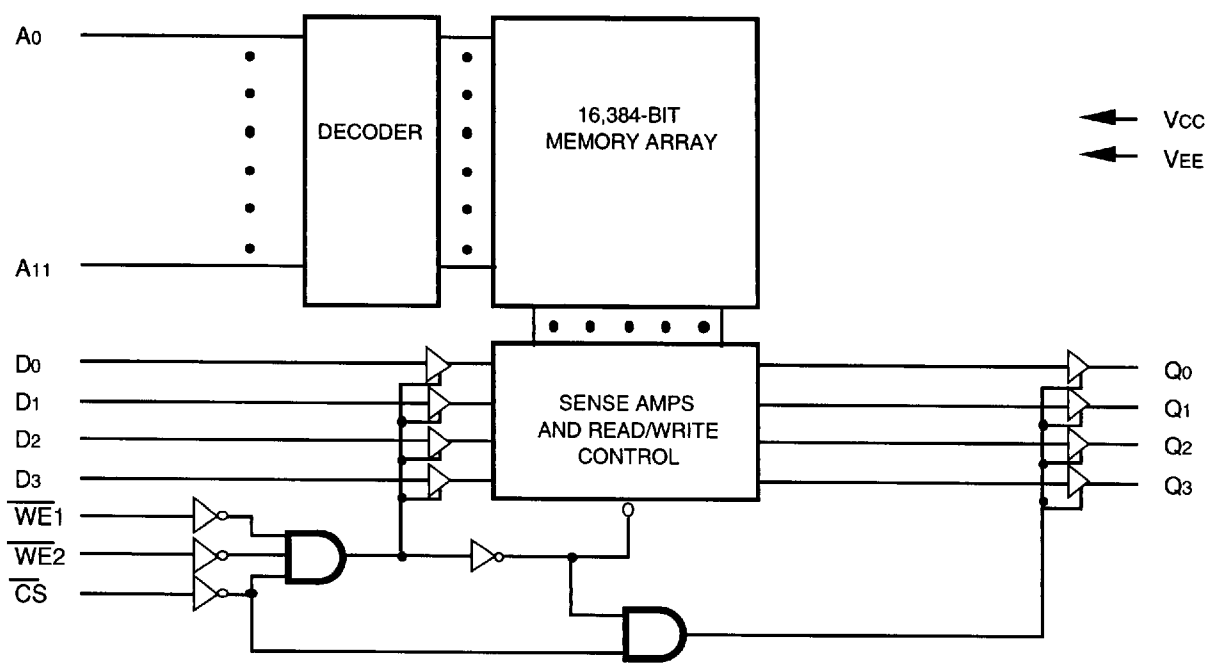
DESCRIPTION:

The IDT10484(10A484), IDT100484(100A484) and IDT101484(101A484) are 16,384-bit high-speed BiCEMOS™ ECL static random access memories organized as 4Kx4, with separate data inputs and outputs. All I/Os are fully compatible with ECL levels.

These devices are part of a family of asynchronous four-bit-wide ECL SRAMs. This device is available in both the traditional corner-power pinout, and "revolutionary" center-power pin configurations. Because they are manufactured in BiCEMOS™ technology, power dissipation is greatly reduced over equivalent bipolar devices. Low power operation provides higher system reliability and makes possible the use of the plastic SOJ package for high-density surface mount assembly.

The fast access time and guaranteed Output Hold time allow greater margin for system timing variation. DataIN setup time specified with respect to the trailing edge of Write Pulse eases write timing allowing balanced Read and Write cycle times.

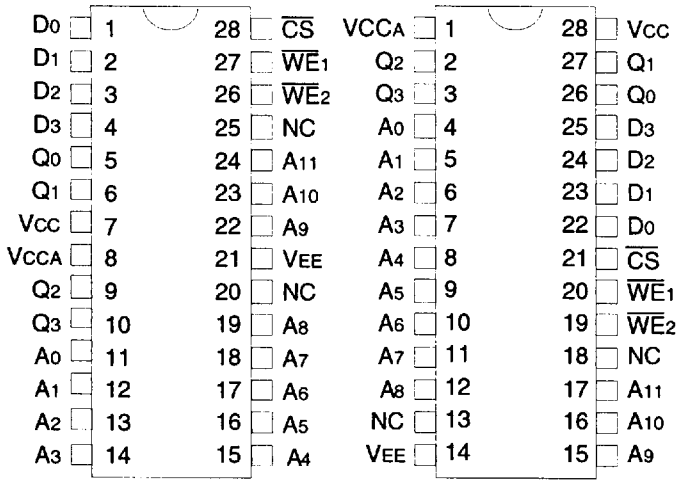
FUNCTIONAL BLOCK DIAGRAM



2811 drw 01

BiCEMOS is a trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



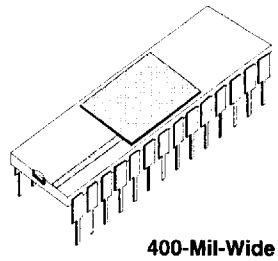
CENTER POWER "A" TOP VIEW

2811 drw 02a

CORNER POWER "NON-A" TOP VIEW

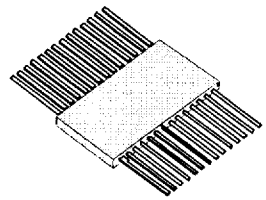
2811 drw 02b

PACKAGES



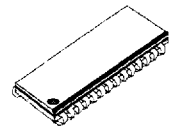
400-Mil-Wide CERAMIC PACKAGE C28-2

2811 drw 03



400-Mil-Wide CERPACK E28-2

2811 drw 04a



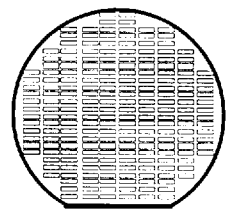
300-Mil-Wide PLASTIC SOJ PACKAGE S028-5

2811 drw 04b

PIN DESCRIPTIONS

Symbol	Pin Name
A0 through A11	Address Inputs
D0 through D3	Data Inputs
Q0 through Q3	Data Outputs
$\overline{WE1}$, $\overline{WE2}$	Write Enable Inputs
$\overline{CS}$	Chip Select Input (Internal pull down)
VEE	More Negative Supply Voltage
VCC	Less Negative Supply Voltage

2811 tbl 01



Characterized Die For Hybrid and MCM Applications

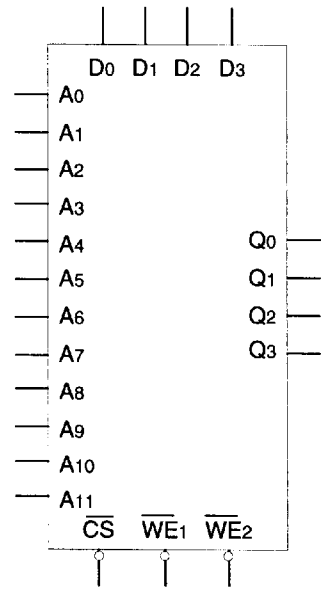
2760 drw 05

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	DIP Typ.	DIP Max.	SOJ Typ.	SOJ Max.	Unit
CIN	Input Capacitance	4	—	3	—	pF
COUT	Output Capacitance	6	—	3	—	pF

2811 tbl 02

LOGIC SYMBOL



2811 drw 06

TRUTH TABLE(1)

CS	WE1, WE2	DataOUT	Function
H	X	L	Deselected
L	*H(2)	RAM Data	Read
L	*L(3)	L	Write

2811 tbl 03

NOTES:
1. H=High, L=Low, X=Don't Care
2. *H = Either WE1 or WE2 are high.
3. *L = Both WE1 and WE2 are low.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating		Value	Unit
VTERM	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
TA	Operating Temperature	10K 100K 101K	0 to +75 0 to +85 0 to +75	°C
TBIAS	Temperature Under Bias		-55 to +125	°C
TSTG	Storage Temperatuure	Ceramic Plastic	-65 to +150 -55 to +125	°C
PT	Power Dissipation		1.5	W
IOUT	DC Output Current (Output High)		-50	mA

NOTE:

2760 tbl 04

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

AC/DC ELECTRICAL OPERATING RANGES

I/O	VEE	TA
10K	-5.2V ± 5%	0 to +75°C, air flow exceeding 2 m/sec
100K	-4.5V ± 5%	0 to +85°C, air flow exceeding 2 m/sec
101K	-4.75V to -5.46V	0 to +75°C, air flow exceeding 2 m/sec

2760 tbl 05

DC ELECTRICAL CHARACTERISTICS (1)

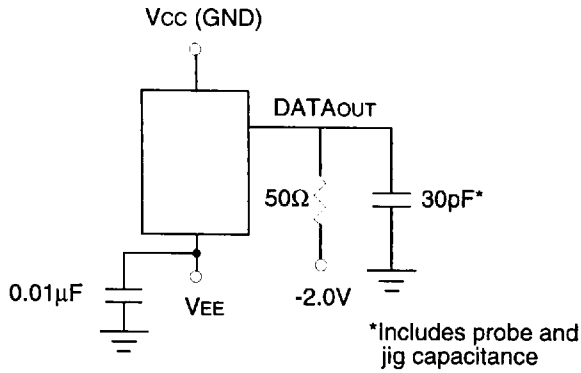
Symbol	Parameter		10K Min.	10K Max.	10K TA	100K/101K Min.	100K/101K Max.	Unit
VOH	Output HIGH Voltage (VIN= VIH(Max) or VIL(Min))		-1000 -960 -900	-840 -810 -720	0°C 25°C 75°C	-1025	-880	mV
VOL	Output LOW Voltage (VIN= VIH(Max) or VIL(Min))		-1870 -1850 -1830	-1665 -1650 -1625	0°C 25°C 75°C	-1810	-1620	mV
VOHC	Output Threshold HIGH Voltage (VIN= VIH(Min) or VIL(Max))		-1020 -980 -920	— — —	0°C 25°C 75°C	-1035	—	mV
VOLC	Output Threshold LOW Voltage (VIN= VIH(Min) or VIL(Max))		— — —	-1645 -1630 -1605	0°C 25°C 75°C	—	-1610	mV
VIH	Input HIGH Voltage (Guaranteed Input Voltage High for All Inputs)		-1145 -1105 -1045	-840 -810 -720	0°C 25°C 75°C	-1165	-880	mV
VIL	Input LOW Voltage (Guaranteed Input Voltage Low for All Inputs)		-1870 -1850 -1830	-1490 -1475 -1450	0°C 25°C 75°C	-1810	-1475	mV
IIH	Input HIGH Current							
	VIN= VIH(Max)	CS Others	— —	220 110	— —	— —	220 110	µA µA
IIL	Input LOW Current							
	VIN= VIL(Min)	CS Others	0.5 -50	170 90	— —	0.5 50	170 90	µA µA
IEE	Supply Current		-210	—	—	-190 (100K) -210 (101K)	— —	mA

NOTE:

1. RL = 50Ω to -2V, air flow exceeding 2 m/sec.

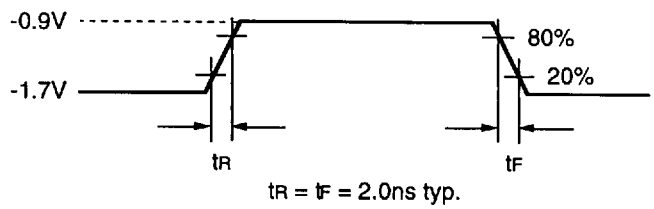
2760 tbl 05

AC TEST LOAD CONDITION



2811 drw 07

AC TEST INPUT PULSE



Note: All timing measurements are referenced to 50% input levels.

2811 drw 08

RISE/FALL TIME

Symbol	Parameter	Min.	Typ.	Max.	Unit
tR	Output Rise Time	—	2	—	ns
tF	Output Fall Time	—	2	—	ns

2811 tbl 06

FUNCTIONAL DESCRIPTION

The IDT10484(10A484), IDT100484(100A484), and IDT101484(101A484) BiCEMOS ECL static RAMs provide high speed with low power dissipation typical of BiCMOS ECL. These devices are available in both the traditional corner-power pinout and the "revolutionary" center-power pinout for reduced noise and improved system performance.

READ TIMING

The read timing on these asynchronous devices is straightforward. DataOUT is held low until the device is selected by Chip Select ($\overline{CS}$). The Address (ADDR) settles and data appears on the output after time t_{AA}. Note that DataOUT is held for a short time (t_{OH}) after the address begins to change for the next access, then ambiguous data is on the bus until a new time t_{AA}.

WRITE TIMING

To write data to the device, a Write Pulse need be formed on the Write Enable input ($\overline{WE}$) to control the write to the SRAM array. This Write Pulse, called $\overline{WE}$, is formed as the logical AND of the $\overline{WE}1$ and $\overline{WE}2$ inputs; that is, when $\overline{WE}1$ and $\overline{WE}2$ both are driven low, $\overline{WE}$ goes low and the write cycle begins.

While $\overline{CS}$ and ADDR must be set-up when $\overline{WE}$ goes low, DataIN can settle after the falling edge of $\overline{WE}$, giving the data path extra margin. Data is written to the memory cell at the end of the Write Pulse, and addresses and Chip Select must be held after the rising edge of the Write Pulse to ensure satisfactory completion of the cycle.

DataOUT is disabled (held low) during the Write Cycle. If $\overline{CS}$ is held low (active) and addresses remain unchanged, the Data OUT pins will output the written data after "Write Recovery time" (t_{WR}).

Because of the very short Write Pulse requirement, these devices can be cycled as quickly for Writes as for Reads.

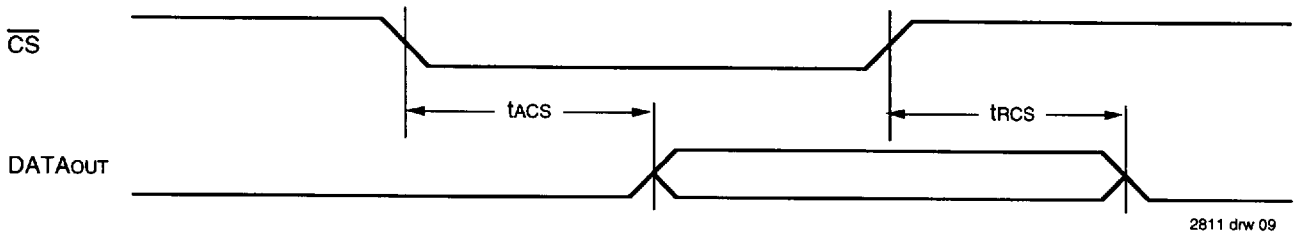
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	S4		S4.5		S5		S7		S8		S10		S15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle																
tACS	Chip Select Access Time	—	2.5	—	2.5	—	3.0	—	3.5	—	5.0	—	5.0	—	5.0	ns
tRCS	Chip Select Recovery Time	—	2.5	—	2.5	—	3.0	—	3.5	—	5.0	—	5.0	—	5.0	ns
tAA	Address Access Time	—	4.0	—	4.5	—	5.0	—	7.0	—	8.0	—	10.0	—	15.0	ns
tOH	Data Hold from Address Change	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	ns

NOTE:
1. Input and Output reference level is 50% point of waveform.

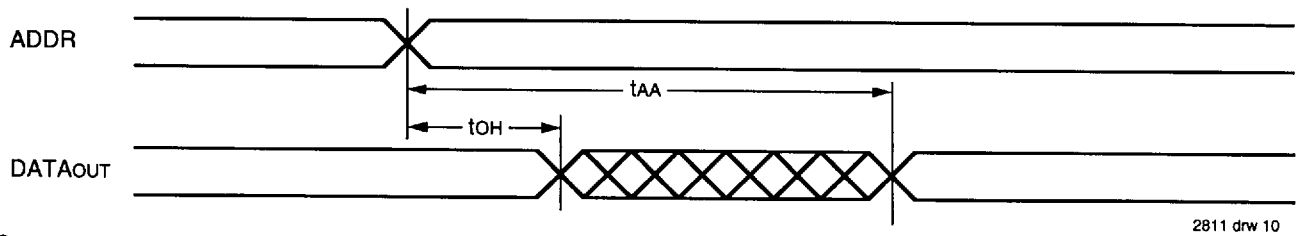
2811 tbl 07

READ CYCLE GATED BY CHIP SELECT (1, 2)



2811 drw 09

READ CYCLE GATED BY ADDRESS (1, 3)



2811 drw 10

NOTES:
1. WE is high for read cycle.
2. Address valid prior to or minimum tAA-tACS before CS active.
3. CS active prior to or minimum tAA-tACS after address valid.

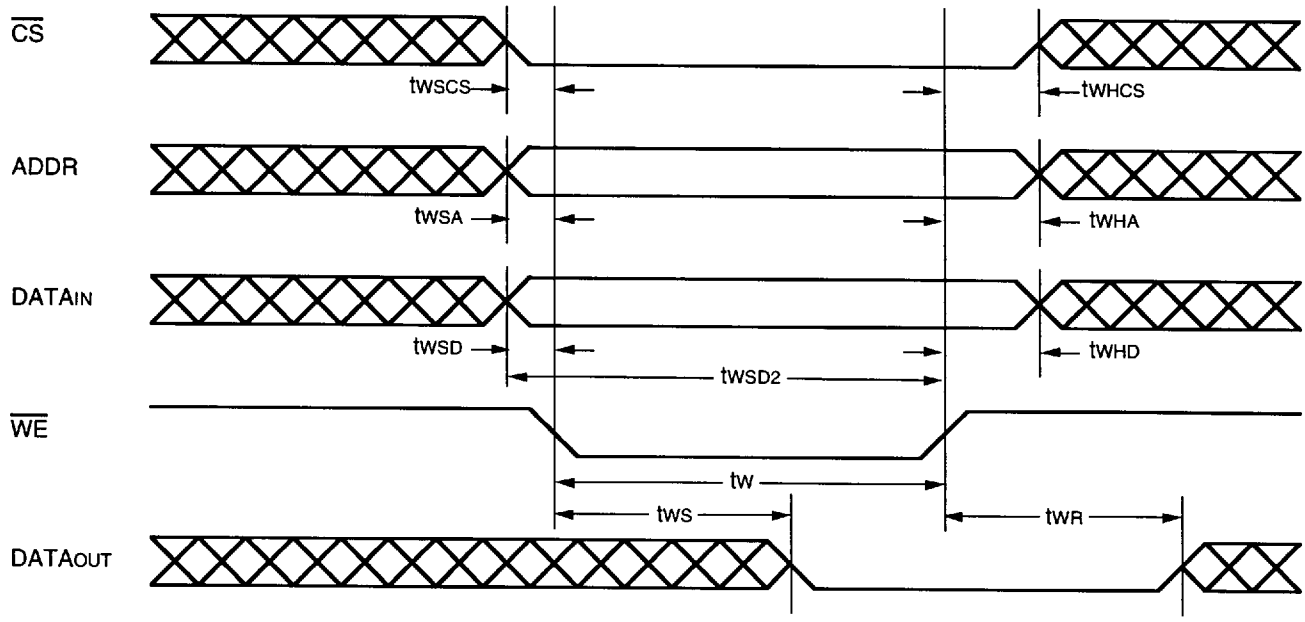
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	S4		S4.5		S5		S7		S8		S10		S15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle																
tW	Write Pulse Width (tWSA = minimum)	3.0	—	3.5	—	4.0	—	6.0	—	7.0	—	8.0	—	10.0	—	ns
tWSD	Data Set-up Time	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
tWSD2[2]	Data Set-up Time to WE High	2.0	—	2.0	—	3.0	—	5.0	—	5.0	—	5.0	—	5.0	—	ns
tWSA	Address Set-up Time (tW = minimum)	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
tWSCS	Chip Select Set-up Time	0	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
tWHD	Data Hold Time	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	ns
tWHA	Address Hold Time	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	ns
tWHCS	Chip Select Hold Time	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	1.0	—	ns
tWS	Write Disable Time	—	3.0	—	3.0	—	3.0	—	5.0	—	5.0	—	5.0	—	5.0	ns
tWR[3]	Write Recovery Time	—	3.0	—	3.0	—	3.0	—	5.0	—	5.0	—	5.0	—	5.0	ns

NOTES:
2811 tbl 08

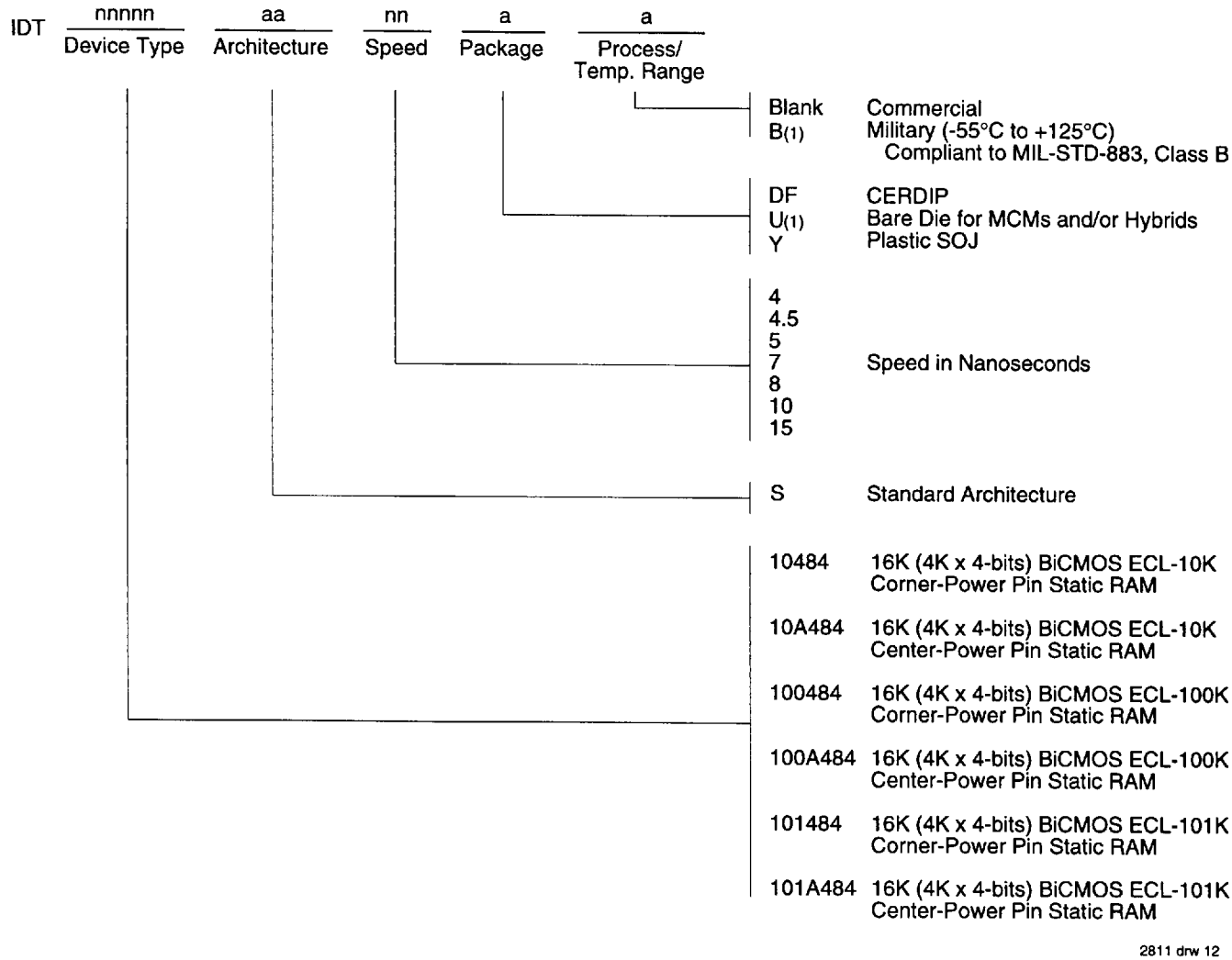
1. Input and Output reference level is 50% point of waveform.
2. tWSD is specified with respect to the falling edge of WE for compatibility with bipolar part specifications, but this device actually only requires tWSD2 with respect to rising edge of WE.
3. tWR is defined as the time to reflect the newly written data on the Data Outputs (Q0 to Q3) when no new Address Transition occurs.

WRITE CYCLE TIMING DIAGRAM



2811 drw 11

ORDERING INFORMATION(1)



2811 drw 12

NOTE:
1. Please contact your IDT Sales Representative for more information on specifications and availability of Military and Die products.

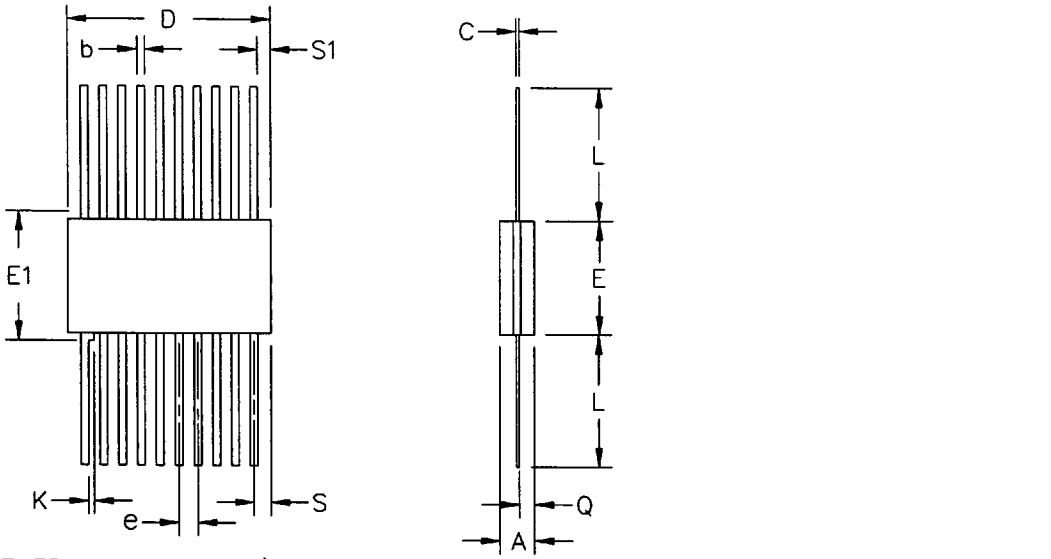
Integrated Device Technology, Inc.

2975 Stender Way, Santa Clara, CA 95054-3090 Telephone: (408) 727-6116 FAX 408-492-8674

PACKAGE DIAGRAM OUTLINES

CERPACK

REV	DCN	DESCRIPTION	DATE	APPROVED
04	17576	UPDATED TO STANDARDIZE DWG	4-6-90	S Thomas



NOTES: (UNLESS OTHERWISE SPECIFIED)
1. ALL DIMENSIONS ARE IN INCHES.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "N" REPRESENTS THE NUMBER OF LEADS.

SYMBOL	E16-1		E20-1		E24-1		E28-1		E28-2	
SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	.055	.085	.045	.092	.045	.090	.045	.115	.045	.090
b	.015	.019	.015	.019	.015	.019	.015	.019	.015	.019
C	.0045	.006	.0045	.006	.0045	.006	.0045	.006	.0045	.006
D	.370	.430	–	.540	–	.640	–	.740	–	.740
E	.245	.285	.245	.300	.300	.420	.460	.520	.340	.380
E1	–	.305	–	.305	–	.440	–	.550	–	.400
e	.050 BSC		.050 BSC		.050 BSC		.050 BSC		.050 BSC	
K	.008	.015	.008	.015	.008	.015	.008	.015	.008	.015
L	.250	.370	.250	.370	.250	.370	.250	.370	.250	.370
N	16		20		24		28		28	
Q	.026	.040	.026	.040	.026	.040	.026	.045	.026	.045
S	–	.045	–	.045	–	.045	–	.045	–	.045
S1	.005	–	.005	–	.005	–	.000	–	.005	–
MIL-M-38510	F-5		F-9		F-6		F-11A		F-11	
EXCEPTIONS	NONE		NONE		NONE		NONE		NONE	
JEDEC	MO-092-AC		NOT		NOT		NOT		NOT	
EXCEPTIONS	NONE		REGISTERED		REGISTERED		REGISTERED		REGISTERED	

TOLERANCES UNLESS OTHERWISE SPECIFIED
FRAC ± – DEC ± – ANGLES ± –

APPROVALS	DATE
DRAWN AA	03/90
CHECKED	

Integrated Device Technology, Inc.
3236 Scott Blvd., Santa Clara, CA 95051
(408) 727-6116 FAX: (408) 727-2328

CERPACK MARKETING DWG

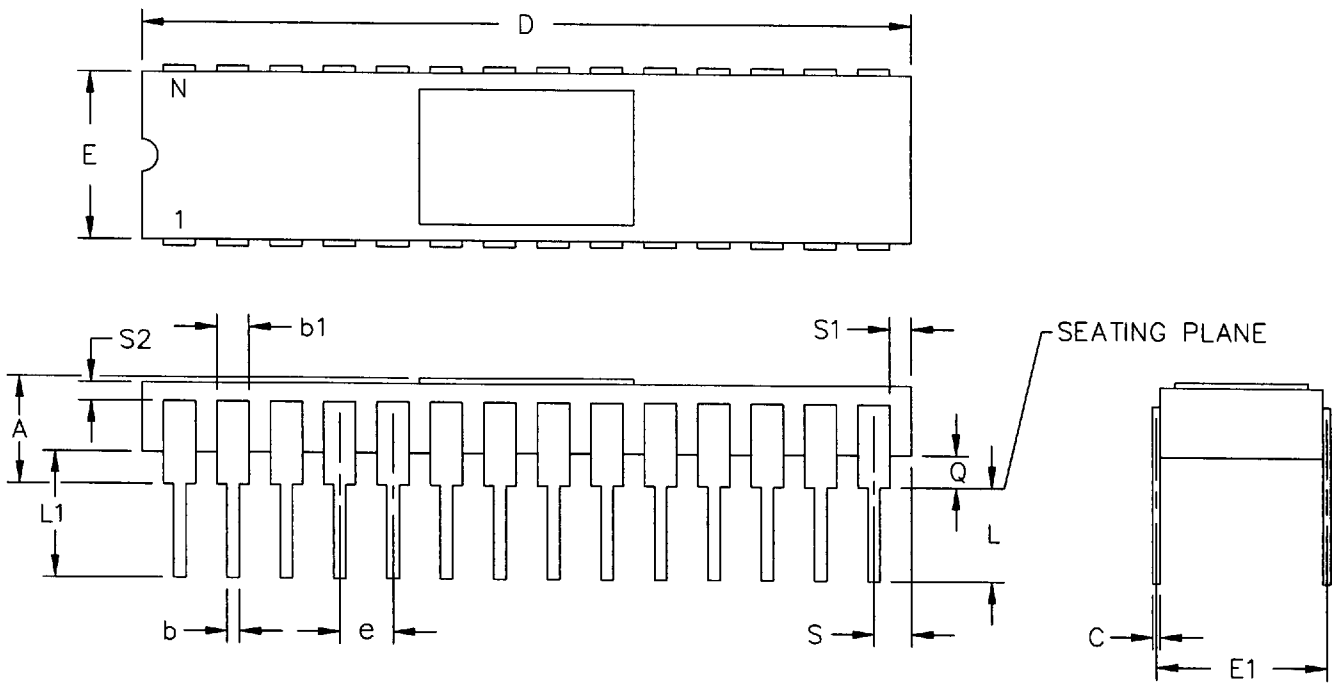
SCALE	SIZE	DRAWING NO.	REV
N/A	A	PSC-2039	04

DO NOT SCALE DRAWING | SHEET 1

PACKAGE DIAGRAM OUTLINES

SIDEBRAZE (Cont

REV	DCN	DESCRIPTION	DATE	APPROVED
05	17563	UPDATED TO STANDARDIZE DWG	4/2/90	S Thomas
06	22239	CHANGED b1 MIN DIMENSION		



NOTES: (UNLESS OTHERWISE SPECIFIED)
1. ALL DIMENSIONS ARE IN INCHES.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "N" REPRESENTS THE NUMBER OF LEADS.

DWG #	C28-2	
SYMBOL	MIN	MAX
A	.090	.200
b	.014	.023
b1	.045	.060
C	.008	.014
D	1.380	1.420
E	.380	.420
E1	.390	.420
e	.100 BSC	
L	.100	.175
L1	.150	–
N	28	
Q	.030	.060
S	.030	.065
S1	.005	–
S2	.005	–

	CONFIGURATION	EXCEPTIONS
MIL-M-38510	NOT LISTED	
JEDEC	NOT REGISTERED	

TOLERANCES UNLESS OTHERWISE SPECIFIED
FRAC ± – DEC ± – ANGLES ± –

APPROVALS	DATE
DRAWN AA	03/90
CHECKED	

Integrated Device Technology, Inc.
3236 Scott Blvd., Santa Clara, CA 95051
(408) 727-6116 FAX: (408) 727-2328

28 LD SIDE BRAZE
(400 MIL) MKT DWG

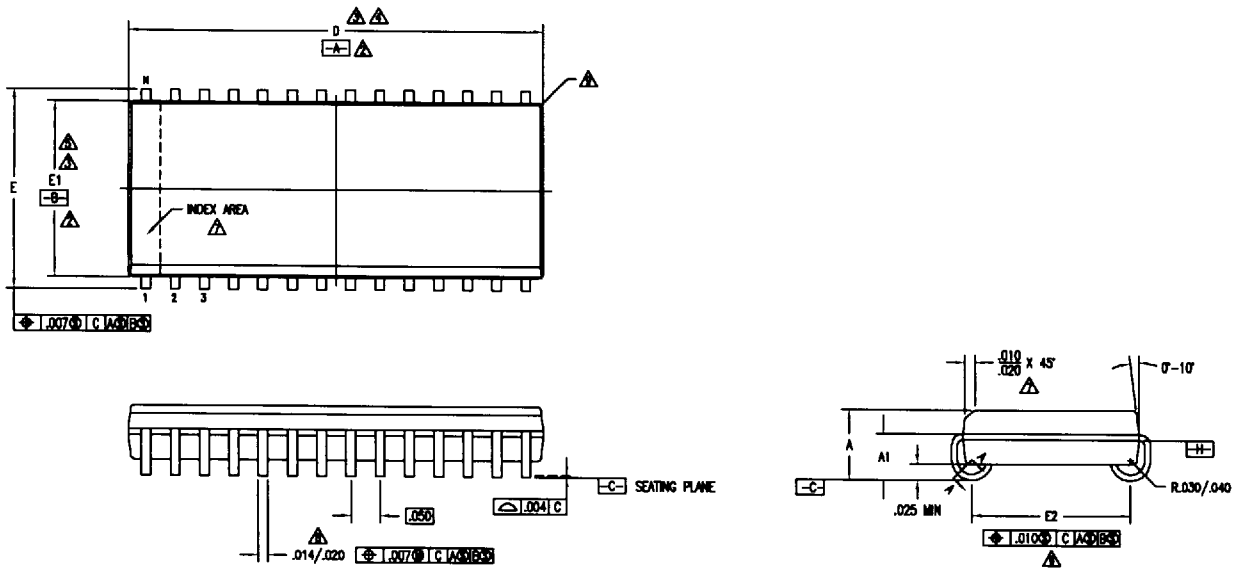
SCALE	SIZE	DRAWING NO.	REV
N/A	A	PSC-2033	06

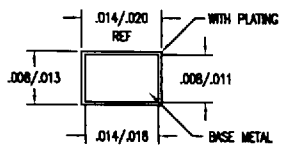
DO NOT SCALE DRAWING | SHEET 35

PACKAGE DIAGRAM OUTLINES

SOJ

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27644	03	REDRAW TO JEDEC FORMAT	03/15/95	





SECTION A-A

TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070
DECIMAL ANGULAR		
XX± ±		
XXX±		
XXXX±		
APPROVALS	DATE	TITLE PJ 20 & 28 PACKAGE OUTLINE .300" BODY WIDTH SOJ .050" PITCH
DRAWN Ad	03/15/95	
CHECKED		
		SIZE C / DRAWING No. PSC-4024 / REV 03
		DO NOT SCALE DRAWING

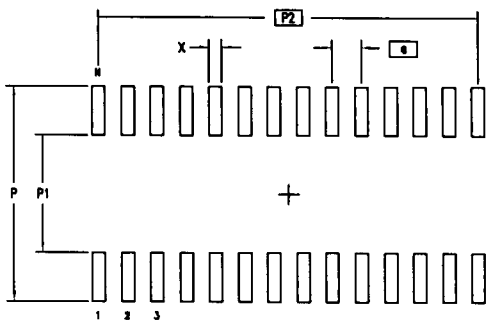
99

SOJ (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27644	03	REDRAW TO JEDEC FORMAT	03/15/95	

DWG #		SO20-1			DWG #		SO28-5		
SYMBOL	JEDEC VARIATION AD			NOTE	JEDEC VARIATION AF			NOTE
	MIN	NOM	MAX		MIN	NOM	MAX	
A	.120	.130	.140		.120	.130	.140	
A1	.078	.086	.095		.078	.086	.095	
D	.500	.506	.512	3,4	.700	.706	.712	3,4
E	.335	.340	.347		.335	.340	.347	
E1	.292	.296	.300	3,5	.292	.296	.300	3,5
E2	.262	.267	.272	6	.262	.267	.272	6
N	20				28			

LAND PATTERN DIMENSIONS



	MIN	MAX	MIN	MAX
P	.362	.370	.362	.370
P1	.196	.204	.196	.204
P2	.450 BSC		.650 BSC	
X	.018	.026	.018	.026
e	.050 BSC		.050 BSC	
N	20		28	

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE -H-
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 PER SIDE
5. DIMENSION E1 DO NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006 PER SIDE
6. DIMENSION E2 TO BE DETERMINED AT SEATING PLANE -C- CONTACT POINT
7. THE CHAMFER ON THE PACKAGE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE ZONE INDICATED
8. LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .004 IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION
9. EXACT SHAPE OF EACH CORNER IS OPTIONAL
10. ALL DIMENSIONS ARE IN INCHES
11. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-088, VARIATION AD & AF

TOLERANCES UNLESS SPECIFIED	
DECIMAL	ANGULAR
.XX±	±
.XXX±	
.XXXX±	

APPROVALS	DATE
DRAWN AA	03/15/95
CHECKED	

Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA 95054
PHONE: (408) 727-6116
FAX: (408) 492-8674 TWX: 910-338-2070

TITLE: PJ 20 & 28 PACKAGE OUTLINE .300" BODY WIDTH SOJ .050" PITCH

SIZE	DRAWING No.	REV
C	PSC-4024	03

DO NOT SCALE DRAWING