Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS ECL STATIC RAM 16K (4K x 4-BIT) SRAM

PRELIMINARY
IDT10A484
IDT100A484
IDT101A484

FEATURES:

- 4096-words x 4-bit organization
- Address access time: 5/7/8/10 ns
- Low power dissipation: 700mW (typ.)
- Guaranteed Output Hold time
- Fully compatible with ECL logic levels
- Separate data input and output
- Center-power pinout for reduced noise
- Standard through-hole and surface mount packages

NOTICE
SEE ORDER OF DATA FOR ERRATA INFORMATION

DESCRIPTION:

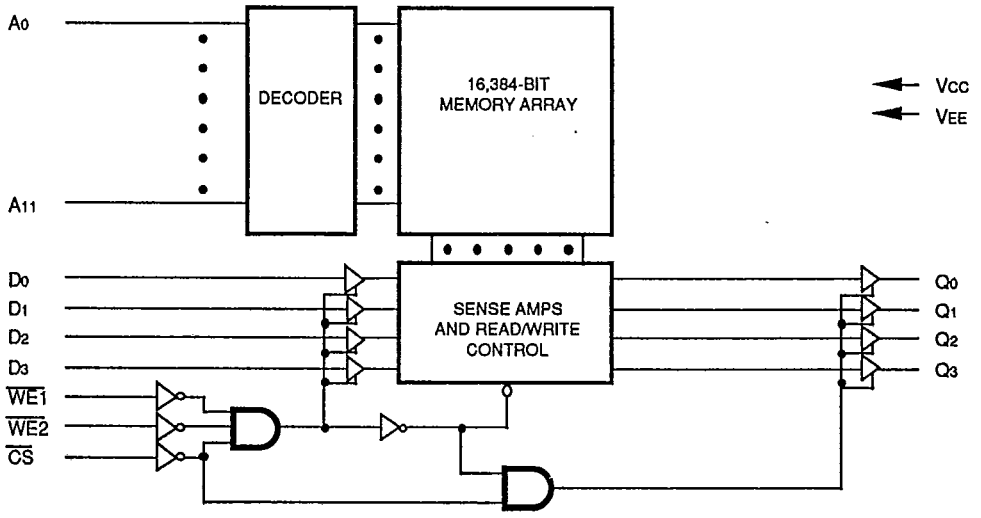
The IDT10A484, IDT100A484 and IDT101A484 are 16,384-bit high-speed BiCEMOS™ ECL static random access memories organized as 4Kx4, with separate data inputs and outputs. All I/Os are fully compatible with ECL levels.

These devices are part of a family of asynchronous four-bit-wide ECL SRAMs. This device have been configured to follow the center-power pinout for reduced noise allowing higher speed operation. Because they are manufactured in BiCEMOS™ technology, power dissipation is greatly reduced over equivalent bipolar devices.

The asynchronous SRAMs are the most straightforward to use because no additional clocks or controls are required: $Data_{OUT}$ is available an access time after the last change of address. To write data into the device requires the creation of a Write Pulse, and the write cycle disables the output pins in conventional fashion. Two Write Enable inputs are supplied, so the write pulse is created as a logical-AND of these signals to allow write gating at the device for minimal skew.

The fast access time and guaranteed Output Hold time allow greater margin for system timing variation. $Data_{IN}$ setup time specified with respect to the trailing edge of Write Pulse eases write timing allowing balanced Read and Write cycle times.

FUNCTIONAL BLOCK DIAGRAM



2811 drw 01

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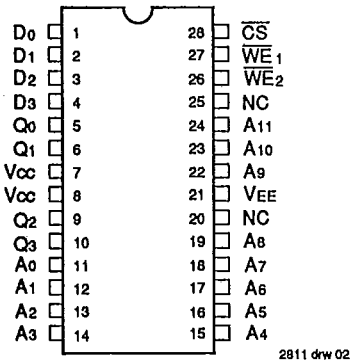
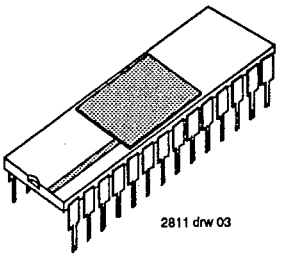
PIN CONFIGURATION

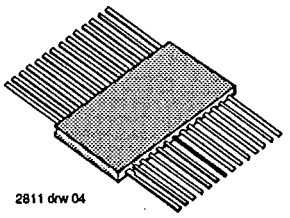
T-46-23-08



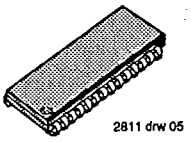
TOP VIEW



400-Mil-Wide
CERAMIC PACKAGE
C28



400-Mil-Wide
CERPACK
E28



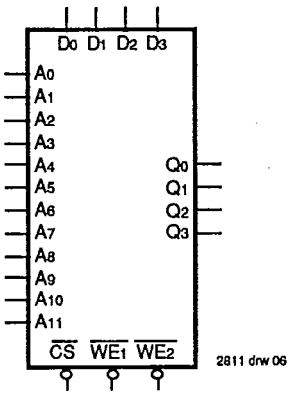
300-Mil-Wide
PLASTIC SOJ PACKAGE
Y28

PIN DESCRIPTIONS

Symbol	Pin Name
A0 through A11	Address Inputs
D0 through D3	Data Inputs
Q0 through Q3	Data Outputs
$\overline{WE}_1$, $\overline{WE}_2$	Write Enable Input
$\overline{CS}$	Chip Select Input (Internal pull down)
VEE	More Negative Supply Voltage
Vcc	Less Negative Supply Voltage

2811 tbl 01

LOGIC SYMBOL



4Kx4
SRAM

AC OPERATING RANGES(1)

I/O	VEE	Temperature
10K	-5.2V ±5%	0 TO 75°C, air flow exceeding 2 m/sed
100K	-4.5V ±5%	0 TO 85°C, air flow exceeding 2 m/sed
101K	-4.75V to -5.46V	0 TO 75°C, air flow exceeding 2 m/sed

NOTE: 2811 tbl 02
1. Referenced to Vcc

CAPACITANCE (TA=+25°C, f=1.0MHz)

Symbol	Parameter	DIP Typ	DIP Max	FP Typ	FP Max	SOJ Typ	SOJ Max	Unit
CIN	Input Capacitance	4	–	TBD	–	3	–	pF
COUT	Output Capacitance	6	–	TBD	–	3	–	pF

2811 tbl 03

TRUTH TABLE(1)

$\overline{CS}$	$\overline{WE1}$	$\overline{WE2}$	DataOUT	Function
H	X	X	L	Deselected
L	H	X	RAM Data	Read
L	X	H	RAM Data	Read
L	L	L	WRITE Data	Write

NOTE: 2811 tbl 04
1. H=High, L=Low, X=Don't Care

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ECL-10K ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +75	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		1.5	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2811 tbl 02

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-10K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, RL=50Ω to -2.0V, T_A = 0 to +75°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.[1]	Max. (A)	Unit	T_A
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1000 -960 -900	-885	-840 -810 -720	mV	0°C 25°C 75°C
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1870 -1850 -1830	–	-1665 -1650 -1625	mV	0°C 25°C 75°C
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1020 -980 -920	–	–	mV	0°C 25°C 75°C
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1645 -1630 -1605	mV	0°C 25°C 75°C
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1145 -1105 -1045	–	-840 -810 -720	mV	0°C 25°C 75°C
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1870 -1850 -1830	–	-1490 -1475 -1450	mV	0°C 25°C 75°C
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA	–
			Others	–	–	110	µA	–
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA	–
			Others	-50	–	90	µA	–
I_{EE}	Supply Current	All Inputs and Outputs Open		-190	-130	–	mA	–

2811 tbl 05

NOTE:
1. Typical parameters are specified at V_{EE} = -5.2V, T_A = +25°C and maximum loading.

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ECL-100K ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +85	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		1.5	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2811 tbl 07

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ECL-100K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -4.5V, RL = 50Ω to -2.0V, T_A = 0 to +85°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Conditions		Min. (B)	Typ.(1)	Max. (A)	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1025	-955	-880	mV
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1810	-1715	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1035	–	–	mV
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1165	–	-880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1810	–	-1475	mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	90	
I_{EE}	Supply Current	All Inputs and Outputs Open		-170	-110	–	mA

2811 tbl 08

NOTE:
1. Typical parameters are specified at V_{EE} = -4.5V, T_A = +25°C and maximum loading.

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ECL-101K ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating		Value	Unit
V_{TERM}	Terminal Voltage With Respect to GND		+0.5 to -7.0	V
T_A	Operating Temperature		0 to +75	°C
T_{BIAS}	Temperature Under Bias		-55 to +125	°C
T_{STG}	Storage Temperature	Ceramic	-65 to +150	°C
		Plastic	-55 to +125	
P_T	Power Dissipation		1.5	W
I_{OUT}	DC Output Current (Output High)		-50	mA

2811 tbl 09

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

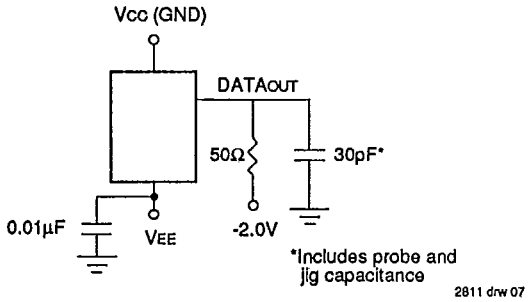
ECL-101K DC ELECTRICAL CHARACTERISTICS

(V_{EE} = -5.2V, R_L = 50Ω to -2.0V, T_A = 0 to +75°C, air flow exceeding 2 m/sec)

Symbol	Parameter	Test Condition		Min. (B)	Typ.(1)	Max. (A)	Unit
V_{OH}	Output HIGH Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1025	-955	-880	mV
V_{OL}	Output LOW Voltage	$V_{IN} = V_{IHA}$ or V_{ILB}		-1810	-1715	-1620	mV
V_{OHC}	Output Threshold HIGH Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		-1035	–	–	mV
V_{OLC}	Output Threshold LOW Voltage	$V_{IN} = V_{IHB}$ or V_{ILA}		–	–	-1610	mV
V_{IH}	Input HIGH Voltage	Guaranteed Input Voltage High for All Inputs		-1165	–	-880	mV
V_{IL}	Input LOW Voltage	Guaranteed Input Voltage Low for All Inputs		-1810	–	-1475	mV
I_{IH}	Input HIGH Current	$V_{IN} = V_{IHA}$	$\overline{CS}$	–	–	220	µA
			Others	–	–	110	
I_{IL}	Input LOW Current	$V_{IN} = V_{ILB}$	$\overline{CS}$	0.5	–	170	µA
			Others	-50	–	90	
I_{EE}	Supply Current	All Inputs and Outputs Open		-190	-130	–	mA

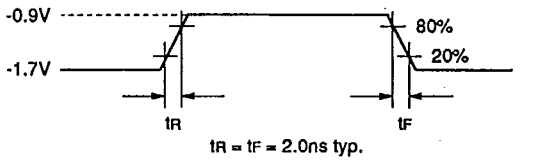
2811 tbl 10

AC TEST LOAD CONDITION



2811 drw 07

AC TEST INPUT PULSE T-46-23-08



tR = tF = 2.0ns typ.

Note: All timing measurements are referenced to 50% input levels.

2811 drw 08

RISE/FALL TIME

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
tR	Output Rise Time	–	–	2	–	ns
tF	Output Fall Time	–	–	2	–	ns

2811 tbl 11

FUNCTIONAL DESCRIPTION

The IDT10484, IDT100484, and IDT101484 BiCMOS ECL static RAMs (SRAM) provide high speed with low power dissipation typical of BiCMOS ECL. These devices follow the center-power pinout for 4Kx4 ECL SRAMs, reducing noise over corner-power versions allowing for improved system performance. (For corner-power pinouts, please see the IDT10484, IDT100494, and IDT101484, respectively.) The ECL-101K meets electrical specifications that combine the ECL-100K temperature and voltage compensated output levels with the high-speed of ECL-10K VEE compatibility (-5.2V).

READ TIMING

The read timing on these asynchronous devices is straightforward. DataOUT is held low until the device is selected by Chip Select (CS). Then Address (ADDR) settles and data appears on the output after time tAA. Note that DataOUT is held for a short time (tOH) after the address begins to change for the next access, then ambiguous data is on the bus until a new time tAA.

WRITE TIMING

To write data to the device, a Write Pulse need be formed to control the write to the SRAM array. This Write Pulse, called $\overline{WE}$, is formed inside the device as the logical-AND of the $\overline{WE1}$ and $\overline{WE2}$ inputs; that is, when $\overline{WE1}$ and $\overline{WE2}$ both are driven low, $\overline{WE}$ goes low and the write cycle begins.

While $\overline{CS}$ and ADDR must be set-up when $\overline{WE}$ goes low, DataIN can settle after the falling edge of $\overline{WE}$, giving the data path extra margin. Data is written to the memory cell at the end of the Write Pulse, and addresses and Chip Select must be held after the rising edge of the Write Pulse to ensure satisfactory completion of the cycle.

DataOUT is disabled (held low) during the Write Cycle. If $\overline{CS}$ is held low (active) and addresses remain unchanged, the DataOUT pins will output the written data after "Write Recovery Time" (tWR).

Because of the very short Write Pulse requirement, these devices can be cycled as quickly for Writes as for Reads. Balanced cycles mean simpler timing in cache applications.

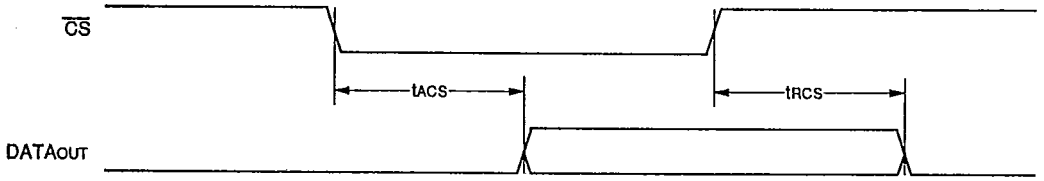
AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

Symbol	Parameter[1]	Test Condition	10A484S5 100A484S5 101A484S5		10A484S7 100A484S7 101A484S7		10A484S8 100A484S8 101A484S8		10A484S10 100A484S10 101A484S10		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle											
tACS	Chip Select Access Time	–	–	2	–	3	–	5	–	5	ns
tRCS	Chip Select Recovery Time	–	–	2	–	3	–	5	–	5	ns
tAA	Address Access Time	–	–	5	–	7	–	8	–	10	ns
tOH	Data Hold from Address Change	–	2	–	3	–	3	–	3	–	ns

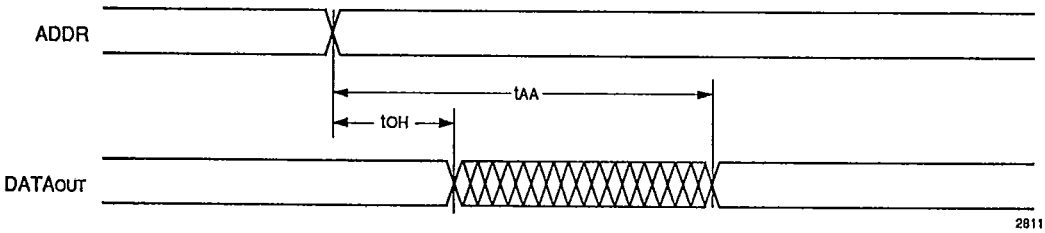
NOTE:
1. Input and Output reference level is 50% point of waveform.

2811 tbl 12

READ CYCLE GATED BY CHIP SELECT



READ CYCLE GATED BY ADDRESS



2811 drw 09

AC ELECTRICAL CHARACTERISTICS (Over the AC Operating Range)

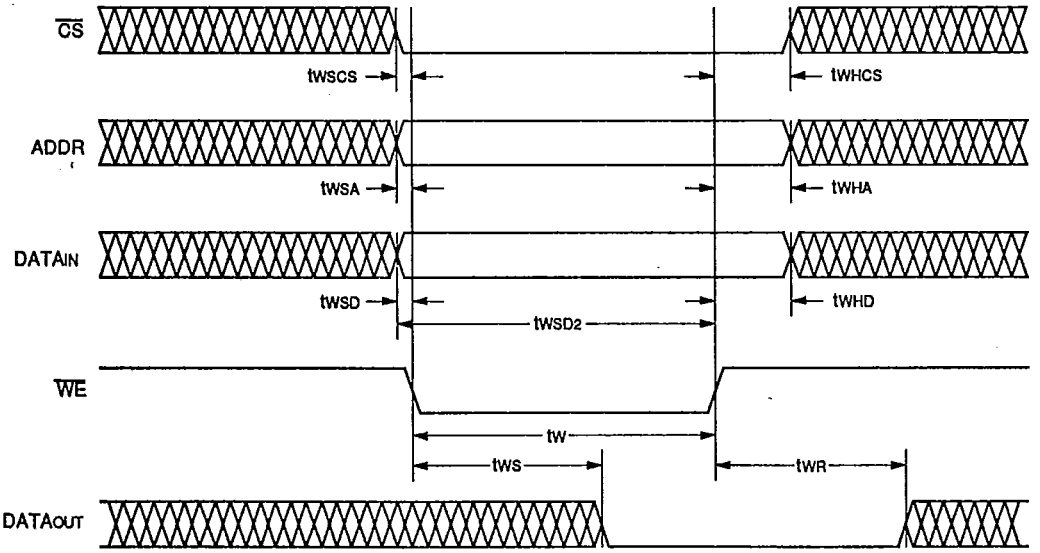
T-46-23-08

Symbol	Parameter[1]	Test Condition	10A484S5 100A484S5 101A484S5		10A484S7 100A484S7 101A484S7		10A484S8 100A484S8 101A484S8		10A484S10 100A484S10 101A484S10		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle											
tW	Write Pulse Width	tWSA= minimum	3	–	5	–	6	–	8	–	ns
tWSD	Data Set-up Time	–	0	–	0	–	0	–	0	–	ns
tWSD2[2]	Data Set-up Time to $\overline{WE}$ High	–	3	–	5	–	5	–	5	–	ns
tWSA	Address Set-up Time	tWSA= minimum	0	–	0	–	0	–	0	–	ns
tWSCS	Chip Select Set-up Time	–	0	–	0	–	0	–	0	–	ns
tWHD	Data Hold Time	–	1	–	1	–	1	–	1	–	ns
tWHA	Address Hold Time	–	1	–	1	–	1	–	1	–	ns
tWHCS	Chip Select Hold Time	–	1	–	1	–	1	–	1	–	ns
tWS	Write Disable Time	–	–	3	–	5	–	5	–	5	ns
tWR[3]	Write Recovery Time	–	–	3	–	5	–	5	–	5	ns

NOTES: 2811 tbl 13

1. Input and Output reference level is 50% point of waveform.
2. tWSD is specified with respect to the falling edge of $\overline{WE}$ for compatibility with bipolar part specifications, but this device actually only requires tWSD2 with respect to rising edge of $\overline{WE}$.
3. tWR is defined as the time to reflect the newly written data on the Data Outputs (Q_0 to Q_3) when no new Address Transition occurs.

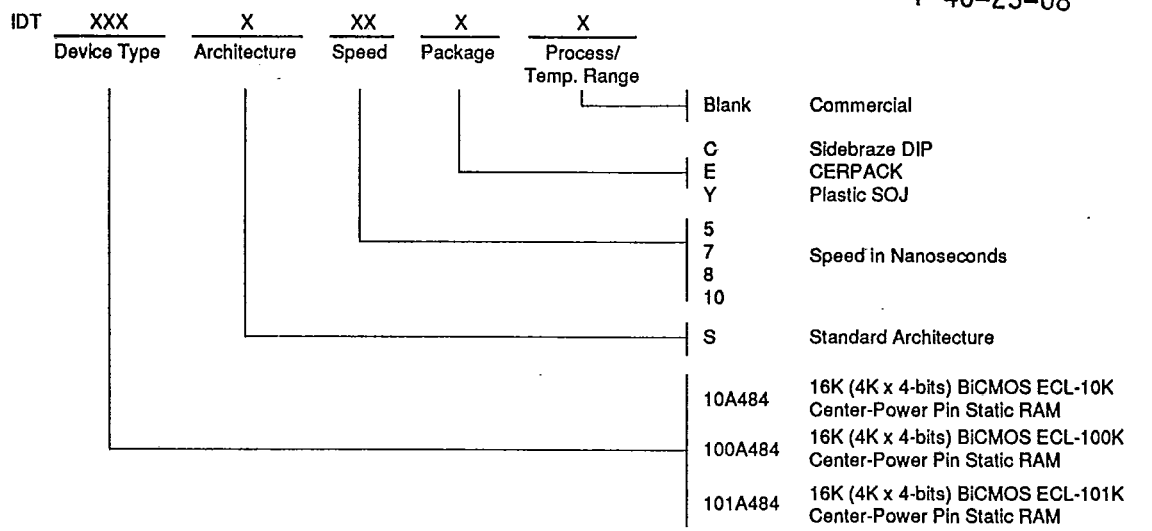
WRITE CYCLE TIMING DIAGRAM



2811 drw 10

ORDERING INFORMATION

T-46-23-08



2811 drw 11