Integrated Device Technology, Inc.

FAST CMOS OCTAL REGISTERED TRANSCEIVERS

IDT29FCT52AT/BT/CT/DT
IDT29FCT53AT/BT/CT

T-52-30-08

FEATURES:

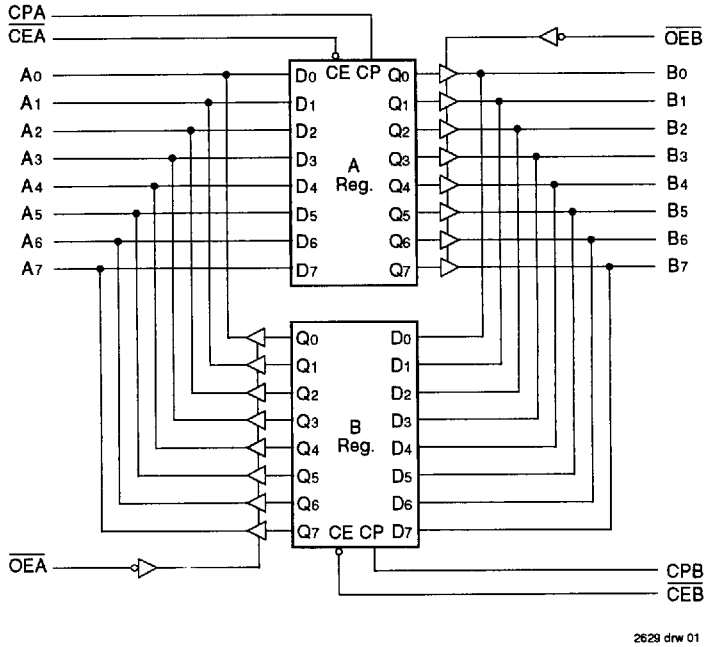
- Fastest CMOS logic family available
- A, B, C and D speed grades with 4.5ns t_{PD}
- Available in DIP, SOIC, SSOP, CERPACK and LCC packages
- Power-off disable feature allows "hot-insertion"
- CMOS power levels (2.5mW typ. static)
- TTL input and output level compatible
- I_{OFF} feature ideal for hot switching of backplane drivers
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT29FCT52AT/BT/CT/DT and IDT29FCT53AT/BT/CT are 8-bit registered transceivers manufactured using advanced CEMOS™, a dual metal CMOS technology. Two 8-bit back-to-back registers store data flowing in both directions between two bidirectional buses. Separate clock, clock enable and 3-state output enable signals are provided for each register. Both A outputs and B outputs are guaranteed to sink 64mA.

The IDT29FCT52AT/BT/CT/DT is a non-inverting option of the IDT29FCT53AT/BT/CT.

FUNCTIONAL BLOCK DIAGRAM(1)



2629 drw 01

NOTE:
1. IDT29FCT52T function is shown. IDT29FCT53T is the inverting option.

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FAST is a trademark of National Semiconductor Co.

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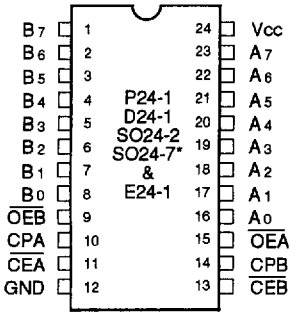
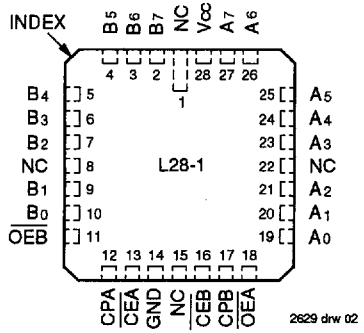
PIN CONFIGURATIONS



DIP/SOIC/SSOP/CERPACK
TOP VIEW

* For 29FCT52AT/BT/CT only



LCC
TOP VIEW

PIN DESCRIPTION

Name	I/O	Description
A_{0-7}	I/O	Eight bidirectional lines carrying the A Register inputs or B Register outputs.
B_{0-7}	I/O	Eight bidirectional lines carrying the B Register inputs or A Register outputs.
CPA	I	Clock for the A Register. When $\overline{CEA}$ is LOW, data is entered into the A Register on the LOW-to-HIGH transition of the CPA signal.
$\overline{CEA}$	I	Clock Enable for the A Register. When $\overline{CEA}$ is LOW, data is entered into the A Register on the LOW-to-HIGH transition of the CPA signal. When $\overline{CEA}$ is HIGH, the A Register holds its contents, regardless of CPA signal transitions.
$\overline{OEB}$	I	Output Enable for the A Register. When $\overline{OEB}$ is LOW, the A Register outputs are enabled onto the B_{0-7} lines. When $\overline{OEB}$ is HIGH, the B_{0-7} outputs are in the high-impedance state.
CPB	I	Clock for the B Register. When $\overline{CEB}$ is LOW, data is entered into the B Register on the LOW-to-HIGH transition of the CPB signal.
$\overline{CEB}$	I	Clock Enable for the B Register. When $\overline{CEB}$ is LOW, data is entered into the B Register on the LOW-to-HIGH transition of the CPB signal. When $\overline{CEB}$ is HIGH, the B Register holds its contents, regardless of CPB signal transitions.
$\overline{OEA}$	I	Output Enable for the B Register. When $\overline{OEA}$ is LOW, the B Register outputs are enabled onto the A_{0-7} lines. When $\overline{OEA}$ is HIGH, the A_{0-7} outputs are in the high-impedance state.

2629 tbl 05

REGISTER FUNCTION TABLE[1]
(Applies to A or B Register)

Inputs			Internal	
D	CP	$\overline{CE}$	Q	Function
X	X	H	NC	Hold Data
L	↑	L	L	Load Data
H	↑	L	H	

2629 tbl 06

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   NC = No Change
   ↑ = LOW-to-HIGH Transition

OUTPUT CONTROL[1]

	Internal	Y-Outputs		
$\overline{OE}$	Q	52	53	Function
H	X	Z	Z	Disable Outputs
L	L	L	H	Enable Outputs
L	H	H	L	

2629 tbl 07

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High Impedance

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2529 tbl 01

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed +0.5V unless otherwise noted.
2. Inputs and V_{CC} terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2640 tbl 02

1. This parameter is guaranteed by characterization data and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_I = 2.7V	Except I/O Pins	—	—	5	µA
			I/O Pins	—	—	15	
I_{IL}	Input LOW Current	V_{CC} = Max., V_I = 0.5V	Except I/O Pins	—	—	–5	µA
			I/O Pins	—	—	–15	
I_I	Input HIGH Current	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	20	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		–60	–120	–225	mA
I_{OFF}	Power Down Disable	V_{CC} = GND, V_O = 4.5V		—	—	100	µA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	3.3	—	V
			I_{OH} = –12mA MIL. I_{OH}= –15mA COM'L.	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48mA MIL.(4) I_{OL} = 64mA COM'L.	—	0.3	0.55	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = GND or V_{CC}		—	0.5	1.5	mA

NOTES: 2629 tbl 03

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. These are maximum I_{OL} values per output, for 8 outputs turned on simultaneously. Total maximum I_{OL} (all outputs) is 512mA for commercial and 384mA for military. Derate I_{OL} for number of outputs exceeding 8 turned on simultaneously.

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POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE_A}$ or $\overline{OE_B}$ = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE_A}$ or $\overline{OE_B}$ = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	2.0	4.0	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2.5	6.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE_A}$ or $\overline{OE_B}$ = GND Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	4.3	7.8[5]	
			V_{IN} = 3.4V V_{IN} = GND	—	6.5	16.8[5]	

2629 tbl 04

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the ICC formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at DH
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	29FCT52AT/53AT				29FCT52BT/53BT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay CPA, CPB to An, Bn	C_L = 50pF R_L = 500Ω	2.0	10.0	2.0	11.0	2.0	7.5	2.0	8.0	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEA}$ or $\overline{OEB}$ to An, Bn		1.5	10.5	1.5	13.0	1.5	8.0	1.5	8.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEA}$ or $\overline{OEB}$ to An, Bn		1.5	10.0	1.5	10.0	1.5	7.5	1.5	8.0	ns
t_{SU}	Set-up Time, HIGH or LOW An, Bn to CPA, CPB		2.5	—	2.5	—	2.5	—	2.5	—	ns
t_H	Hold Time, HIGH or LOW An, Bn to CPA, CPB		2.0	—	2.0	—	1.5	—	1.5	—	ns
t_{SU}	Set-up Time, HIGH or LOW $\overline{CEA}$, $\overline{CEB}$ to CPA, CPB		3.0	—	3.0	—	3.0	—	3.0	—	ns
t_H	Hold Time, HIGH or LOW $\overline{CEA}$, $\overline{CEB}$ to CPA, CPB		2.0	—	2.0	—	2.0	—	2.0	—	ns
t_W	Clock Pulse Width HIGH or LOW[3]		3.0	—	3.0	—	3.0	—	3.0	—	ns

Symbol	Parameter	Condition[1]	29FCT52CT/53CT				29FCT52DT				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay CPA, CPB to An, Bn	C_L = 50pF R_L = 500Ω	2.0	6.3	2.0	7.3	2.0	4.5	—	—	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEA}$ or $\overline{OEB}$ to An, Bn		1.5	7.0	1.5	8.0	1.5	5.6	—	—	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEA}$ or $\overline{OEB}$ to An, Bn		1.5	6.5	1.5	7.5	1.5	4.3	—	—	ns
t_{SU}	Set-up Time, HIGH or LOW An, Bn to CPA, CPB		2.5	—	2.5	—	1.5	—	—	—	ns
t_H	Hold Time, HIGH or LOW An, Bn to CPA, CPB		1.5	—	1.5	—	1.0	—	—	—	ns
t_{SU}	Set-up Time, HIGH or LOW $\overline{CEA}$, $\overline{CEB}$ to CPA, CPB		3.0	—	3.0	—	2.0	—	—	—	ns
t_H	Hold Time, HIGH or LOW $\overline{CEA}$, $\overline{CEB}$ to CPA, CPB		2.0	—	2.0	—	1.0	—	—	—	ns
t_W	Clock Pulse Width HIGH or LOW[3]		3.0	—	3.0	—	3.0	—	—	—	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

2629 tbl 08

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