Integrated Device Technology, Inc.

4-BIT CMOS MICROPROCESSOR SLICE

IDT39C01C
IDT39C01D
IDT39C01E

FEATURES:

- Low-power CEMOS™
  - Icc (max.)
    Military: 35mA
    Commercial: 30mA
  Fast
  - IDT39C01C — meets 2901C speeds
  - IDT39C01D — 20% speed upgrade
  - IDT39C01E — 40% speed upgrade
- Eight-function ALU
  - Performs addition, two subtraction operations and five logic functions on two source operands
- Expandable
  - Longer word lengths achieved through cascading any number of IDT39C01s
- Four status flags
  - Carry, overflow, negative and zero
- Pin-compatible and functionally equivalent to all versions of the 2901
- Available in 40-pin DIP and 44-pin LCC
- Military product available compliant to MIL-STD-883 and DESC Standard Military Drawing (SMD) 5962-88535

DESCRIPTION:

The IDT39C01s are high-speed, cascadable ALUs which can be used to implement CPUs, peripheral controllers and programmable microprocessors. The IDT39C01's microinstruction flexibility allows for easy emulation of most digital computers.

This extremely low-power yet high-speed ALU consists of a 16-word-by-4-bit dual-port RAM, a high-speed ALU and the required shifting, decoding and multiplexing logic. It is expandable in 4-bit increments, contains a flag output along with three-state data outputs, and can easily use either a ripple carry or full lookahead carry. The nine-bit microinstruction word is organized into three groups of three bits each and selects the ALU destination register, ALU source operands and the ALU function.

The IDT39C01 is fabricated using CEMOS™, a CMOS technology designed for high-performance and high-reliability. It is a pin-compatible, performance-enhanced, functional replacement for all versions of the 2901.

Military grade product is manufactured in compliance with the latest version of MIL-STD-883, Class B.

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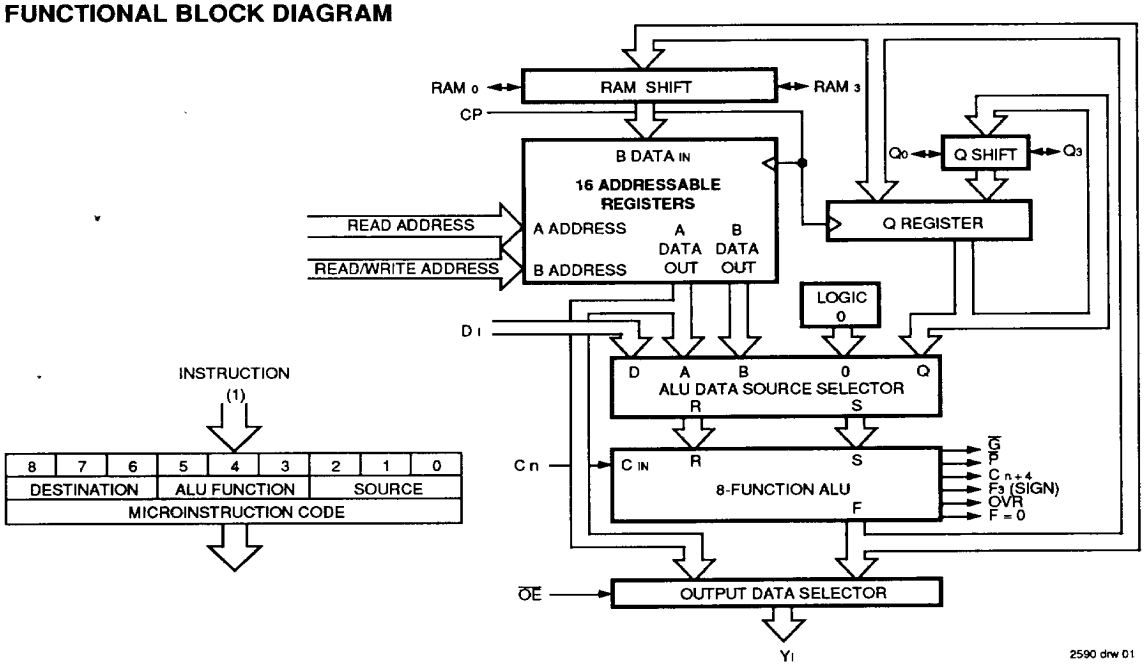
FUNCTIONAL BLOCK DIAGRAM



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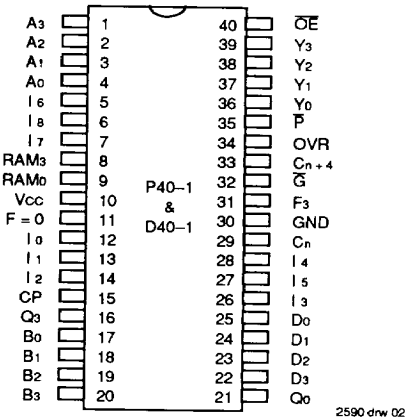
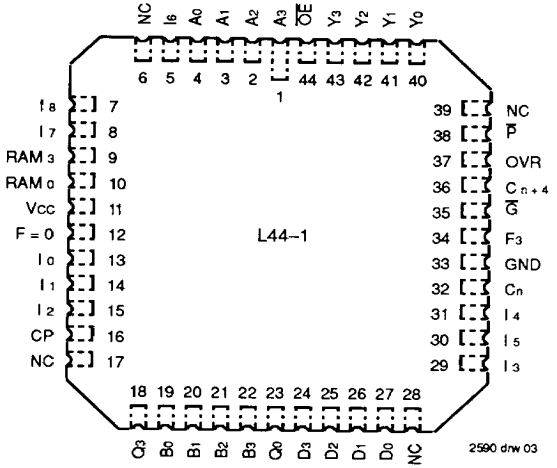
PIN CONFIGURATION



DIP
TOP VIEW



LCC
TOP VIEW

PIN DESCRIPTIONS

Pin Name	I/O	Description
A_0 - A_3	I	Four address inputs to the register file which select one register and displays its contents through the A port.
B_0 - B_3	I	Four address inputs to the register file which select one of the registers in the file, the contents of which is displayed through the B port. They also select the location into which new data can be written when the clock goes LOW.
I_0 - I_8	I	Nine instruction control lines which determine what data source will be applied to the ALU $I_{(0, 1, 2)}$, what function the ALU will perform $I_{(3, 4, 5)}$ and what data is to be deposited in the Q Register or the register file $I_{(6, 7, 8)}$.
D_0 - D_3	I	Four-bit direct data inputs which are the data source for entering external data into the device. D_0 is the LSB.
Y_0 - Y_3	O	Four three-state output lines which, when enabled, display either the four outputs of the ALU or the data on the A port of the register stack. This is determined by the destination code $I_{(6, 7, 8)}$.
F_3	O	Most significant ALU output bit (sign-bit).
F = 0	O	Open drain output which goes HIGH if the F_0 - F_3 ALU outputs are all LOW. This indicates that the result of an ALU operation is zero (positive logic).
C_n	I	Carry-in to the internal ALU.
C_{n+4}	O	Carry-out of the internal ALU.
Q_3 RAM_3	I/O	Bidirectional lines controlled by $I_{(6, 7, 8)}$. Both are three-state output drivers connected to the TTL-compatible CMOS inputs. When the destination code on $I_{(6, 7, 8)}$ indicates an up shift, the three-state outputs are enabled, the MSB of the Q Register is available on the Q_3 pin and the MSB of the ALU output is available on the RAM_3 pin. When the destination code indicates a down shift, the pins are the data inputs to the MSB of the Q Register and the MSB of the RAM.
Q_0 RAM_0	I/O	Both bidirectional lines function identically to Q_3 and RAM_3 lines except they are the LSB of the Q Register and RAM.
$\overline{OE}$	I	Output enable on which, when pulled HIGH, the Y outputs are OFF (high impedance). When pulled LOW, the Y outputs are enabled.
$\overline{G}$, $\overline{P}$	O	Carry generate and carry propagate output of the ALU. These are used to perform a carry lookahead operation.
OVR	O	Overflow. This pin is logically the Exclusive-OR of the carry-in and carry-out of the MSB of the ALU. At the most significant end of the word, this pin indicates that the result of an arithmetic two's complement operation has overflowed into the sign-bit.
CP	I	Clock input. LOW-to-HIGH clock transitions will change the Q Register and the register file outputs. Clock LOW time is internally the write enable time for the 16 x 4 RAM which comprises the master latches of the register file. While the clock is LOW, the slave latches on the RAM outputs are closed, storing the data previously on the RAM outputs. Synchronous MASTER-SLAVE operation of the register file is achieved by this.

2590 tbl 01

ALU SOURCE OPERAND CONTROL

Mnemonic	Microcode				ALU Source Operands	
	I_2	I_1	I_0	Octal Code	R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	0	Q
ZB	L	H	H	3	0	B
ZA	H	L	L	4	0	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	0

2590 tbl 02

ALU FUNCTION CONTROL

Mnemonic	Microcode				ALU Function	Symbol
	I_5	I_4	I_3	Octal Code		
ADD	L	L	L	0	R Plus S	R + S
SUBR	L	L	H	1	S Minus R	S − R
SUBS	L	H	L	2	R Minus S	R − S
OR	L	H	H	3	R OR S	$R \vee S$
AND	H	L	L	4	R AND S	$R \wedge S$
NOTRS	H	L	H	5	$\overline{R}$ AND S	$\overline{R} \wedge S$
EXOR	H	H	L	6	R EX-OR S	$R \nabla S$
EXNOR	H	H	H	7	R EX-NOR S	$\overline{R \nabla S}$

2590 tbl 03

DEVICE ARCHITECTURE:

The IDT39C01 CMOS bit-slice microprocessor is configured four bits wide and is cascadable to any number of bits (4, 8, 12, 16, etc.). Key elements which make up this four-bit microprocessor slice are: 1) the register file (16 x 4 dual-port RAM) with shifter; 2) ALU and 3) Q Register and shifter.

REGISTER FILE — RAM data is read from the A port as controlled by the 4-bit A address field input. Data, as defined by the B address field input, can be simultaneously read from the B port of the RAM. This same code can be applied to the A select and B select field with the identical data appearing at both the RAM A port and B port outputs, simultaneously. New data is written into the file (word) defined by the B address field of the RAM when activated by the RAM write enable. The RAM data input field is driven by a 3-input multiplexer that is used to shift the ALU output data (F). It is capable of shifting the data up one position, down one position or not shifting at all. The other inputs to the multiplexer are from the RAM_3 and RAM_0 I/O pins. For a shift up operation, the RAM_3 output buffer is enabled and the RAM_0 multiplexer input is enabled. During a shift down operation, the RAM_0 output buffer is enabled and the RAM_3 multiplexer input is enabled. Four-bit latches hold the RAM data while the clock is LOW, with the A port output and B port output each driving separate latches. The data to be written into the RAM is applied from the ALU F output.

ALU — The ALU can perform three binary arithmetic and five logic operations on the two 4-bit input words S and R. The S input field is driven from a 3-input multiplexer and the R input field is driven from a 2-input multiplexer, with both having an inhibit capability. Both multiplexers are controlled by the I_0, I_1, I_2 inputs. This multiplexer configuration enables the user to select various pairs of the A, B, D, Q and "0" inputs as source operands to the ALU. Microinstruction inputs (I_3, I_4, I_5) are used to select the ALU function. This high-speed ALU also incorporates a carry-in (C_n) input, carry propagate ($\overline{P}$) output, carry generate ($\overline{G}$) output and carry-out (C_{n+4}) all aimed at accelerating arithmetic operations by the use of carry look ahead logic. The overflow output pin (OVR) will be HIGH when arithmetic operations exceed the two's complement number range. The ALU data outputs (F_0, F_1, F_2, F_3) are routed to the RAM, Q Register inputs and the Y outputs under control of the I_6, I_7, I_8 control signal inputs. The MSB of the ALU is output as F_3 so the user can examine the sign-bit without enabling the three-state outputs. An open drain output, F = 0, is HIGH when $F_0 = F_1 = F_2 = F_3 = 0$ so the user can determine when the ALU output is zero by wire-ORing these outputs together.

Q REGISTER — The Q Register is a separate 4-bit file intended for multiplication and division routines and can also be used as an accumulator or holding register for other types of applications. It is driven from a 3-input multiplexer. In the no-shift mode, the multiplexer enters the ALU data into the Q Register. In either the shift-up or shift-down mode, the multiplexer selects the Q Register data appropriately shifted up or down. The Q shifter has two ports, Q_0 and Q_3, which operate comparably to the RAM shifter. They are controlled by the I_6, I_7, I_8 inputs.

The clock input of the IDT39C01 controls the RAM, Q Register and A and B data latches. When enabled, the data is clocked into the Q Register on the LOW-to-HIGH transition. When the clock is HIGH, the A and B latches are open and pass data that is present at the RAM outputs. When the clock is LOW, the latches are closed and retain the last data entered. When the clock is LOW and RAM EN is enabled, new data will be written into the RAM file defined by the B address field.

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ALU DESTINATION CONTROL(1)

Mnemonic	Microcode I8	I7	I6	Octal Code	RAM Function Shift	RAM Function Load	Q Register Function Shift	Q Register Function Load	Y Output	RAM Shifter RAM0	RAM Shifter RAM3	Q Shifter Q0	Q Shifter Q3
QREG	L	L	L	0	X	NONE	NONE	F → Q	F	X	X	X	X
NOP	L	L	H	1	X	NONE	X	NONE	F	X	X	X	X
RAMA	L	H	L	2	NONE	F → B	X	NONE	A	X	X	X	X
RAMF	L	H	H	3	NONE	F → B	X	NONE	F	X	X	X	X
RAMQD	H	L	L	4	DOWN	F/2 → B	DOWN	Q/2 → Q	F	F0	IN3	Q0	IN3
RAMD	H	L	H	5	DOWN	F/2 → B	X	NONE	F	F0	IN3	Q0	X
RAMQU	H	H	L	6	UP	2F → B	UP	2Q → Q	F	IN0	F3	IN0	Q3
RAMU	H	H	H	7	UP	2F → B	X	NONE	F	IN0	F3	X	Q3

NOTE:

2590 tbl 04

1. X = Don't care. Electrically, the shift pin is a TTL input internally connected to a three-state output which is in the high-impedance state.
   B = Register Addressed by B inputs.
   UP is toward MSB; DOWN is toward LSB.

SOURCE OPERAND AND ALU FUNCTION MATRIX(1)

Octal I5, 4, 3	ALU Function	I2, 1, 0 Octal 0	1	2	3	4	5	6	7
		ALU Source A, Q	A, B	0, Q	0, B	0, A	D, A	D, Q	D, 0
0	Cn = L R Plus S	A + Q	A + B	Q	B	A	D + A	D + Q	D
	Cn = H	A + Q + 1	A + B + 1	Q + 1	B + 1	A + 1	D + A + 1	D + Q + 1	D + 1
1	Cn = L S Minus R	Q − A − 1	B − A − 1	Q − 1	B − 1	A − 1	A − D − 1	Q − D − 1	−D − 1
	Cn = H	Q − A	B − A	Q	B	A	A − D	Q − D	−D
2	Cn = L R Minus S	A − Q − 1	A − B − 1	−Q − 1	−B − 1	−A − 1	D − A − 1	D − Q − 1	D − 1
	Cn = H	A − Q	A − B	−Q	−B	−A	D − A	D − Q	D
3	R OR S	A ∨ Q	A ∨ B	Q	B	A	D ∨ A	D ∨ Q	D
4	R AND S	A ∧ Q	A ∧ B	0	0	0	D ∧ A	D ∧ Q	0
5	$\overline{R}$ AND S	$\overline{A}$ ∧ Q	$\overline{A}$ ∧ B	Q	B	A	$\overline{D}$ ∧ A	$\overline{D}$ ∧ Q	0
6	R EX-OR S	A ∇ Q	A ∇ B	Q	B	A	D ∇ A	D ∇ Q	D
7	R EX-NOR S	$\overline{A \nabla Q}$	$\overline{A \nabla B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \nabla A}$	$\overline{D \nabla Q}$	$\overline{D}$

NOTE:

2590 tbl 05

1. + = Plus; − = Minus; ∧ = AND; ∇ = EX-OR; ∨ = OR.

ALU LOGIC MODE FUNCTIONS

Octal			
I5, 4, 3	I2, 1, 0	Group	Function
4	0	AND	A ∧ Q
4	1		A ∧ B
4	5		D ∧ A
4	6		D ∧ Q
3	0	OR	A ∨ Q
3	1		A ∨ B
3	5		D ∨ A
3	6		D ∨ Q
6	0	EX–OR	A ∇ Q
6	1		A ∇ B
6	5		D ∇ A
6	6		D ∇ Q
7	0	EX–NOR	$\overline{A \nabla Q}$
7	1		$\overline{A \nabla B}$
7	5		$\overline{D \nabla A}$
7	6		$\overline{D \nabla Q}$
7	2	INVERT	$\overline{Q}$
7	3		$\overline{B}$
7	4		$\overline{A}$
7	7		$\overline{D}$
6	2	PASS	Q
6	3		B
6	4		A
6	7		D
3	2	PASS	Q
3	3		B
3	4		A
3	7		D
4	2	"ZERO"	0
4	3		0
4	4		0
4	7		0
5	0	MASK	$\overline{A} \wedge Q$
5	1		$\overline{A} \wedge B$
5	5		$\overline{D} \wedge A$
5	6		$\overline{D} \wedge Q$

2590 tbl 06

ALU ARITHMETIC MODE FUNCTIONS

Octal		Cn = L		Cn = H	
I5, 4, 3	I2, 1, 0	Group	Function	Group	Function
0	0	ADD	A + Q	ADD plus one	A + Q + 1
0	1		A + B		A + B + 1
0	5		D + A		D + A + 1
0	6		D + Q		D + Q + 1
0	2	PASS	Q	Increment	Q + 1
0	3		B		B + 1
0	4		A		A + 1
0	7		D		D + 1
1	2	Decrement	Q – 1	PASS	Q
1	3		B – 1		B
1	4		A – 1		A
2	7		D – 1		D
2	2	1's Comp.	–Q – 1	2's Comp. (Negate)	–Q
2	3		–B – 1		–B
2	4		–A – 1		–A
1	7		–D – 1		–D
1	0	Subtract (1's Comp)	Q – A – 1	Subtract (2's Comp)	Q – A
1	1		B – A – 1		B – A
1	5		A – D – 1		A – D
1	6		Q – D – 1		Q – D
2	0		A – Q – 1		A – Q
2	1		A – B – 1		A – B
2	5		D – A – 1		D – A
2	6		D – Q – 1		D – Q

2590 tbl 07

DEFINITIONS(1)

$P_0 = R_0 + S_0$
$P_1 = R_1 + S_1$
$P_2 = R_2 + S_2$
$P_3 = R_3 + S_3$
$G_0 = R_0S_0$
$G_1 = R_1S_1$
$G_2 = R_2S_2$
$G_3 = R_3S_3$
$C_4 = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0 + P_3P_2P_1P_0C_n$
$C_3 = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$

NOTE:
1. + = OR

2590 tbl 08

LOGIC FUNCTIONS FOR $\overline{G}$, $\overline{P}$, C_{n+4} AND OVR (1)

I5, 4, 3	Function	$\overline{P}$	$\overline{G}$	C_{n+4}	OVR
0	R + S	$\overline{P_3P_2P_1P_0}$	$\overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$	C_4	$C_3 \nabla C_4$
1	S – R	Same as R + S equations, but substitute $\overline{R}_i$ for R_i in definitions			
2	R – S	Same as R + S equations, but substitute $\overline{S}_i$ for S_i in definitions			
3	R ∨ S	LOW	$P_3P_2P_1P_0$	$\overline{P_3P_2P_1P_0} + C_n$	$\overline{P_3P_2P_1P_0} + C_n$
4	R ∧ S	LOW	$\overline{G_3 + G_2 + G_1 + G_0}$	$G_3 + G_2 + G_1 + G_0 + C_n$	$G_3 + G_2 + G_1 + G_0 + C_n$
5	$\overline{R} \wedge S$	LOW	Same as R ∨ S equations, but substitute $\overline{R}_i$ for R_i in definitions		
6	R ∇ S	Same as $\overline{R} \vee \overline{S}$ equations, but substitute $\overline{R}_i$ for R_i in definitions			
7	$\overline{R \nabla S}$	$G_3 + G_2 + G_1 + G_0$	$G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1P_0$	$\overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1P_0 (G_0 + C_n)}$	(2)

NOTES:
1. + = OR.
2. $[\overline{P}_2 + \overline{G}_2\overline{P}_1 + \overline{G}_2\overline{G}_1\overline{P}_0 + \overline{G}_2\overline{G}_1\overline{G}_0C_n] \nabla [\overline{P}_3 + \overline{G}_3\overline{P}_2 + \overline{G}_3\overline{G}_2\overline{P}_1 + \overline{G}_3\overline{G}_2\overline{G}_1\overline{P}_0 + \overline{G}_3\overline{G}_2\overline{G}_1\overline{C}_n]$

2590 tbl 09

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{CC}	Power Supply Voltage	-0.5 to +7.0	-0.5 to +7.0	V
V_{TERM}	Terminal Voltage with Respect to Ground	–0.5 to V_{CC} +0.5	–0.5 to V_{CC} +0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	30	30	mA

NOTE: 2590 tbl 10

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE: 2590 tbl 26

1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS

Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions		Min.	Typ.(3)	Max.	Unit
I_{IH}	Input HIGH Current (All Inputs)	V_{CC} = Max. V_{IN} = V_{CC}		–	0.1	5	µA
I_{IL}	Input LOW Current (All Inputs)	V_{CC} = Max. V_{IN} = GND		–	–0.1	–5	µA
V_{OH}	Output High Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –1.0mA (MIL.)	2.4	4.3	–	V
			I_{OH} = –1.6mA (COM'L.)	2.4	4.3	–	
V_{OL}	Output Low Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA (MIL.)	–	0.3	0.5	V
			I_{OL} = 20mA (COM'L.)	–	0.3	0.5	
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level(1)		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level(1)		–	–	0.8	V
I_{OZ}	Output Leakage Current	V_{CC} = Max.	V_{OUT} = 0V	–	–0.1	–10	µA
			V_{OUT} = V_{CC} (Max.)	–	0.1	10	
I_{OS}	Output Short Circuit Current	V_{CC} = Max. V_{OUT} = 0V(2)		–30	–	–	mA

NOTES: 2590 tbl 11

1. These input levels provide zero noise immunity and should only be static tested in a noise-free environment.
2. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
3. V_{CC} = 5.0V at T_A +25°C.

DC ELECTRICAL CHARACTERISTICS (Cont'd.)

Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%
V_{LC} = 0.2V; V_{HC} = VCC –0.2V

Symbol	Parameter	Test Conditions[1]			Min.	Typ.[3]	Max.	Unit
I_{CCQH}	Quiescent Power Supply Current CP = H (CMOS Inputs)	V_{CC} = Max. $V_{HC} \le V_{IH}$, $V_{IL} \le V_{LC}$ f_{CP} = 0, CP = H			–	0.5	5.0	mA
I_{CCQL}	Quiescent Power Supply Current CP = L (CMOS Inputs)	V_{CC} = Max. $V_{HC} \le V_{IH}$, $V_{IL} \le V_{LC}$ f_{CP} = 0, CP = L			–	0.5	5.0	mA
I_{CCT}	Quiescent Input Power Supply[4] Current (per Input @ TTL High)	V_{CC} = Max., V_{IH} = 3.4V f_{CP} = 0			–	0.3	0.5	mA/ Input
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. $V_{HC} \le V_{IH}$, $V_{IL} \le V_{LC}$ Outputs Open, $\overline{OE}$ = L		MIL. COM'L.	– –	1.5 1.0	2.5 2.0	mA/ MHz
I_{CC}	Total Power Supply Current[5]	V_{CC} = Max.. Outputs Open, $\overline{OE}$ = L CP = 50 % Duty cycle $V_{HC} \le V_{IH}$, $V_{IL} \le V_{LC}$ 50% Data Duty Cycle	IDT39C01C f_{CP} = 10MHz	MIL. COM'L.	– –	– –	30 25	mA
			IDT39C01D f_{CP} = 15MHz	MIL. COM'L.	– –	– –	35 30	
			IDT39C01E f_{CP} = 17.5MHz	MIL. COM'L.	– –	– –	40 35	
		V_{CC} = Max.. Outputs Open, $\overline{OE}$ = L CP = 50 % Duty Cycle V_{IH} = 3.4V, V_{IL} = 0.4V 50% Data Duty Cycle	IDT39C01C f_{CP} = 10MHz	MIL. COM'L.	– –	– –	35 30	
			IDT39C01D f_{CP} = 15MHz	MIL. COM'L.	– –	– –	40 35	
			IDT39C01E f_{CP} = 17.5MHz	MIL. COM'L.	– –	– –	45 40	

2590 tbl 12

NOTES:
1. These input levels should only be static tested in a noise-free environment.
2. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
3. V_{CC} = 5.0V at T_A +25°C.
4. I_{CCT} is derived by measuring the total current with all the inputs tied together at 3.4V, subtracting out I_{CCQH}, then dividing by the total number of inputs.
5. Total Supply Current is the sum of the Quiescent current and the Dynamic current (at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:
   $I_{CC} = I_{CCQH} (C_{DH}) + I_{CCQL} (1 - C_{DH}) + I_{CCT} (N_T \times D_H) + I_{CCD} (f_{CP})$
   C_{DH} = Clock duty cycle high period
   D_H = Data duty cycle TTL high period (V_{IN} = 3.4V)
   N_T = Number of dynamic inputs driven at TTL levels
   f_{CP} = Clock input frequency

CMOS TESTING CONSIDERATIONS

. There are certain testing considerations which must be taken into account when testing high-speed CMOS devices in an automatic environment. These are:

1) Proper decoupling at the test head is necessary. Placement of the capacitor set and the value of capacitors used is critical in reducing the potential erroneous failures resulting from large Vcc current changes. Capacitor lead length must be short and as close to the DUT power pins as possible.
2) All input pins should be connected to a voltage potential during testing. If left floating, the device may begin to oscillate causing improper device operation and possible latchup.
3) Definition of input levels is very important. Since many inputs may change coincidentally, significant noise at the device pins may cause the V_{IL} and V_{IH} levels not to be met until the noise has settled. To allow for this testing/board induced noise, IDT recommends using $V_{IL} \le 0V$ and $V_{IH} \ge 3V$ for AC tests.
4) Device grounding is extremely important for proper device testing. The use of multi-layer performance boards with radial decoupling between power and ground planes is required. The ground plane must be sustained from the performance board to the DUT interface board. All unused interconnect pins must be properly connected to the ground pin. Heavy gauge stranded wire should be used for power wiring and twisted pairs are recommended to minimize inductance.

AC ELECTRICAL CHARACTERISTICS
IDT39C01C

(Military and Commercial Temperature Ranges)

The tables below specify the guaranteed performance of the IDT39C01C over the –55°C to +125°C and 0°C to +70°C temperature ranges. VCC is specified at 5V ± 10% for military temperature range and 5V ± 5% for commercial temperature range. All times are in nanoseconds and are measured at the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads.

CYCLE TIME AND CLOCK CHARACTERISTICS

	Mil.	Com'l.	Unit
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle)	32	31	ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	31	32	MHz
Minimum Clock LOW Time	15	15	ns
Minimum Clock HIGH Time	15	15	ns
Minimum Clock Period	32	31	ns

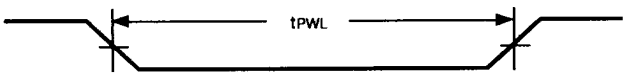
2590 tbl 13

COMBINATIONAL PROPAGATION DELAYS(1) C_L = 50pF

	To Output																
	Y		F_3		C_{n+4}		$\overline{G}, \overline{P}$		F = 0		OVR		RAM_0 RAM_3		Q_0 Q_3		
From Input	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Unit
A, B Address	48	40	48	40	48	40	44	37	48	40	48	40	48	40	–	–	ns
D	37	30	37	30	37	30	34	30	40	38	37	30	37	30	–	–	ns
C_n	25	22	25	22	21	20	–	–	28	25	25	22	28	25	–	–	ns
$I_{0,1,2}$	40	35	40	35	40	35	44	37	44	37	40	35	40	35	–	–	ns
$I_{3,4,5}$	40	35	40	35	40	35	40	35	40	38	40	35	40	35	–	–	ns
$I_{6,7,8}$	29	25	–	–	–	–	–	–	–	–	–	–	29	26	29	26	ns
A Bypass ALU (I = 2XX)	40	35	–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns
Clock ∫	40	35	40	35	40	35	40	35	40	35	40	35	40	35	33	28	ns

2590 tbl 14

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP INPUT)

CP: 

Input	Set-up Time Before H → L		Hold Time After H → L		Set-up Time Before L → H		Hold Time After L → H		Unit
	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	
A, B Source Address	15	15	2	1 (3)	30,15 + tPWL (4)		2	1	ns
B Destination Address	15	15	Do not change (2)				2	1	ns
D	– (1)	–	–	–	25	25	0	0	ns
C_n	–	–	–	–	20	20	0	0	ns
$I_{0,1,2}$	–	–	–	–	30	30	0	0	ns
$I_{3,4,5}$	–	–	–	–	30	30	0	0	ns
$I_{6,7,8}$	10	10	Do not change (2)				0	0	ns
$RAM_{0,3}$, $Q_{0,3}$	–	–	–	–	12	12	0	0	ns

2590 tbl 15

NOTES:
1. A dash indicates a propagation delay or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation.
3. Source addresses must be stable prior to the H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU and returned to the RAM. It includes all the time from stable A and B addresses to the clock L → H transition, regardless of when the H → L transition occurs.

OUTPUT ENABLE/DISABLE TIMES

(C_L = 5pF, measured to 0.5V change of V_{OUT} in nanoseconds)

Input	Output	Enable		Disable	
		Mil.	Com'l.	Mil.	Com'l.
$\overline{OE}$	Y	25	23	25	23

2590 tbl 16

5

AC ELECTRICAL CHARACTERISTICS
IDT39C01D

(Military and Commercial Temperature Ranges)

The tables below specify the guaranteed performance of the IDT39C01D over the –55°C to +125°C and 0°C to +70°C temperature ranges. VCC is specified at 5V ± 10% for military temperature range and 5V ± 5% for commercial temperature range. All times are in nanoseconds and are measured at the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads.

CYCLE TIME AND CLOCK CHARACTERISTICS

	Mil.	Com'l.	Unit
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle)	27	23	ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	37	43	MHz
Minimum Clock LOW Time	13	11	ns
Minimum Clock HIGH Time	13	11	ns
Minimum Clock Period	27	23	ns

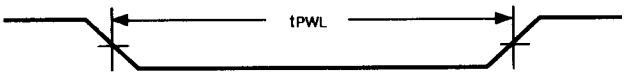
2590 tbl 17

COMBINATIONAL PROPAGATION DELAYS(1) C_L = 50pF

	To Output																
	Y		F_3		C_{n+4}		$\overline{G}$, $\overline{P}$		F = 0		OVR		RAM_0 RAM_3		Q_0 Q_3		
From Input	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Unit
A, B Address	33	30	33	30	33	30	33	30	33	30	33	30	33	30	–	–	ns
D	24	21	23	20	23	20	21	20	25	24	24	21	25	22	–	–	ns
C_n	18	17	17	16	14	14	–	–	19	18	17	16	19	18	–	–	ns
$I_{0,1,2}$	28	26	27	25	26	24	28	24	29	25	27	24	27	25	–	–	ns
$I_{3,4,5}$	27	26	27	24	26	24	26	24	27	26	26	24	27	26	–	–	ns
$I_{6,7,8}$	18	16	–	–	–	–	–	–	–	–	–	–	21	21	21	21	ns
A Bypass ALU (I = 2XX)	26	24	–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns
Clock ↓	27	24	26	23	26	23	25	23	27	24	26	24	27	24	20	19	ns

2590 tbl 18

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP INPUT)

CP: 

Input	Set-up Time Before H → L		Hold Time After H → L		Set-up Time Before L → H		Hold Time After L → H		Unit
	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	
A, B Source Address	11	10	0	0 (3)	24, 11 + tPWL (4)	21, 10 + tPWL (4)	2	1	ns
B Destination Address	11	10	Do not change (2)				2	1	ns
D	– (1)	–	–	–	16	16	0	0	ns
C_n	–	–	–	–	13	13	0	0	ns
$I_{0,1,2}$	–	–	–	–	19	19	0	0	ns
$I_{3,4,5}$	–	–	–	–	19	19	0	0	ns
$I_{6,7,8}$	7	7	Do not change (2)				0	0	ns
$RAM_{0,3}$, $Q_{0,3}$	–	–	–	–	9	9	0	0	ns

2590 tbl 19

NOTES:
1. A dash indicates a propagation delay or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation.
3. Source addresses must be stable prior to the H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU and returned to the RAM. It includes all the time from stable A and B addresses to the clock L → H transition, regardless of when the H → L transition occurs.

OUTPUT ENABLE/DISABLE TIMES

(C_L = 5pF, measured to 0.5V change of V_{OUT} in nanoseconds)

Input	Output	Enable		Disable	
		Mil.	Com'l.	Mil.	Com'l.
$\overline{OE}$	Y	16	14	18	16

2590 tbl 20

5

AC ELECTRICAL CHARACTERISTICS
IDT39C01E

(Military and Commercial Temperature Ranges)

The tables below specify the guaranteed performance of the IDT39C01E over the −55°C to +125°C and 0°C to +70°C temperature ranges. VCC is specified at 5V ± 10% for military temperature range and 5V ± 5% for commercial temperature range. All times are in nanoseconds and are measured at the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads.

CYCLE TIME AND CLOCK CHARACTERISTICS

	Mil.	Com'l.	Unit
Read-Modify-Write Cycle (from selection of A, B registers to end of cycle)	21	20	ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	46	50	MHz
Minimum Clock LOW Time	10	8	ns
Minimum Clock HIGH Time	10	8	ns
Minimum Clock Period	21	20	ns

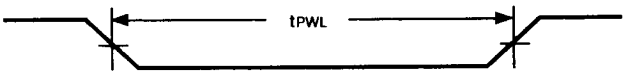
2590 tbl 21

COMBINATIONAL PROPAGATION DELAYS (1) C_L = 50pF

	To Output																
	Y		F_3		C_{n+4}		$\overline{G}$, $\overline{P}$		F = 0		OVR		RAM_0 RAM_3		Q_0 Q_3		
From Input	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Unit
A, B Address	26	22	26	22	26	22	26	21	29	25	26	22	26	22	–	–	ns
D	18	16	17	15	17	15	16	15	22	20	18	16	19	16	–	–	ns
Cn	13	13	13	12	10	10	–	–	16	15	13	12	14	13	–	–	ns
$I_{0,1,2}$	21	20	20	19	19	18	21	18	25	21	20	18	20	19	–	–	ns
$I_{3,4,5}$	20	20	20	18	19	18	19	18	23	23	19	18	20	20	–	–	ns
$I_{6,7,8}$	13	12	–	–	–	–	–	–	–	–	–	–	16	16	16	16	ns
A Bypass ALU (I = 2XX)	26	24	–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns
Clock ∫	20	18	19	17	19	17	19	17	25	22	19	18	20	18	15	15	ns

2590 tbl 22

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP INPUT)



Input	Set-up Time Before H → L		Hold Time After H → L		Set-up Time Before L → H		Hold Time After L → H		Unit
	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	
A, B Source Address	8	7	0	0 (3)	18, 8 + tPWL (4)	15, 7 + tPWL (4)	2	1	ns
B Destination Address	8	7	Do not change (2)				2	1	ns
D	– (1)	–	–	–	12	12	0	0	ns
C_n	–	–	–	–	10	10	0	0	ns
$I_{0,1,2}$	–	–	–	–	14	14	0	0	ns
$I_{3,4,5}$	–	–	–	–	14	14	0	0	ns
$I_{6,7,8}$	5	5	Do not change (2)				0	0	ns
$RAM_{0,3}$, $Q_{0,3}$	–	–	–	–	9	9	0	0	ns

2590 tbl 23

NOTES:
1. A dash indicates a propagation delay or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation.
3. Source addresses must be stable prior to the H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU and returned to the RAM. It includes all the time from stable A and B addresses to the clock L → H transition, regardless of when the H → L transition occurs.

OUTPUT ENABLE/DISABLE TIMES

(C_L = 5pF, measured to 0.5V change of V_{OUT} in nanoseconds)

Input	Output	Enable		Disable	
		Mil.	Com'l.	Mil.	Com'l.
$\overline{OE}$	Y	14	10	12	12

2590 tbl 24

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 4

2590 tbl 25

Test	Switch
Open Drain Disable Low Enable Low	Closed
All other Tests	Open

2590 tbl 27

INPUT/OUTPUT INTERFACE CIRCUIT

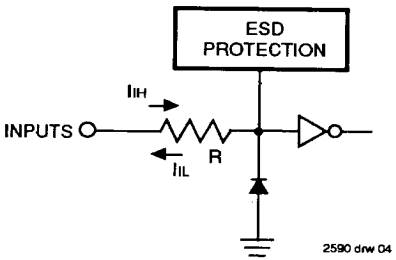


Figure 1. Input Structure (All Inputs)

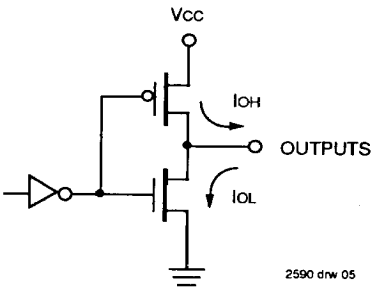


Figure 2. Outputs Structure (All Outputs Except F=0)

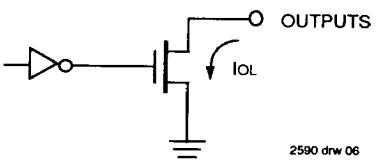
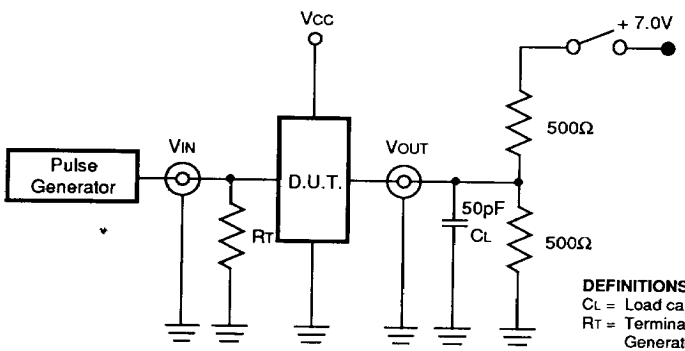


Figure 3. Output Structure (F=0 Only)

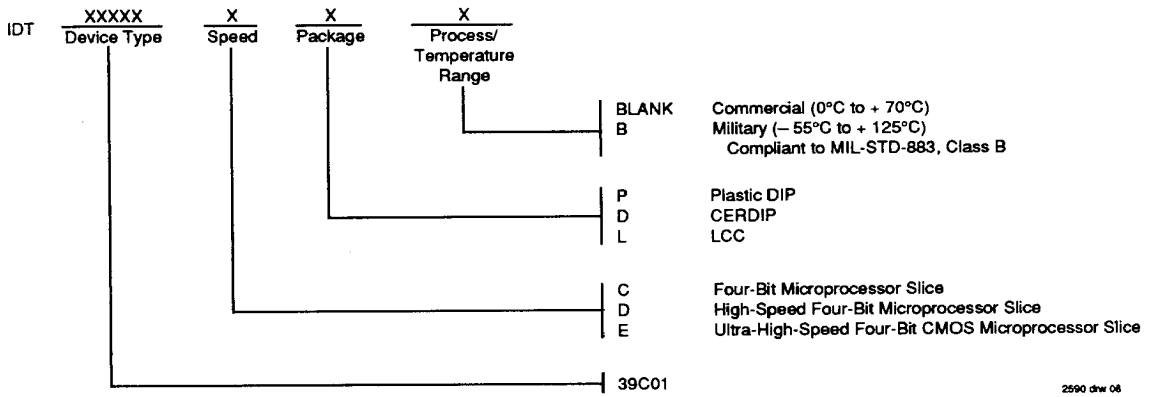
TEST CIRCUIT LOAD



DEFINITIONS:
C_L = Load capacitance: includes jig and probe capacitance
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator

Figure 4. Switching Test Circuits

ORDERING INFORMATION



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