



IDT39C02A

MICROSLICE™ PRODUCT

- Provides lookahead carries across any number of 4-bit microprocessor ALUs
- Very high speed and output drive over full temperature and voltage supply extremes
- 6ns typical propagation delay
- $I_{OL} = 32\text{mA}$ over full military temperature range
- CMOS power levels ($5\mu\text{W}$ typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than bipolar ($5\mu\text{W}$ max.)
- JEDEC standard pinout for DIP and LCC
- Military product compliant to MIL-STD-883, Class B

The IDT39C02A is a high-speed carry lookahead generator built using advanced CEMOS™, a dual metal CMOS technology. The IDT39C02A is generally used with an arithmetic logic unit to provide high-speed lookahead over larger word lengths.

The IDT39C02A is a pin-compatible, performance enhanced, functional replacement for all versions of the 2902.

The figure shows two pin diagrams for the L20-2 device. The left diagram is for the DIP/CERPACK/SOIC package (16 pins), and the right diagram is for the LCC package (20 pins). Both diagrams show the pin numbers, the pin names, and the internal connections to the device pins.

DIP/CERPACK/SOIC TOP VIEW

Pin	Signal
1	$\bar{G}_1$
2	P_1
3	$\bar{G}_0$
4	$\bar{P}_0$
5	$\bar{G}_3$
6	$\bar{P}_3$
7	$\bar{P}$
8	GND
9	C_{n+z}
10	$\bar{G}$
11	C_{n+y}
12	C_{n+x}
13	$E16-1$
14	$D16-1$
15	$\bar{P}_2$
16	V_{CC}

LCC TOP VIEW

Pin	Signal
1	G_1
2	P_1
3	NC
4	$\bar{G}_0$
5	$\bar{P}_0$
6	$\bar{G}_3$
7	$\bar{P}_3$
8	NC
9	$\bar{P}$
10	GND
11	C_{n+z}
12	$\bar{G}$
13	NC
14	C_{n+y}
15	C_{n+x}
16	C_n
17	$\bar{G}_2$
18	NC
19	V_{CC}
20	P_2

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MILITARY AND COMMERCIAL TEMPERATURE RANGES

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DSC-4059/-

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V _{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T _A	Operating Temperature	0 to +70	-55 to +125	°C
T _{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T _{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P _T	Power Dissipation	0.5	0.5	W
I _{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS ⁽¹⁾	MIN.	TYP. ⁽²⁾	MAX.	UNIT
V _{IH}	Input HIGH Level	Guaranteed Logic High Level	2.0	—	—	V
V _{IL}	Input LOW Level	Guaranteed Logic Low Level	—	—	0.8	V
I _{IH}	Input HIGH Current	V _{CC} = Max., V _{IN} = V _{CC}	—	—	5	μA
I _{IL}	Input LOW Current	V _{CC} = Max., V _{IN} = GND	—	—	-5	μA
I _{SC}	Short Circuit Current	V _{CC} = Max. ⁽³⁾	-60	-120	—	mA
V _{OH}	Output HIGH Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OH} = -300μA		V _{HC}	V
			I _{OH} = -12mA MIL.		V _{CC}	
			I _{OH} = -15mA COM'L.		—	
V _{OL}	Output LOW Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OL} = 300μA		GND	V
			I _{OL} = 32mA MIL.		0.3	
			I _{OL} = 48mA COM'L.		0.5	
I _{CCOC}	Quiescent Power Supply Current (CMOS Inputs)	V _{CC} = Max. V _{HC} ≤ V _{IN} ≤ V _{LC} f = 0	—	0.001	2.0	mA
I _{CCOT}	Quiescent Power Supply Current (TTL Inputs)	V _{CC} = Max. V _{IN} = 3.4V ⁽⁴⁾	—	0.5	2.5	mA
I _{CCD}	Dynamic Power Supply Current	V _{CC} = Max. Outputs Open One Input Toggling 50% Duty Cycle	V _{HC} ≤ V _{IN} ≤ V _{LC}		0.15	mA/MHz
I _{CC}	Total Power Supply Current ⁽⁵⁾	V _{CC} = Max. f = 10MHz Outputs Open 50% Duty Cycle One Input Toggling	V _{HC} ≤ V _{IN} ≤ V _{LC}		1.5	mA
			V _{IN} = 3.4V ⁽⁴⁾		2.0	
		All Inputs	V _{IN} = 3.4V ⁽⁴⁾		16.0	

NOTES:

- For conditions shown as max. or min. use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
- I_{CC} = I_{CCOC} + (I_{CCOT} × N_T) + (I_{CCD} × f × N) + D × N_D
N = Total number of inputs toggling.
f = Frequency in MHz.
D = Percent high duty cycle.
N_T = Number of TTL statically driven inputs (V_{IN} = 3.4V)
N_D = Number of TTL dynamically driven inputs (V_{IN} = 3.4V)

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
C_n	Carry Input
$\overline{G}_0, \overline{G}_1, \overline{G}_2, \overline{G}_3$	Carry Generate Inputs (Active LOW)
$\overline{P}_0, \overline{P}_1, \overline{P}_2, \overline{P}_3$	Carry Propagate Inputs (Active LOW)
$C_n + x - C_n + z$	Carry Outputs
G	Carry Generate Output (Active LOW)
P	Carry Propagate Output (Active LOW)

TRUTH TABLE ⁽¹⁾

C_n	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	$C_n + x$	$C_n + y$	$C_n + z$	G	P
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L											
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						L			
X	L	X	X	L						L			
H	X	L	X	L						L			
X	X	X	X	X	H	H					L		
X	X	X	H	X	H	X					L		
X	H	H	H	X	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	X	X	L	X					L		
X	L	X	X	L	X	L					L		
X	X	X	X	L	X	L					L		
H	X	L	X	L	X	L					L		
	X		X	X	X	X	H	H				H	
	X		X	H	H	X	H	X				H	
	X		H	X	H	X	H	X				H	
	H		X	X	X	X	L	X				L	
	X		X	X	L	L	X	L				L	
	L		X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					L

NOTE:

1. H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION ⁽¹⁾	TYPICAL	COMMERCIAL		MILITARY		UNIT
				MIN. ⁽²⁾	MAX.	MIN. ⁽²⁾	MAX.	
t _{PLH} t _{PHL}	Propagation Delay C _n to C _n + x C _n + y, C _n + z	C _L = 50pF R _L = 500Ω	6.0	3.0	14.0	3.0	16.5	ns
t _{PLH} t _{PHL}	Propagation Delay P ₀ , P ₁ , or P ₂ , to C _n + x, C _n + y, C _n + z		6.0	2.0	9.0	2.0	11.5	ns
t _{PLH} t _{PHL}	Propagation Delay G ₀ , G ₁ , or G ₂ to C _n + x, C _n + y, C _n + z		6.0	2.0	9.5	2.0	11.5	ns
t _{PLH} t _{PHL}	Propagation Delay P ₁ , P ₂ or P ₃ , to G		7.0	3.0	12.0	3.0	16.5	ns
t _{PLH} t _{PHL}	Propagation Delay G _n to G		7.5	3.0	12.0	3.0	16.5	ns
t _{PLH} t _{PHL}	Propagation Delay P _n to P		6.0	2.5	11.0	2.5	12.5	ns

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ORDERING INFORMATION

