Integrated Device Technology Inc

4-BIT CMOS MICROPROCESSOR SLICE

IDT39C03A
IDT39C03B

MICROSLICE™ PRODUCT

FEATURES:

- Fast
  - IDT39C03A matches 2903A speeds
  - IDT39C03B 20% speed upgrade
- Low-power CMOS
  - Commercial: 50mA (max.)
  - Military: 55mA (max.)
- Pin-compatible, performance enhanced functional replacement for the 2903A
- Cascadable to 8, 12, 16, etc. bits
- Expandable Register File
- On-chip Parity Generation and Sign Extension Logic
  - Provide parity across the entire ALU output and sign extension at any slice boundary
- On-chip Normalized Logic
  - Floating-point mantissa and exponent easily developed using single microcycle per shift
- On-chip multiplication and division logic
  - Executes unsigned and two's complement multiplication along with last cycle of two's complement multiplication
- Packaged in 48-pin plastic and ceramic DIPs and 52-pin LCC
- Military product available compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT39C03s are four-bit expandable CMOS microprocessor slices. While executing the identical functions associated with the high-speed IDT39C01 series of 4-bit slices, the IDT39C03s also provide additional enhancements for use in arithmetic-oriented processors.

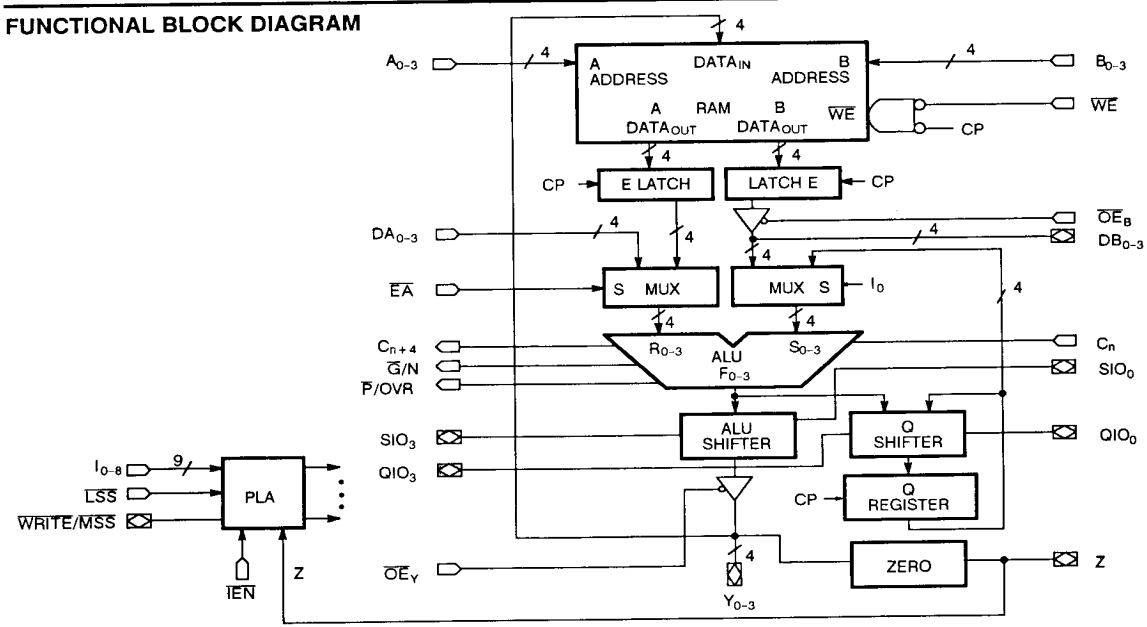
These extremely low-power yet high-speed microprocessors consist of a 16-word by 4-bit dual-port RAM, a multidirectional three-port architecture, 16 logic operation ALU and the necessary shifting, decoding and multiplexing logic. Compatible 2903A arithmetic and logic instructions, including the special multiplication, division and normalized instructions, are available on the IDT39C03s. Both are easily expandable in 4-bit increments.

Both devices are pin-compatible, functional-replacements for the 2903A. The fastest version, the IDT39C03B, is a 20% speed upgrade from the normal 2903A device. The IDT39C03A meets the 2903A speeds.

The IDT39C03s are fabricated using CEMOS™, a CMOS technology designed for high-performance and high-reliability.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to military temperature applications.

FUNCTIONAL BLOCK DIAGRAM



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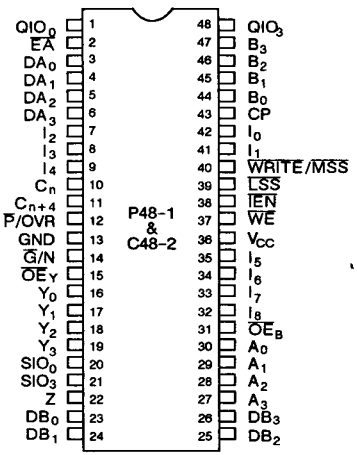
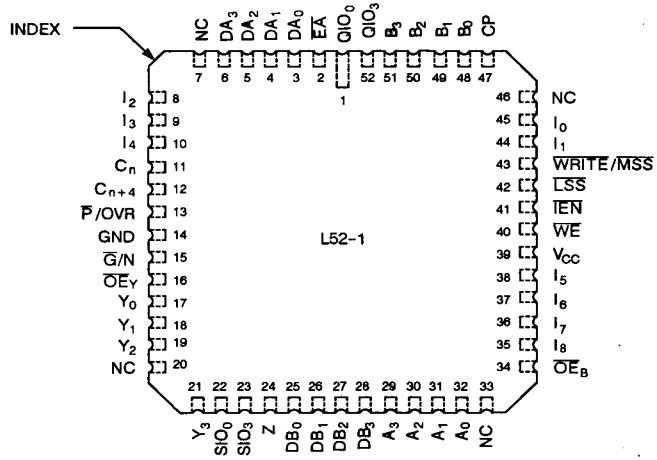
PIN CONFIGURATIONS



DIP
TOP VIEW



LCC
TOP VIEW

8

PIN DESCRIPTIONS

PIN NAME	I/O	DESCRIPTION
A_{0-3}	I	RAM A Address Inputs (TTL Input) – Four RAM address inputs which contain the address of the RAM word appearing at the RAM A output port.
B_{0-3}	I	RAM B Address Inputs (TTL Input) – Four RAM address inputs which contain the address of the RAM word appearing at the RAM B output port and into which new data is written when the $\overline{WE}$ input and the CP input are LOW.
$\overline{WE}$	I	Write Enable Input (TTL Input) – The RAM write enable input. If $\overline{WE}$ is LOW, data at the Y I/O port is written into the RAM when the CP input is LOW. When $\overline{WE}$ is HIGH, writing data into the RAM is inhibited.
DA_{0-3}	I	External Data Inputs (TTL Input) – A 4-bit external data input which can be selected as one of the IDT39C03 ALU operand sources; DA_0 is the least significant bit.
$\overline{EA}$	I	Control Input (TTL Input) – A control input which, when HIGH, selects DA_{0-3} as the ALU R operand and, when LOW, selects RAM output A as the ALU R operand and the DA_{0-3} output data.
DB_{0-3}	I/O	External Data Inputs/Outputs (Three-State Input/Output) – A four-bit external data input/output. Under control of the $\overline{OE}_B$ input, RAM output port B can be directly read on these lines, or input data on these lines can be selected as the ALU S operand.
$\overline{OE}_B$	I	Control Input (TTL Input) – A control input which, when LOW, enables RAM output B onto the DB_{0-3} lines and, when HIGH, disables the RAM output B tri-state buffers.
C_n	I	Carry-in Input (TTL Input) – The carry-in input to the IDT39C03 ALU.
I_{0-8}	I	Instruction Inputs (TTL Input) – The nine instruction inputs used to select the IDT39C03 operation to be performed.
$\overline{IEN}$	I	Instruction Enable Input (TTL Input) – The instruction enable input which, when LOW, allows the Q Register and the Sign Compare flip-flop to be written. When $\overline{IEN}$ is HIGH, the Q Register and Sign Compare flip-flop are in the hold mode. On the IDT39C03, $\overline{IEN}$ also controls $\overline{WRITE}$.
C_{n+4}	O	Carry-Out Output (TTL Input) – This output generally indicates the carry-out of the IDT39C03 ALU. Refer to Table 5 for an exact definition of this pin.
$\overline{G}$/N	O	Carry-Generate Output (TTL Output) – A multi-purpose pin which indicates the carry generate, $\overline{G}$ function, at the least significant and intermediate slices and generally indicates the sign N of the ALU result at the most significant slice. Refer to Table 5 for an exact definition of this pin.
$\overline{P}$/OVR	O	Carry Propagate Output (TTL Output) – A multi-purpose pin which indicates the carry propagate, $\overline{P}$, function at the least significant and intermediate slices and indicates the conventional two's complement overflow, OVR, signal at the most significant slice. Refer to Table 5 for an exact definition of this pin.
Z	I/O	Open-Drain I/O Pin (Open-Drain Input/Output) – An open-drain input/output pin which, when HIGH, generally indicates the outputs are all LOW. For some Special Functions, Z is used as an input pin. Refer to Table 5 for an exact definition of this pin.
SIO_0, SIO_3	I/O	Bidirectional Serial Shift I/Os for the ALU (Three-State Input/Output) – Bidirectional serial shift inputs/outputs for the ALU shifter. During a shift-up operation, SIO_0 is an input and SIO_3 an output. During a shift-down operation, SIO_3 is an input and SIO_0 is an output. Refer to Tables 3 and 4 for an exact definition of these pins.
QIO_0, QIO_3	I/O	Bidirectional Serial Shift I/Os for the Q Shifter (Three-State Input/Output) – Bidirectional serial shift inputs/outputs for the Q Shifter shifter which operate line SIO_0 and SIO_3. Refer to Tables 3 and 4 for an exact definition of these pins.
$\overline{LSS}$	I	Control Input (TTL Input) – An input pin which, when tied LOW, programs the chip to act as the least significant slice (LSS) of an IDT39C03 array and enables the $\overline{WRITE}$ output onto the $\overline{WRITE}/\overline{MSS}$ pin. When $\overline{LSS}$ is tied HIGH, the chip is programmed to operate as either an intermediate or most significant slice and the $\overline{WRITE}$ output buffer is disabled.
$\overline{WRITE}/\overline{MSS}$	I/O	Control Input (Three-State Input/Output) – When $\overline{LSS}$ is tied LOW, the $\overline{WRITE}$ output signal appears at this pin; the $\overline{WRITE}$ signal is LOW when an instruction which writes data into the RAM is being executed. When $\overline{LSS}$ is tied HIGH, $\overline{WRITE}/\overline{MSS}$ is an input pin; tying it HIGH programs the chip to operate as an intermediate slice (IS) and tying it LOW programs the chip to operate as the most significant slice (MSS).
Y_{0-3}	I/O	Data Inputs/Outputs (Three-State Input/Output) – Four data inputs/outputs of the IDT39C03. Under control of the $\overline{OE}_Y$ input, the ALU shifter output data can be enabled onto these lines, or these lines can be used as data inputs when external data is written directly into the RAM.
$\overline{OE}_Y$	I	Control Input (TTL Input) – A control input which, when LOW, enables the ALU shifter output data onto the Y_{0-3} lines and, when HIGH, disables the Y_{0-3} three-state output buffers.
CP	I	Clock Input (TTL Input) – The clock input to the IDT39C03. The Q Register and Sign Compare flip-flop are clocked on the LOW-to-HIGH transition of the CP signal. When enabled by $\overline{WE}$, data is written in the RAM when CP is LOW.

ARCHITECTURE OF THE IDT39C03

The IDT39C03s are high-performance, cascadable, 4-bit microprocessor slices used in CPUs, peripheral controllers, microprogrammable machines and in a number of other applications. The functional blocks consist of the following:

- 16-word-by-4-bit dual-port RAM
- high-speed ALU and shifter
- Q register with shifter input
- 9-bit instruction decoder

DUAL-PORT RAM

Both the A and B ports of the dual-port RAM can be addressed and read simultaneously at the respective RAM A and B output ports. If both ports address the same memory location, identical data will be read from both the A and B port. The latches at the RAM output ports are transparent when the clock input, CP, is HIGH and holds the RAM output data when CP is LOW. RAM data is read at the DB (I/O) port under control of the $\overline{OE}_B$ three-state output enable.

External data can be written directly into the RAM from the Y I/O port, or the ALU shifter output data can be enabled onto the Y I/O port and entered into the RAM. Data is written into the RAM at the B address when the write enable input, $\overline{WE}$, is LOW and the clock input, CP, is LOW.

ALU

The IDT39C03s perform seven arithmetic operations and nine logic operations on two 4-bit operands. Various pairs of ALU source operands are easily selected via the ALU multiplexer inputs. The $\overline{EA}$ input selects either the DA external data input or RAM output port A for use as one ALU operand. The $\overline{OE}_B$ and I_0 inputs select RAM output port B, DB external data input or the Q register content for use as the second ALU source operand. During certain ALU operations, zeros are forced at the ALU operand inputs. Thus, the IDT39C03s are capable of operating on data from two external sources, from an internal and external source, or from two internal sources. Table 1 indicates all the possible pairs of ALU source operands as a function of the $\overline{EA}$, $\overline{OE}_B$ and I_0 inputs.

With instruction bits I_4, I_3, I_2, I_1 and I_0 LOW, the IDT39C03s execute special functions which have been defined in Table 4. When the IDT39C03s execute instructions other than the nine special instructions, the ALU operation is defined by instruction bits I_4, I_3, I_2, and I_1. Table 2 defines the ALU operation as a function of these four instruction bits.

Cascading the IDT39C03s, in either the carry lookahead or ripple carry approach, is very simple. In a cascaded configuration, each slice must be properly programmed to Most Significant Slice (MSS), Intermediate Slice (IS) or Least Significant Slice (LSS). The IDT39C03s incorporate the carry generate ($\overline{G}$) and carry propagate ($\overline{P}$) signals necessary for cascading.

TABLE 1.
ALU OPERAND SOURCES (1)

$\overline{EA}$	I_0	$\overline{OE}$	ALU OPERAND R	ALU OPERAND S
L	L	L	RAM Output A	RAM Output B
L	L	H	RAM Output A	DB_{0-3}
L	H	X	RAM Output A	Q Register
H	L	L	DA_{0-3}	RAM Output B
H	L	H	DA_{0-3}	DB_{0-3}
H	H	X	DA_{0-3}	Q Register

NOTE:
1. L = LOW, H = HIGH, X = Don't Care

TABLE 2.
IDT39C03 ALU FUNCTIONS (1)

I_4	I_3	I_2	I_1	HEX CODE	ALU FUNCTIONS
L	L	L	L	0	I_0 = L: Special Functions; I_0 = H: F_i = HIGH
L	L	L	H	1	F = S Minus R Minus 1 Plus C_n
L	L	H	L	2	F = R Minus S Minus 1 Plus C_n
L	L	H	H	3	F = R Plus S Plus C_n
L	H	L	L	4	F = S Plus C_n
L	H	L	H	5	F = $\overline{S}$ Plus C_n
L	H	H	L	6	F = R Plus C_n
L	H	H	H	7	F = $\overline{R}$ Plus C_n
H	L	L	L	8	F_i = LOW
H	L	L	H	9	F_i = $\overline{R}_i$ AND S_i
H	L	H	L	A	F_i = R_i EXCLUSIVE NOR S_i
H	L	H	H	B	F_i = R_i EXCLUSIVE OR S_i
H	H	L	L	C	F_i = R_i AND S_i
H	H	L	H	D	F_i = R_i NOR S_i
H	H	H	L	E	F_i = R_i NAND S_i
H	H	H	H	F	F_i = R_i OR S_i

NOTE:
1. L = LOW, H = HIGH, i = 0 to 3

Also generated is a carry-out signal, C_{n+4}, which is generally available as an output of each slice. Both the carry-in (C_n) and carry-out (C_{n+4}) signals are active HIGH. The ALU generates two other status outputs. These are negative, N, and overflow, OVR. The N output is generally the most significant (sign) bit of the ALU output and can be used to determine positive or negative results. The OVR output indicates that the arithmetic operation being performed exceeds the available two's complement number range. The N and OVR signals are available as outputs of the most significant slice. Thus, the multipurpose $\overline{G}$/N and $\overline{P}$/OVR outputs indicate $\overline{G}$ and $\overline{P}$ at the least significant and intermediate slices, and sign and overflow at the most significant slice. Refer to Table 5 for the exact definition of these four signals.

ALU SHIFTER

Under instruction control, the ALU shifter passes the ALU output (F) non-shifted, shifts it up one bit position (2F) or shifts it down one position (F/2). Both arithmetic and logical shift operations are possible. The arithmetic shift operation shifts data around the most significant (sign) bit position of the MSS and a logical shift operation shifts data through this bit position (see Figure 1). SIO_0 and SIO_3 are bidirectional serial shift inputs/outputs. During a shift-up operation SIO_3 is generally a serial shift input and SIO_0 a serial shift output. For exact definition of the SIO_0 and SIO_3 operation, refer to Tables 3 and 4.

Also provided in the ALU shifter is sign extension at the slice boundaries. Under instruction control, the SIO_0 (sign) input can be extended through Y_0, Y_1, Y_2, Y_3, and propagated to the SIO_3 output.

Providing ALU error detection, the IDT39C03s ALU shifter contains a cascadable, five-bit parity generator/checker. Parity for the F_0, F_1, F_2, F_3, ALU outputs and SIO_3 input is generated and, under instruction control, is made available at the SIO_0 output.

The operation of the ALU shifter is defined by the instruction inputs. Specified in Table 4 are the special functions and the operations the ALU shifter performs. When the IDT39C03s execute instructions other than special functions,the ALU shifter operation is

8

determined by instruction bits I_8, I_7, I_6 and I_5. How these four bits operate with the ALU shifter is defined in Table 3.

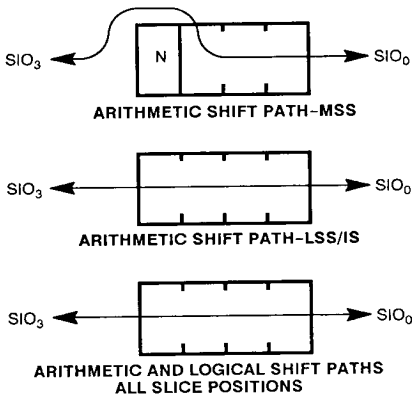


Figure 1.

Q REGISTER

The Q Register is an auxiliary 4-bit register which is clocked on the LOW-to-HIGH transition of the CP input. It is intended primarily for use in multiplication and division operations; however, it can also be used as an accumulator or holding register for some applications. The F output of the ALU can be loaded into the Q Register and/or the Q Register can be selected as the source for the ALU S operand. The shifter at the input to the Q Register can shift the Q Register contents up one bit position (2Q) or down one bit position (Q/2). Only logical shifts are performed. Both QIO_0 and QIO_3 are bidirectional shift serial inputs/outputs. During a Q Register shift-up operation, QIO_0 is a serial shift input and QIO_3 is a serial shift output. During a shift-down operation, QIO_3 is a serial shift input and QIO_0 is a serial shift output.

The IDT39C03s provide the capability of double-length arithmetic and logical shifting. To perform the double-length shift, QIO_3 of the MSS is connected to SIO_0 of the LSB and executing an instruction which shifts both the ALU output and the Q Register.

The instruction inputs also control the Q Register and shifter, as shown in Table 4. When executing instructions other than the special functions, the Q Register and shifter operation is controlled by instruction bits I_8, I_7, I_6 and I_5, as shown in Table 3.

OUTPUT BUFFERS

Both the DB and Y ports are bidirectional I/O ports driven by three-state output buffers with external output enable controls. The Y output buffers are enabled when the $\overline{OE}_Y$ is LOW and are in the High Z state when $\overline{OE}_Y$ is HIGH. The DB output buffers are enabled when the $\overline{OE}_B$ input is LOW. The zero, Z pin, is an open drain I/O that can be wire-Ored between slices. As an output it can be used as a zero detect status flag and generally indicates that the Y_{0-3} pins are all LOW. Table 5 defines the exact signal functions.

INSTRUCTION DECODER

The Instruction Decoder generates the required internal control signals relative to the nine instruction inputs, I_{0-8}, the Instruction Enable input, $\overline{IEN}$, the $\overline{LSS}$ input and the $\overline{WRITE}/\overline{MSS}$ input/output.

When an instruction which writes data into the RAM is being performed, the $\overline{WRITE}$ output is LOW. Reference Tables 3 and 4 for proper pin operation. When $\overline{IEN}$ is HIGH, the $\overline{WRITE}$ output is forced HIGH and the Q Register and Sign Compare Flip-Flop contents are preserved. When $\overline{IEN}$ is LOW, the $\overline{WRITE}$ output is enabled and the Q Register and Sign Compare Flip-Flop can be written according to the IDT39C03s instruction. The Sign Compare Flip-Flop is an on-chip flip-flop which is used during a divide operation. See Figure 2.

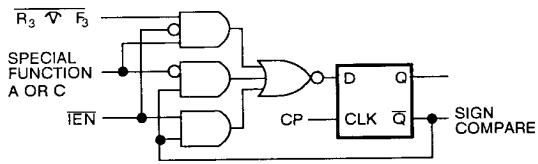


Figure 2. Sign Compare Flip-Flop

SLICE POSITION PROGRAMMING

When the $\overline{LSS}$ input is LOW, the device becomes the Least Significant Slice and enables the $\overline{WRITE}$ output signal onto the $\overline{WRITE}/\overline{MSS}$ bidirectional I/O pin. When the $\overline{LSS}$ input is HIGH, the $\overline{WRITE}/\overline{MSS}$ pin becomes an input which when HIGH programs the slice to operate as an Intermediate Slice (IS). Connecting it LOW programs the slice to operate as a Most Significant Slice (MSS). The $\overline{WRITE}/\overline{MSS}$ pin must be tied HIGH via a pull-up resistor. $\overline{WRITE}/\overline{MSS}$ and $\overline{LSS}$ should not be connected together.

SPECIAL FUNCTIONS

Nine special functions are provided on the IDT39C03s which make possible the implementation of the following operations:

- Single and Double Length Normalization
- Two's Complement Division
- Unsigned and Two's Complement Multiplication
- Conversion Between Two's Complement and Sign/Magnitude Representation
- Incrementation by One or Two

Adjusting a single-precision or double-precision floating-point number in order to bring its mantissa within a specified range can be performed using the single-length and double-length normalization operations. These special functions can be used to perform a two's complement, non-restoring divide operation. They provide single and double-precision divide operations and can be performed in "n" clock cycles (where "n" is the number of bits in the quotient). The unsigned multiply special function and the two two's complement multiply special functions can be used to multiply two n-bit, unsigned or two's complement numbers, respectively, in "n" clock cycles. During the last cycle of the two's complement multiplication, a conditional subtraction (rather than addition) is performed due to the fact that the sign bit of the multiplier carries negative weight.

The sign/magnitude-two's complement special function can be used to convert number representation systems. A number expressed in sign/magnitude representation can be converted to the two's complement representation, and vice-versa, in one clock cycle.

Incrementing an unsigned or two's complement number by one or two is easily accomplished using the increment by one or two special function.

TABLE 3. ALU DESTINATION CONTROL FOR I_0 OR I_1 OR I_2 OR I_3 = HIGH, $\overline{IEN}$ = LOW

I_8	I_7	I_6	I_5	HEX CODE	ALU SHIFTER FUNCTION	SIO_3		Y_3		Y_2		Y_1	Y_0	SIO_0	$\overline{WRITE}$	Q REG & SHIFTER FUNCTION	QIO_3	QIO_0
						MOST SIG. SLICE	OTHER SLICES	MOST SIG. SLICE	OTHER SLICES	MOST SIG. SLICE	OTHER SLICES							
L	L	L	L	0	Arith. F/2 → Y	Input	Input	F_3	SIO_3	SIO_3	F_3	F_2	F_1	F_0	L	Hold	Z	Z
L	L	L	H	1	Log. F/2 → Y	Input	Input	SIO_3	SIO_3	F_3	F_3	F_2	F_1	F_0	L	Hold	Z	Z
L	L	H	L	2	Arith. F/2 → Y	Input	Input	F_3	SIO_3	SIO_3	F_3	F_2	F_1	F_0	L	Log. Q/2 → Q	Input	Q_0
L	L	H	H	3	Log. F/2 → Y	Input	Input	SIO_3	SIO_3	F_3	F_3	F_2	F_1	F_0	L	Log. Q/2 → Q	Input	Q_0
L	H	L	L	4	F → Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	L	Hold	Z	Z
L	H	L	H	5	F → Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	H	Log. Q/2 → Q	Input	Q_0
L	H	H	L	6	F → Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	H	F → Q	Z	Z
L	H	H	H	7	F → Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	L	F → Q	Z	Z
H	L	L	L	8	Arith. 2F → Y	F_2	F_3	F_3	F_2	F_1	F_1	F_0	SIO_0	Input	L	Hold	Z	Z
H	L	L	H	9	Log. 2F → Y	F_3	F_3	F_2	F_2	F_1	F_1	F_0	SIO_0	Input	L	Hold	Z	Z
H	L	H	L	A	Arith. 2F → Y	F_2	F_3	F_3	F_2	F_1	F_1	F_0	SIO_0	Input	L	Log. 2Q → Q	Q_3	Input
H	L	H	H	B	Log. 2F → Y	F_3	F_3	F_2	F_2	F_1	F_1	F_0	SIO_0	Input	L	Log. 2Q → Q	Q_3	Input
H	H	L	L	C	F → Y	F_3	F_3	F_3	F_3	F_2	F_2	F_1	F_0	Z	H	Hold	Z	Z
H	H	L	H	D	F → Y	F_3	F_3	F_3	F_3	F_2	F_2	F_1	F_0	Z	H	Log. 2Q → Q	Q_3	Input
H	H	H	L	E	SIO_0 → Y_0, Y_1, Y_2, Y_3	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	Input	L	Hold	Z	Z
H	H	H	H	F	F → Y	F_3	F_3	F_3	F_3	F_2	F_2	F_1	F_0	Z	L	Hold	Z	Z

NOTE:
1. Parity = $F_3 \oplus F_2 \oplus F_1 \oplus F_0 \oplus SIO_3$. L = LOW Z = High Impedance $\oplus$ = Exclusive OR, H = HIGH

8

TABLE 4. SPECIAL FUNCTIONS FOR $I_4 = I_3 = I_2 = I_1 = I_0$ LOW [4]

(HEX) $I_8 I_7 I_6 I_5$	SPECIAL FUNCTION	ALU FUNCTION	ALU SHIFTER FUNCTION	SIO_3		SIO_0	Q REGISTER & SHIFTER FUNCTION	QIO_3	QIO_0	$\overline{WRITE}$
				MSS	OTHER SLICES					
0	Unsigned Multiply	$F = S + C_n$ if $Z = L$ $F = R + S + C_n$ if $Z = H$	Log F/2 → Y [1]	Z	Input	F_0	Log Q/2 → Q	Input	Q_0	L
1	(5)									
2	Two's Complement Multiply	$F = S + C_n$ if $Z = L$ $F = R + S + C_n$ if $Z = H$	Log F/2 → Y [2]	Z	Input	F_0	Log Q/2 → Q	Input	Q_0	L
3	(5)									
4	Increment by One or Two	$F = S + 1 + C_n$	F → Y	Input	Input	Parity	Hold	Z	Z	L
5	Sign/Magnitude Two's Complement	$F = \overline{S} + C_n$ if $Z = L$ $F = \overline{S} + C_n$ if $Z = H$	F → Y [3]	Input	Input	Parity	Hold	Z	Z	L
6	Two's Complement Multiply Last Cycle	$F = S + C_n$ if $Z = L$ $F = S - R - 1 + C_n$ if $Z = H$	Log F/2 → Y [2]	Z	Input	$\overline{F_0}$	Log Q/2 → Q	Input	Q_0	L
7	(5)									
8	Single Length Normalize	$F = S + C_n$	F → Y	F_3	F_3	Z	Log 2Q → Q	Q_3	Input	L
9	(5)									
A	Double Length Normalize and First Divide Op	$F = S + C_n$	Log 2F → Y	$R_3 \oplus F_3$	F_3	Input	Log 2Q → Q	Q_3	Input	L
B	(5)									
C	Two's Complement Divide	$F = S + R + C_n$ if $Z = L$ $F = S - R - 1 + C_n$ if $Z = H$	Log 2F → Y	$\overline{R_3 \oplus F_3}$	F_3	Input	Log 2Q → Q	Q_3	Input	L
D	(5)									
E	Two's Complement Divide Correction and Remainder	$F = S + R + C_n$ if $Z = L$ $F = S - R - 1 + C_n$ if $Z = H$	F → Y	F_3	F_3	Z	Log 2Q → Q	Q_3	Input	L
F	(5)									

NOTES:

1. At the most significant slice only, the C_{n+4} signal is internally gated to the Y_3 output.
2. At the most significant slice only, $F_3 \oplus$ OVR is internally gated to the Y_3 output.
3. At the most significant slice only, $S_3 \oplus F_3$ is generated the Y_3 output.
4. The Q Register cannot be used explicitly as an operand for any Special Functions. It is defined implicitly within the functions.
5. Not Valid
6. L = LOW, H = HIGH, X = Don't Care, Z = High Impedance, $\oplus$ = Exclusive OR, PARITY = $SIO_3 \oplus F_3 \oplus F_2 \oplus F_1 \oplus F_0$

TABLE 5. IDT39C03A STATUS OUTPUTS

(HEX) I_{8-5}	(HEX) I_{4-1}	I_0	G_i (i = 0 to 3)	P_i (i = 0 to 3)	C_{n+4}	$\overline{F}$/OVR		$\overline{G}$/N		Z ($\overline{OEY}$ = L)		
						MOST SIG. SLICE	OTHER SLICES	MOST SIG. SLICE	OTHER SLICES	MOST SIG. SLICE	INTER-MEDIATE SLICE	LEAST SIG. SLICE
X	0	H	0	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	1	X	$\overline{R}_i \wedge S_i$	$\overline{R}_i \vee S_i$	G V PC_n	$C_{n+3} \veebar C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	2	X	$R_i \wedge \overline{S}_i$	$R_i \vee \overline{S}_i$	G V PC_n	$C_{n+3} \veebar C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	3	X	$R_i \wedge S_i$	$R_i \vee S_i$	G V PC_n	$C_{n+3} \veebar C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	4	X	0	S_i	G V PC_n	$C_{n+3} \veebar C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	5	X	0	$\overline{S}_i$	G V PC_n	$C_{n+3} \veebar C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	6	X	0	R_i	G V PC_n	$C_{n+3} \veebar C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	7	X	0	$\overline{R}_i$	G V PC_n	$C_{n+3} \veebar C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	8	X	0	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	9	X	$\overline{R}_i \wedge S_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	A	X	$R_i \wedge S_i$	$R_i \vee S_i$	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	B	X	$\overline{R}_i \wedge S_i$	$R_i \vee S_i$	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	C	X	$R_i \wedge S_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	D	X	$\overline{R}_i \wedge \overline{S}_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	E	X	$R_i \wedge \overline{S}_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	F	X	$\overline{R}_i \wedge \overline{S}_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
0	0	L	0 if Z = L $R_i \wedge S_i$ if Z = H	S_i if Z = L $R_i \vee S_i$ if Z = H	G V PC_n	$C_{n+3} \veebar C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Input	Input	Q_0
1	0	L	(Note 6)	–	–	–	–	–	–	–	–	–
1	8	L	(Note 6)	–	–	–	–	–	–	–	–	–
2	0	L	0 if Z = L $R_i \wedge S_i$ if Z = H	S_i if Z = L $R_i \vee S_i$ if Z = H	G V PC_n	$C_{n+3} \veebar C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Input	Input	Q_0
3	0	L	(Note 6)	–	–	–	–	–	–	–	–	–
4	0	L	(Note 1)	(Note 2)	G V PC_n	$C_{n+3} \veebar C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
5	0	L	0	S_i if Z = L S_i if Z = H	G V PC_n	$C_{n+3} \veebar C_{n+4}$	$\overline{P}$	F_3 if Z = L $F_3 \veebar S_3$ if Z = H	$\overline{G}$	S_3	Input	Input
6	0	L	0 if Z = L $\overline{R}_i \wedge S_i$ if Z = H	S_i if Z = L $\overline{R}_i \vee S_i$ if Z = H	G V PC_n	$C_{n+3} \veebar C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Input	Input	Q_0
7	0	L	(Note 6)	–	–	–	–	–	–	–	–	–
8	0	L	0	S_i	(Note 3)	$Q_2 \veebar Q_1$	$\overline{P}$	Q_3	$\overline{G}$	$\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$	$\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$	$\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$
9	0	L	(Note 6)	–	–	–	–	–	–	–	–	–
9	8	L	(Note 6)	–	–	–	–	–	–	–	–	–
A	0	L	0	S_i	(Note 4)	$F_2 \veebar F_1$	$\overline{P}$	F_3	$\overline{G}$	(Note 5)	(Note 5)	(Note 5)
B	0	L	(Note 6)	–	–	–	–	–	–	–	–	–
C	0	L	$R_i \wedge S_i$ if Z = L $\overline{R}_i \wedge S_i$ if Z = H	$R_i \vee S_i$ if Z = L $\overline{R}_i \vee S_i$ if Z = H	G V PC_n	$C_{n+3} \veebar C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Sign Compare FF Output	Input	Input
D	0	L	(Note 6)	–	–	–	–	–	–	–	–	–
E	0	L	$R_i \wedge S_i$ if Z = L $\overline{R}_i \wedge S_i$ Z = H	$R_i \vee S_i$ if Z = L $\overline{R}_i \vee S_i$ Z = H	G V PC_n	$C_{n+3} \veebar C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Sign Compare FF Output	Input	Input
F	0	L	(Note 6)	–	–	–	–	–	–	–	–	–

Continued next page

NOTES:

1. If $\overline{LSS}$ is LOW, $G_0 = S_0$ and $G_{1,2,3} = 0$. If $\overline{LSS}$ is HIGH, $G_{0,1,2,3} = 0$.
2. If $\overline{LSS}$ is LOW, $P_0 = 1$ and $P_{1,2,3} = S_{1,2,3}$. If $\overline{LSS}$ is HIGH, $P_i = S_i$.
3. At the most significant slice, $C_{n+4} = Q_3 \veebar Q_2$. At other slices $C_{n+4} = G \vee PC_n$.
4. At the most significant slice, $C_{n+4} = F_3 \veebar F_2$. At other slices $C_{n+4} = G \vee PC_n$.
5. $Z = \overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3\,\overline{F}_0\,\overline{F}_1\,\overline{F}_2\,\overline{F}_3$.

8

NOTES (Cont'd.):

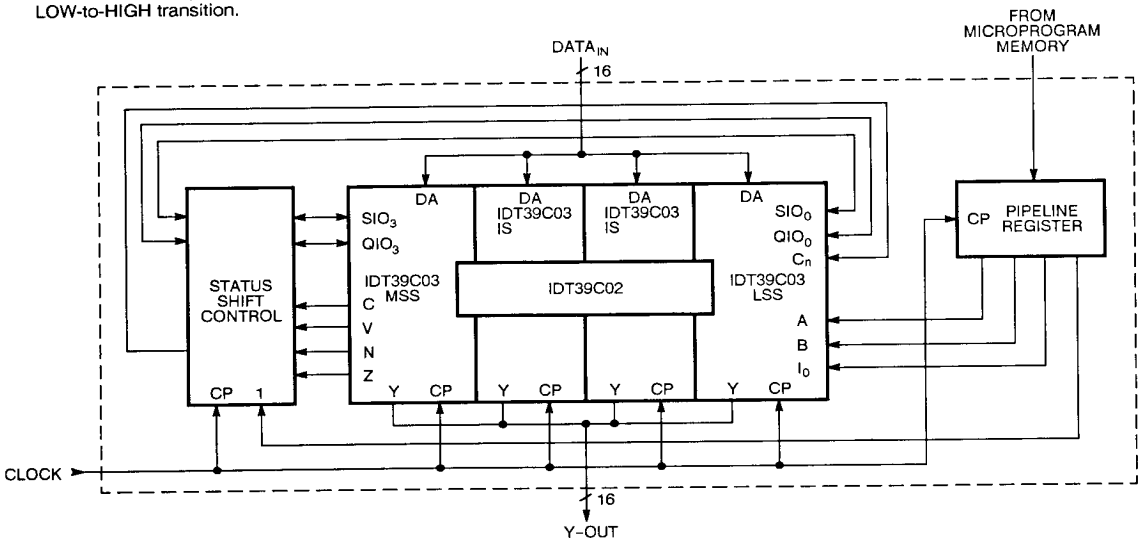
6. Not Valid.
7. L = LOW = 0, H = HIGH = 1, V = OR, Λ = AND, ∇= EXCLUSIVE OR, $P = P_3P_2P_1P_0$, $G = G_3 \vee G_2P_3 \vee G_1P_2P_3 \vee G_0P_1P_2P_3$, $C_{n+3} = G_2 \vee G_1P_2 \vee G_0P_1P_2 \vee C_nP_0P_1P_2$

Shown below is a circuit diagram for a 16-bit application using four IDT39C03s, one IDT39C02 and a status shift control device. This application has four key speed paths which are defined below:

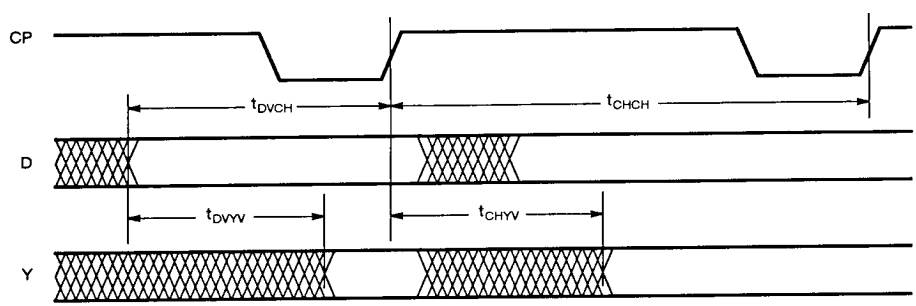
1. **Microcycle Time (t_{CHCH})**
   Minimum elapsed time between a LOW-to-HIGH clock transition and the next LOW-to-HIGH clock transition.
2. **Data Set-up Time (t_{DVCH})**
   Minimum allowable time between valid data on the D inputs and the clock LOW-to-HIGH transition.
3. **D to Y (t_{TDVYV})**
   Maximum time needed to receive valid Y output data after the D inputs are valid.
4. **CP to Y (t_{TCHYV})**
   Maximum time required to obtain valid Y outputs after a clock LOW-to-HIGH transition.

TIME IN NANOSECONDS OVER COMMERCIAL OPERATING RANGE

CYCLE	t_{CHYV}		t_{DVCH}		t_{DVYV}		t_{CHYV}	
	A	B	A	B	A	B	A	B
Logic	99	79	79	63	59	47	81	65
Logic Rotate	118	94	99	79	79	63	98	78
Arithmetic	130	104	109	87	91	73	112	90
Multiply	152	122	113	90	95	76	135	108
Divide	139	111	113	90	95	76	121	97



TIMING WAVEFORM FOR DATA$_{IN}$, CLOCK AND Y OUTPUT



ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	30	30	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:

1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level (4)		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level (4)		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		–	0.1	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		–	-0.1	-5	µA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	V
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	V
			I_{OL} = 20mA MIL.	–	0.3	0.5	
			I_{OL} = 24mA COM'L.	–	0.3	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0V	–	-0.1	-10	µA
			V_O = V_{CC} (Max.)	–	0.1	10	
I_{OS}	Output Short Circuit Current	V_{CC} = Min., V_{OUT} = 0V (3)		-30	–	–	mA

NOTES:

1. For conditions shown as max. or min. use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. These input levels provide zero noise immunity and should only be static tested in a noise-free environment.

8

DC ELECTRICAL CHARACTERISTICS (Cont'd)

T_A = 0°C to +70°C V_{CC} = 5.0V ±5% (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ±10% (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQH}	Quiescent Power Supply Current CP = H (CMOS Inputs)	V_{CC} = Max. $V_{HC} \leq V_{IN}$, $V_{IN} \leq V_{LC}$ f_{CP} = 0, CP = H		–	5	15	mA
I_{CCQL}	Quiescent Power Supply Current CP = L (CMOS Inputs)	V_{CC} = Max. $V_{HC} \leq V_{IN}$, $V_{IN} \leq V_{LC}$ f_{CP} = 0, CP = L		–	5	15	mA
I_{CCT}	Quiescent Input Power Supply[5] Current (per Input @ TTL High)	V_{CC} = Max. V_{IN} = 3.4V, f_{CP} = 0		–	0.25	0.5	mA/ Input
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. $V_{HC} \leq V_{IN}$, $V_{IN} \leq V_{LC}$ Outputs Open, $\overline{OE}$ = L	MIL.	–	0.5	2.0	mA/ MHz
			COM'L.	–	0.5	1.5	
I_{CC}	Total Power Supply Current[6]	V_{CC} = Max., f_{CP} = 10MHz Outputs Open, $\overline{OE}$ = L CP = 50% Duty cycle $V_{HC} \leq V_{IN}$, $V_{IN} \leq V_{LC}$	MIL.	–	10	35	mA
			COM'L.	–	10	30	
		V_{CC} = Max., f_{CP} = 10MHz Outputs Open, $\overline{OE}$ = L CP = 50% Duty cycle V_{IH} = 3.4V, V_{IL} = 0.4V	MIL.	–	20	55	
			COM'L.	–	20	50	

NOTES:

5. I_{CCT} is derived by measuring the total current with all the inputs tied together at 3.4V, subtracting out I_{CCQH}, then dividing by the total number of inputs.
6. Total Supply Current is the sum of the Quiescent current and the Dynamic current (at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:

$$I_{CC} = I_{CCQH}(CD_H) + I_{CCQL}(1 - CD_H) + I_{CCT}(N_T \times D_H) + I_{CCD}(f_{CP})$$

CD_H = Clock duty cycle high period
D_H = Data duty cycle TTL high period (V_{IN} = 3.4V)
N_T = Number of dynamic inputs driven at TTL levels
f_{CP} = Clock Input frequency

CMOS TESTING CONSIDERATIONS

Special test board considerations must be taken into account when applying high-speed CMOS products to the automatic test environment. Large output currents are being switched in very short periods and proper testing demands that test set-ups have minimized inductance and guaranteed zero voltage grounds. The techniques listed below will assist the user in obtaining accurate testing results:

1) All input pins should be connected to a voltage potential during testing. If left floating, the device may oscillate, causing improper device operation and possible latchup.
2) Placement and value of decoupling capacitors is critical. Each physical set-up has different electrical characteristics and it is recommended that various decoupling capacitor sizes be experimented with. Capacitors should be positioned using the minimum lead lengths. They should also be distributed to decouple power supply lines and be placed as close as possible to the DUT power pins.
3) Device grounding is extremely critical for proper device testing. The use of multi-layer performance boards with radial decoupling between power and ground planes is necessary. The ground plane must be sustained from the performance board to the DUT interface board and wiring unused interconnect pins to the ground plane is recommended. Heavy gauge stranded wire should be used for power wiring, with twisted pairs being recommended for minimized inductance.
4) To guarantee data sheet compliance, the input thresholds should be tested per input pin in a static environment. To allow for testing and hardware-induced noise, IDT recommends using $V_{IL} \leq 0V$ and $V_{IH} \geq 3V$ for AC tests.

IDT39C03A GUARANTEED COMMERCIAL RANGE PERFORMANCE

The tables below specify the guaranteed performance of the IDT39C03A over the commercial operating range of 0°C to +70°C with V_{CC} from 4.75 to 5.25V. All data are in nanoseconds, with inputs switching between 0 and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

TABLE 6. CLOCK AND WRITE PULSE CHARACTERISTICS ALL FUNCTIONS

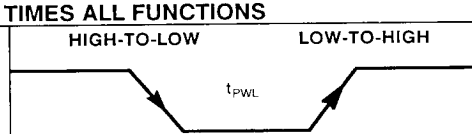
Minimum Clock Low Time	30ns
Minimum Clock High Time	30ns
Minimum Time CP and $\overline{WE}$ both Low to Write	15ns

TABLE 7. ENABLE/DISABLE TIMES ALL FUNCTIONS(1)

FROM	TO	ENABLE	DISABLE
$\overline{OE}_Y$	Y	25	21
$\overline{OE}_B$	DB	25	21
I_8	SIO	25	21
I_8	QIO	38	38
$I_{8,7,6,5}$	QIO	38	38
$I_{4,3,2,1,0}$	QIO	38	35
$\overline{LSS}$	$\overline{WRITE}$	25	21

NOTE:
1. C_L = 5pF for output disable tests. Measurement is made to a 0.5V change on the output.

TABLE 8. SET-UP AND HOLD TIMES ALL FUNCTIONS



FROM	WITH RESPECT TO	SET-UP	HOLD	SET-UP	HOLD	COMMENTS
Y	CP	Don't Care	Don't Care	14	3	Store Y in RAM/Q(1)
$\overline{WE}$ HIGH	CP	15	T_{PWL}		0	Prevent Writing
$\overline{WE}$ LOW	CP	Don't Care	Don't Care	15	0	Write into RAM
A, B Source	CP	20	3	Don't Care	Don't Care	Latch Data from RAM Out
B Destination	CP	6	T_{PWL}		3	Write Data into B Address
$QIO_{0,3}$	CP	Don't Care	Don't Care	17	3	Shift Q
$I_{8,7,6,5}$	CP	12	–	20	0	Write into Q(2)
$\overline{IEN}$ HIGH	CP	24	T_{PWL}		0	Prevent Writing into Q
$\overline{IEN}$ LOW	CP	Don't Care	Don't Care	21	0	Write into Q
$I_{4,3,2,1,0}$	CP	18	–	32	0	Write into Q(2)

NOTES:
1. The internal Y-bus to RAM set-up condition will be met 5ns after valid Y output ($\overline{OE}_Y$ = L)
2. The set-up time with respect to CP falling edge is to prevent writing. The set-up time with respect to CP rising edge is to enable writing.
3. For all other set-up conditions not specified in this table, the set-up time should be the delay to stable Y output plus the Y to RAM internal set-up time. Even if the RAM is not being loaded, this set-up condition ensures valid writing into the Q register and sign compare flip-flop.
4. $\overline{WE}$ controls writing into the RAM. IEN controls writing into Q and, indirectly, controls $\overline{WE}$ through the $\overline{WRITE}/\overline{MSS}$ output. To prevent writing, $\overline{IEN}$ and $\overline{WE}$ must go HIGH during the entire clock LOW time. They may go LOW after the clock has gone LOW to cause a write, provided the $\overline{WE}$ LOW and $\overline{IEN}$ LOW set-up times are met. Having gone LOW, they should not be returned HIGH until after the clock has gone HIGH.
5. A and B addresses must be set up prior to the clock HIGH-TO-LOW transition to latch data at the RAM output.
6. Writing occurs when CP and $\overline{WE}$ are both LOW. The B address should be stable during this entire period.
7. Because $I_{8,7,6,5}$ controls the writing or not writing of data into RAM and Q, they should be stable during the entire clock LOW time unless $\overline{IEN}$ is HIGH, which prevents writing.
8. The set-up time prior to the clock LOW-TO-HIGH transition occurs in parallel with the set-up time prior to the clock HIGH-TO-LOW transition and the clock LOW time. The actual set-up time requirement on $I_{4,3,2,1,0}$ relative to the clock LOW-TO-HIGH transition is the longer of (1) the set-up time prior to clock L → H and (2) the sum of the set-up time prior to clock H → L and the clock LOW time.

8

IDT39C03A GUARANTEED COMMERCIAL RANGE PERFORMANCE
STANDARD FUNCTIONS AND INCREMENT BY ONE OR TWO INSTRUCTIONS (SF4)

FROM	TO											
	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_0	SIO_3	SIO_0 PARITY
A, B Addr	67	55	52	74	61	67	28	–	–	41	62	78
DA, DB	58	50	40	65	54	58	–	–	–	35	59	65
C_n	33	18	–	35	28	26	–	–	–	23	30	38
I_{8-0}	64	64	50	72	61	62	–	34	26*	50*	62*	74*
CP	58	42	43	61	54	58	22	–	22	37	54	60
SIO_0, SIO_3	23	–	–	29	–	–	–	–	–	–	29	19
$\overline{MSS}$	44	–	44	44	44	44	–	–	–	–	44	–
Y	–	–	–	17	–	–	–	–	–	–	–	–
$\overline{IEN}$	–	–	–	–	–	–	–	20	–	–	–	–
$\overline{EA}$	58	50	40	65	54	58	–	–	–	35	59	65

NOTES:
1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. Standard Functions: See Table 2, Increment SF4: $F = S + 1 + C_n$

MULTIPLY INSTRUCTIONS (SF0, SF2, SF6)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_0
A, B Addr	MSS	(67)	(55)	–	–	(61)	(67)	(28)	–	–	(41)
	IS	(67)	(55)	(52)	–	–	–	(28)	–	–	(41)
	LSS	(67)	(55)	(52)	–	–	–	(28)	–	–	(41)
DA, DB	MSS	(58)	(50)	–	–	(54)	(58)	–	–	–	(35)
	IS	(58)	(50)	(40)	–	–	–	–	–	–	(35)
	LSS	(58)	(50)	(40)	–	–	–	–	–	–	(35)
C_n	MSS	35	(18)	–	–	(28)	(26)	–	–	–	(23)
	IS	(33)	(18)	–	–	–	–	–	–	–	(23)
	LSS	(33)	(18)	–	–	–	–	–	–	–	(23)
I_{8-0}	MSS	94	75	–	–	88	88	–	–	(26)	73*
	IS	94	75	71	–	–	–	–	–	(26)	73*
	LSS	94	75	71	30	–	–	–	(34)	(26)	73*
CP	MSS	(58)	(42)	–	–	(54)	(58)	(22)	–	(22)	(37)
	IS	(58)	(42)	(43)	–	–	–	(22)	–	(22)	(37)
	LSS	90	71	67	26	–	–	(22)	–	(22)	69
Z	MSS	64	45	–	–	58	58	–	–	–	43
	IS	64	45	41	–	–	–	–	–	–	43
	LSS	–	–	–	–	–	–	–	–	–	–
SIO_0, SIO_3	Any	(23)	–	–	–	–	–	–	–	–	–

NOTES:
1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.
3. An ( ) means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.
4. Unsigned Multiply
   SF0: $F = S + C_n$ if $Z = 0$
   $F = S + R + C_n$ if $Z = 1$
   Y = Log. F/2
   Q = Log. Q/2
   $Y_3 = C_{n+4}$ (MSS)
   $Z = Q_0$ (LSS)

   Two's Complement Multiply
   SF2: $F = S + C_n$ if $Z = 0$
   $F = R + S + C_n$ if $Z = 1$
   Y = Log. F/2
   Q = Log. Q/2
   $Y_3 = F_3 \oplus$ OVR (MSS)
   $Z = Q_0$ (LSS)

   Two's Complement Multiply Last Cycle
   SF6: $F = S + C_n$ if $Z = 0$
   $F = S - R - 1 + C_n$ if $Z = 1$
   Y = Log. F/2
   Q = Log. Q/2
   $Y_3 =$ OVR $\oplus$ F_3 (MSS)
   $Z = Q_0$ (LSS)

IDT39C03A GUARANTEED COMMERCIAL RANGE PERFORMANCE
DIVIDE INSTRUCTIONS (SFA, SFC, SFE)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	(67)	61/(55)	–	(74)/–	(61)	(67)	(28)	–	–	62
	IS	(67)	(55)	(52)	(74)/–	–	–	(28)	–	–	(41)
	LSS	(67)	(55)	(52)	(74)/–	–	–	(28)	–	–	(41)
DA, DB	MSS	(58)	55/(50)	–	(65)/–	(54)	(58)	–	–	–	59
	IS	(58)	(50)	(40)	(65)/–	–	–	–	–	–	(35)
	LSS	(58)	(50)	(40)	(65)/–	–	–	–	–	–	(35)
C_n	MSS	(33)	33/(18)	–	(35)/–	(28)	27	–	–	–	32
	IS	(33)	(18)	–	(35)/–	–	–	–	–	–	(23)
	LSS	(33)	(18)	–	(35)/–	–	–	–	–	–	(23)
I_{8-0}	MSS	(64)/84	75/68	–	(72)/29	(61)/77	(62)/77	–	–	(26)	63/83*
	IS	(64)/84	(64)/68	(50)/70	(72)	–	–	–	–	(26)	(62)/83*
	LSS	(64)/84	(64)/68	(50)/70	(72)	–	–	–	(34)	(26)	(62)/83*
CP	MSS	(58)/80	46/64	–	(61)/25	(54)/66	(58)/66	(22)	–	(22)	(54)/79
	IS	(58)	(42)	(43)	(61)/–	–	–	(22)	–	(22)	(54)
	LSS	(58)	(42)	(43)	(61)/–	–	–	(22)	–	(22)	(54)
Z	MSS	–	–	–	–	–	–	–	–	–	–
	IS	–/55	–/39	–/41	–	–	–	–	–	–	–/54
	LSS	–/55	–/39	–/41	–	–	–	–	–	–	–/54
SIO_0, SIO_3	Any	(23)	–	–	–	–	–	–	–	–	–

NOTES:

1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. An ( ) means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.
4. If two delays are given, the first is for first divide and normalization; the second is for two's complement divide and two's complement divide correction.
5. Double Length Normalize and First Divide Op
   SFA: $F = S + C_n$
   Y = Log. 2F
   Q = Log. 2Q
   $SIO_3 = F_3 \oplus R_3$(MSS)
   $C_{n+4} = F_3 \oplus F_2$ (MSS)
   $OVR = F_2 \oplus F_1$ (MSS)
   $Z = \overline{Q_0}\,\overline{Q_1}\,\overline{Q_2}\,\overline{Q_3}\,\overline{F_0}\,\overline{F_1}\,\overline{F_2}\,\overline{F_3}$

   Two's Complement Divide
   SFC: $F = R + S + C_n$ if $Z = 0$
   $F = S - R - 1 + C_n$ if $Z = 1$
   Y = Log. 2F
   Q = Log. 2Q
   $SIO_3 = \overline{F_3} \oplus R_3$(MSS)
   $Z = \overline{F_3} \oplus R_3$ (MSS) from previous cycle

   Two's Complement Divide Correction and Remainder
   SFE: $F = R + S + C_n$ if $Z = 0$
   $F = S - R - 1 + C_n$ if $Z = 1$
   $Y = F$
   Q = Log. 2Q
   $Z = \overline{F_3} \oplus R_3$ (MSS) from previous cycle
6. This specification is not tested but is guranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.

8

IDT39C03A GUARANTEED COMMERCIAL RANGE PERFORMANCE
SIGN MAGNITUDE TO TWO'S COMPLEMENT CONVERSION (SF5)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	97	81	–	42	89	89	(28)	–	–	102
	IS	(67)	(55)	(52)	–	–	–	(28)	–	–	(62)
	LSS	(67)	(55)	(52)	–	–	–	(28)	–	–	(62)
DA, DB	MSS	94	76	–	37	84	84	–	–	–	97
	IS	(58)	(50)	(40)	–	–	–	–	–	–	(59)
	LSS	(58)	(50)	(40)	–	–	–	–	–	–	(59)
C_n	MSS	(33)	(18)	–	–	32	27	–	–	–	(30)
	IS	(33)	(18)	–	–	–	–	–	–	–	(30)
	LSS	(33)	(18)	–	–	–	–	–	–	–	(30)
I_{8-0}	MSS	85	67	–	28	82	73	–	–	(26)	88*
	IS	85	67	63	–	–	–	–	–	(26)	88*
	LSS	85	67	63	–	–	–	–	(34)	(26)	88*
CP	MSS	94	76	–	37	84	84	(22)	–	(22)	97
	IS	(58)	(42)	(43)	–	–	–	(22)	–	(22)	(54)
	LSS	(58)	(42)	(43)	–	–	–	(22)	–	(22)	(54)
Z	MSS	–	–	–	–	–	–	–	–	–	–
	IS	57	39	35	–	–	–	–	–	–	60
	LSS	57	39	35	–	–	–	–	–	–	60
SIO_0, SIO_3	Any	(23)	–	–	–	–	–	–	–	–	–

NOTES:

1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. An ( ) means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.
4. SF5: $F = S + C_n$ if $Z = 0$
   $F = \overline{S} + C_n$ if $Z = 1$
   $Y_3 = S_3 \oplus F_3$ (MSS)
   $Z = S_3$ (MSS)
   $Q = Q$
   $N = F_3$ if $Z = 0$
   $N = F_3 \oplus S_3$ if $Z = 1$
5. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.

IDT39C03A GUARANTEED COMMERCIAL RANGE PERFORMANCE SINGLE LENGTH NORMALIZATION (SF8)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	(67)	–	–	–	–	–	(28)	–	–	(62)
	IS	(67)	(55)	(52)	–	–	–	(28)	–	–	(62)
	LSS	(67)	(55)	(52)	–	–	–	(28)	–	–	(62)
DA, DB	MSS	(58)	–	–	–	–	–	–	–	–	(59)
	IS	(58)	(50)	(40)	–	–	–	–	–	–	(59)
	LSS	(58)	(50)	(40)	–	–	–	–	–	–	(59)
C_n	MSS	(33)	–	–	–	–	–	–	–	–	(30)
	IS	(33)	(18)	–	–	–	–	–	–	–	(30)
	LSS	(33)	(18)	–	–	–	–	–	–	–	(30)
I_{8-0}	MSS	(64)	37	–	29	24	24	–	–	(26)	(62)*
	IS	(64)	(64)	(50)	29	–	–	–	–	(26)	(62)*
	LSS	(64)	(64)	(50)	29	–	–	–	(34)	(26)	(62)*
CP	MSS	(58)	29	–	26	26	29	(22)	–	(22)	(54)
	IS	(58)	(42)	(43)	26	–	–	(22)	–	(22)	(54)
	LSS	(58)	(42)	(43)	26	–	–	(22)	–	(22)	(54)
SIO_0, SIO_3	Any	(23)	–	–	–	–	–	–	–	–	–

NOTES:

1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. An ( ) means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.
4. SF8: $F = S + C_n$
   $N = Q_3$ (MSS)
   $Y = F$
   Q = LOG. 2Q
   $C_{n+4} = Q_3 \oplus Q_2$ (MSS)
   $Z = \overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$
   $OVR = Q_2 \oplus Q_1$ (MSS)
5. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.

8

IDT39C03A GUARANTEED MILITARY RANGE PERFORMANCE

The tables below specify the guaranteed performance of the IDT39C03A over the military operating range of -55°C to + 125°C with V_{CC} from 4.5 to 5.5V. All data are in nanoseconds, with inputs switching between 0 and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

TABLE 9. CLOCK AND WRITE PULSE CHARACTERISTICS ALL FUNCTIONS

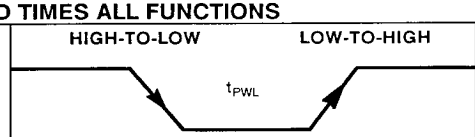
Minimum Clock Low Time	30ns
Minimum Clock High Time	30ns
Minimum Time CP and $\overline{WE}$ both Low to Write	30ns

TABLE 10. ENABLE/DISABLE TIMES ALL FUNCTIONS(1)

FROM	TO	ENABLE	DISABLE
$\overline{OE}_Y$	Y	25	21
$\overline{OE}_B$	DB	25	21
I_8	SIO	25	21
I_8	QIO	38	38
$I_{8,7,6,5}$	QIO	38	38
$I_{4,3,2,1,0}$	QIO	38	35
$\overline{LSS}$	$\overline{WRITE}$	30	25

NOTE:
1. C_L = 5pF for output disable tests. Measurement is made to a 0.5V change on the output.

TABLE 11. SET-UP AND HOLD TIMES ALL FUNCTIONS



FROM	WITH RESPECT TO	SET-UP	HOLD	SET-UP	HOLD	COMMENTS
Y	CP	Don't Care	Don't Care	14	3	Store Y in RAM/Q(1)
$\overline{WE}$ HIGH	CP	15	T_{PWL}		0	Prevent Writing
$\overline{WE}$ LOW	CP	Don't Care	Don't Care	15	0	Write into RAM
A, B Source	CP	20	3	Don't Care	Don't Care	Latch Data from RAM Out
B Destination	CP	6	T_{PWL}		3	Write Data into B Address
$QIO_{0,3}$	CP	Don't Care	Don't Care	17	3	Shift Q
$I_{8,7,6,5}$	CP	12	–	20	0	Write into Q(2)
$\overline{IEN}$ HIGH	CP	24	T_{PWL}		0	Prevent Writing into Q
$\overline{IEN}$ LOW	CP	Don't Care	Don't Care	21	0	Write into Q
$I_{4,3,2,1,0}$	CP	18	–	32	0	Write into Q(2)

NOTES:
1. The internal Y-bus to RAM set-up condition will be met 5ns after valid Y output ($\overline{OE}_Y$ = L)
2. The set-up time with respect to CP falling edge is to prevent writing. The set-up time with respect to CP rising edge is to enable writing.
3. For all other set-up conditions not specified in this table, the set-up time should be the delay to stable Y output plus the Y to RAM internal set-up time. Even if the RAM is not being loaded, this set-up condition ensures valid writing into the Q register and sign compare flip-flop.
4. $\overline{WE}$ controls writing into the RAM. $\overline{IEN}$ controls writing into Q and, indirectly, controls $\overline{WE}$ through the $\overline{WRITE}/\overline{MSS}$ output. To prevent writing, $\overline{IEN}$ and $\overline{WE}$ must go HIGH during the entire clock LOW time. They may go LOW after the clock has gone LOW to cause a write, provided the $\overline{WE}$ LOW and $\overline{IEN}$ LOW set-up times are met. Having gone LOW, they should not be returned HIGH until after the clock has gone HIGH.
5. A and B addresses must be set up prior to the clock HIGH-TO-LOW transition to latch data at the RAM output.
6. Writing occurs when CP and $\overline{WE}$ are both LOW. The B address should be stable during this entire period.
7. Because $I_{8,7,6,5}$ controls the writing or not writing of data into RAM and Q, they should be stable during the entire clock LOW time unless $\overline{IEN}$ is HIGH, which prevents writing.
8. The set-up time prior to the clock LOW-TO-HIGH transition occurs in parallel with the set-up time prior to the clock HIGH-TO-LOW transition and the clock LOW time. The actual set-up time requirement on $I_{4,3,2,1,0}$ relative to the clock LOW-TO-HIGH transition is the longer of (1) the set-up time prior to clock L ⟶ H and (2) the sum of the set-up time prior to clock H ⟶ L and the clock LOW time.

IDT39C03A GUARANTEED MILITARY RANGE PERFORMANCE
STANDARD FUNCTIONS AND INCREMENT BY ONE OR TWO INSTRUCTIONS (SF4)

FROM	TO											
	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_0	SIO_3	SIO_0 PARITY
A, B Addr	70	58	52	78	68	67	28	–	–	47	71	84
DA, DB	60	52	40	66	55	58	–	–	–	35	61	74
C_n	35	19	–	41	31	29	–	–	–	23	33	40
I_{8-0}	72	69	56	80	71	69	–	36	26*	58*	75*	89*
CP	60	42	43	67	55	58	22	–	22	41	61	66
SIO_0, SIO_3	26	–	–	29	–	–	–	–	–	–	29	19
$\overline{MSS}$	44	–	44	44	44	44	–	–	–	–	44	–
Y	–	–	–	17	–	–	–	–	–	–	–	–
$\overline{IEN}$	–	–	–	–	–	–	–	20	–	–	–	–
$\overline{EA}$	60	52	40	66	55	58	–	–	–	35	61	74

NOTES:
1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. Standard Functions: See Table 2, Increment SF4: $F = S + 1 + C_n$

MULTIPLY INSTRUCTIONS (SF0, SF2, SF6)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_0
A, B Addr	MSS	72	(58)	–	–	(68)	(67)	(28)	–	–	(47)
	IS	(70)	(58)	(52)	–	–	–	(28)	–	–	(47)
	LSS	(70)	(58)	(52)	–	–	–	(28)	–	–	(47)
DA, DB	MSS	62	(52)	–	–	(55)	(58)	–	–	–	(35)
	IS	(60)	(52)	(40)	–	–	–	–	–	–	(35)
	LSS	(60)	(52)	(40)	–	–	–	–	–	–	(35)
C_n	MSS	40	(19)	–	–	(31)	(29)	–	–	–	(23)
	IS	(35)	(19)	–	–	–	–	–	–	–	(23)
	LSS	(35)	(19)	–	–	–	–	–	–	–	(23)
I_{8-0}	MSS	108	84	–	–	98	98	–	–	(26)	81*
	IS	108	84	80	–	–	–	–	–	(26)	81*
	LSS	108	84	80	33	–	–	–	(36)	(26)	81*
CP	MSS	62	(42)	–	–	(55)	(58)	(22)	–	(22)	(41)
	IS	(60)	(42)	(43)	–	–	–	(22)	–	(22)	(41)
	LSS	104	80	74	29	–	–	(22)	–	(22)	77
Z	MSS	75	51	–	–	65	65	–	–	–	48
	IS	75	51	47	–	–	–	–	–	–	48
	LSS	–	–	–	–	–	–	–	–	–	–
SIO_0, SIO_3	Any	(26)	–	–	–	–	–	–	–	–	–

NOTES:
1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. An ( ) means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.
4. Unsigned Multiply
   SF0: $F = S + C_n$ if $Z = 0$
   $F = S + R + C_n$ if $Z = 1$
   Y = Log. F/2
   Q = Log. Q/2
   $Y_3 = C_{n+4}$ (MSS)
   $Z = Q_0$ (LSS)

   Two's Complement Multiply
   SF2: $F = S + C_n$ if $Z = 0$
   $F = R + S + C_n$ if $Z = 1$
   Y = Log. F/2
   Q = Log. Q/2
   $Y_3 = F_3 \oplus$ OVR (MSS)
   $Z = Q_0$ (LSS)

   Two's Complement Multiply Last Cycle
   SF6: $F = S + C_n$ if $Z = 0$
   $F = S - R - 1 + C_n$ if $Z = 1$
   Y = Log. F/2
   Q = Log. Q/2
   $Y_3 =$ OVR $\oplus F_3$ (MSS)
   $Z = Q_0$ (LSS)
5. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.

IDT39C03A GUARANTEED MILITARY RANGE PERFORMANCE
DIVIDE INSTRUCTIONS (SFA, SFC, SFE)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	(70)	72/(58)	–	(78)/–	(68)	(67)	(28)	–	–	(71)
	IS	(70)	(58)	(52)	(78)/–	–	–	(28)	–	–	(71)
	LSS	(70)	(58)	(52)	(78)/–	–	–	(28)	–	–	(71)
DA, DB	MSS	(60)	66/(52)	–	(66)/–	(55)	(58)	–	–	–	(61)
	IS	(60)	(52)	(40)	(66)/–	–	–	–	–	–	(61)
	LSS	(60)	(52)	(40)	(66)/–	–	–	–	–	–	(61)
C_n	MSS	(35)	37/(19)	–	(41)/–	(31)	(29)	–	–	–	36
	IS	(35)	(19)	–	(41)/–	–	–	–	–	–	(33)
	LSS	(35)	(19)	–	(41)/–	–	–	–	–	–	(33)
I_{8-0}	MSS	(72)/96	89/79	–	(80)/33	(71)/91	(69)/91	–	–	(26)	76/98*
	IS	(72)/96	(69)/79	(56)/79	(80)/–	–	–	–	–	(26)	(75)/98*
	LSS	(72)/96	(69)/79	(56)/79	(80)/–	–	–	–	(36)	(26)	(75)/98*
CP	MSS	(60)/91	51/74	–	(67)/28	(55)/74	(58)/74	(22)	–	(22)	(61)/93
	IS	(60)	(42)	(43)	(67)/–	–	–	(22)	–	(22)	(61)
	LSS	(60)	(42)	(43)	(67)/–	–	–	(22)	–	(22)	(61)
Z	MSS	–	–	–	–	–	–	–	–	–	–
	IS	–/63	–/46	–/46	–	–	–	–	–	–	–/65
	LSS	–/63	–/46	–/46	–	–	–	–	–	–	–/65
SIO_0, SIO_3	Any	(26)	–	–	–	–	–	–	–	–	–

NOTES:

1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. An ( ) means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.
4. If two delays are given, the first is for 1st divide and normalization; the second is for two's complement divide and two's complement divide correction.
5. Double Length Normalize and First Divide Op
   SFA: $F = S + C_n$
   $Y = \text{Log. } 2F$
   $Q = \text{Log. } 2Q$
   $SIO_3 = F_3 \oplus R_3(MSS)$
   $C_{n+4} = F_3 \oplus F_2\ (MSS)$
   $OVR = F_2 \oplus F_1\ (MSS)$
   $Z = \overline{Q_0}\,\overline{Q_1}\,\overline{Q_2}\,\overline{Q_3}\,\overline{F_0}\,\overline{F_1}\,\overline{F_2}\,\overline{F_3}$

   Two's Complement Divide
   SFC: $F = R + S + C_n$ if $Z = 0$
   $F = S - R - 1 + C_n$ if $Z = 1$
   $Y = \text{Log. } 2F$
   $Q = \text{Log. } 2Q$
   $SIO_3 = \overline{F_3 \oplus R_3}(MSS)$
   $Z = \overline{F_3 \oplus R_3}$ (MSS) from previous cycle

   Two's Complement Divide Correction and Remainder
   SFE: $F = R + S + C_n$ if $Z = 0$
   $F = S - R - 1 + C_n$ if $Z = 1$
   $Y = F$
   $Q = \text{Log. } 2Q$
   $Z = F_3 \oplus R_3(MSS)$ from previous cycle
6. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.

IDT39C03A GUARANTEED MILITARY RANGE PERFORMANCE
SIGN MAGNITUDE TO TWO'S COMPLEMENT CONVERSION (SF5)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	114	95	–	49	106	106	(28)	–	–	125
	IS	(70)	(58)	(52)	–	–	–	(28)	–	–	(71)
	LSS	(70)	(58)	(52)	–	–	–	(28)	–	–	(71)
DA, DB	MSS	108	89	–	43	101	101	–	–	–	119
	IS	(60)	(52)	(40)	–	–	–	–	–	–	(61)
	LSS	(60)	(52)	(40)	–	–	–	–	–	–	(61)
C_n	MSS	36	(19)	–	–	35	(29)	–	–	–	(33)
	IS	(35)	(19)	–	–	–	–	–	–	–	(33)
	LSS	(35)	(19)	–	–	–	–	–	–	–	(33)
I_{8-0}	MSS	98	79	–	33	97	88	–	–	(26)	109*
	IS	98	79	73	–	–	–	–	–	(26)	109*
	LSS	98	79	73	–	–	–	–	(36)	(26)	109*
CP	MSS	108	89	–	43	101	101	(22)	–	(22)	119
	IS	(60)	(42)	(43)	–	–	–	(22)	–	(22)	(61)
	LSS	(60)	(42)	(43)	–	–	–	(22)	–	(22)	(61)
Z	MSS	–	–	–	–	–	–	–	–	–	–
	IS	65	46	40	–	–	–	–	–	–	76
	LSS	65	46	40	–	–	–	–	–	–	76
SIO_0, SIO_3	Any	(26)	–	–	–	–	–	–	–	–	–

NOTES:

1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. An ( ) means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.
4. SF5: $F = S + C_n$ if $Z = 0$
   $F = \overline{S} + C_n$ if $Z = 1$
   $Y_3 = S_3 \oplus F_3$ (MSS)
   $Z = S_3$ (MSS)
   $Y = F$
   $Q = Q$
   $N = F_3$ if $Z = 0$
   $N = F_3 \oplus S_3$ if $Z = 1$
5. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.

8

IDT39C03A GUARANTEED MILITARY RANGE PERFORMANCE
SINGLE LENGTH NORMALIZATION (SF8)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	(70)	–	–	–	–	–	(28)	–	–	(71)
	IS	(70)	(58)	(52)	–	–	–	(28)	–	–	(71)
	LSS	(70)	(58)	(52)	–	–	–	(28)	–	–	(71)
DA, DB	MSS	(60)	–	–	–	–	–	–	–	–	(61)
	IS	(60)	(52)	(40)	–	–	–	–	–	–	(61)
	LSS	(60)	(52)	(40)	–	–	–	–	–	–	(61)
C_n	MSS	(35)	–	–	–	–	–	–	–	–	(33)
	IS	(35)	(19)	–	–	–	–	–	–	–	(33)
	LSS	(35)	(19)	–	–	–	–	–	–	–	(33)
I_{8-0}	MSS	(72)	47	–	33	27	27	–	–	(26)	(75)*
	IS	(72)	(69)	(56)	33	–	–	–	–	(26)	(75)*
	LSS	(72)	(69)	(56)	33	–	–	–	(36)	(26)	(75)*
CP	MSS	(60)	31	–	28	26	31	(22)	–	(22)	(61)
	IS	(60)	(42)	(43)	28	–	–	(22)	–	(22)	(61)
	LSS	(60)	(42)	(43)	28	–	–	(22)	–	(22)	(61)
SIO_0, SIO_3	Any	(26)	–	–	–	–	–	–	–	–	–

NOTES:

1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. An ( ) means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.
4. SF8: $F = S + C_n$
   $N = Q_3$ (MSS)
   $Y = F$
   Q = LOG. 2Q
   $C_{n+4} = Q_3 \oplus Q_2$ (MSS)
   $Z = \overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$
   $OVR = Q_2 \oplus Q_1$ (MSS)
5. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.

IDT39C03B GUARANTEED COMMERCIAL RANGE PERFORMANCE

The tables below specify the guaranteed performance of the IDT39C03B over the commercial operating range of 0°C to +70°C with V_{CC} from 4.75 to 5.25V. All data are in nanoseconds, with inputs switching between 0 and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

TABLE 12. CLOCK AND WRITE PULSE CHARACTERISTICS ALL FUNCTIONS

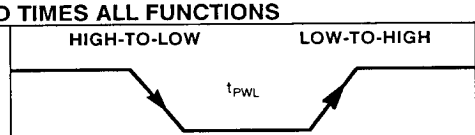
Minimum Clock Low Time	24ns
Minimum Clock High Time	24ns
Minimum Time CP and $\overline{WE}$ both Low to Write	12ns

TABLE 13. ENABLE/DISABLE TIMES ALL FUNCTIONS(1)

FROM	TO	ENABLE	DISABLE
$\overline{OE}_Y$	Y	20	17
$\overline{OE}_B$	DB	20	17
I_8	SIO	20	17
I_8	QIO	30	30
$I_{8,7,6,5}$	QIO	30	30
$I_{4,3,2,1,0}$	QIO	30	30
$\overline{LSS}$	$\overline{WRITE}$	20	17

NOTE:
1. C_L = 5pF for output disable tests. Measurement is made to a 0.5V change on the output.

TABLE 14. SET-UP AND HOLD TIMES ALL FUNCTIONS



FROM	WITH RESPECT TO	SET-UP	HOLD	SET-UP	HOLD	COMMENTS
Y	CP	Don't Care	Don't Care	11	3	Store Y in RAM/Q(1)
$\overline{WE}$ HIGH	CP	12	T_{PWL}		0	Prevent Writing
$\overline{WE}$ LOW	CP	Don't Care	Don't Care	12	0	Write into RAM
A, B Source	CP	16	3	Don't Care	Don't Care	Latch Data from RAM Out
B Destination	CP	5	T_{PWL}		3	Write Data into B Address
$QIO_{0,3}$	CP	Don't Care	Don't Care	14	3	Shift Q
$I_{8,7,6,5}$	CP	10	–	16	0	Write into Q(2)
$\overline{IEN}$ HIGH	CP	19	T_{PWL}		0	Prevent Writing into Q
$\overline{IEN}$ LOW	CP	Don't Care	Don't Care	17	0	Write into Q
$I_{4,3,2,1,0}$	CP	14	–	25	0	Write into Q(2)

NOTES:
1. The internal Y-bus to RAM set-up condition will be met 5ns after valid Y output ($\overline{OE}_Y$ = L)
2. The set-up time with respect to CP falling edge is to prevent writing. The set-up time with respect to CP rising edge is to enable writing.
3. For all other set-up conditions not specified in this table, the set-up time should be the delay to stable Y output plus the Y to RAM internal set-up time. Even if the RAM is not being loaded, this set-up condition ensures valid writing into the Q register and sign compare flip-flop.
4. $\overline{WE}$ controls writing into the RAM. $\overline{IEN}$ controls writing into Q and, indirectly, controls $\overline{WE}$ through the $\overline{WRITE}/\overline{MSS}$ output. To prevent writing, $\overline{IEN}$ and $\overline{WE}$ must go HIGH during the entire clock LOW time. They may go LOW after the clock has gone LOW to cause a write, provided the $\overline{WE}$ LOW and $\overline{IEN}$ LOW set-up times are met. Having gone LOW, they should not be returned HIGH until after the clock has gone HIGH.
5. A and B addresses must be set up prior to the clock HIGH-TO-LOW transition to latch data at the RAM output.
6. Writing occurs when CP and $\overline{WE}$ are both LOW. The B address should be stable during this entire period.
7. Because $I_{8,7,6,5}$ controls the writing or not writing of data into RAM and Q, they should be stable during the entire clock LOW time unless $\overline{IEN}$ is HIGH, which prevents writing.
8. The set-up time prior to the clock LOW-TO-HIGH transition occurs in parallel with the set-up time prior to the clock HIGH-TO-LOW transition and the clock LOW time. The actual set-up time requirement on $I_{4,3,2,1,0}$ relative to the clock LOW-TO-HIGH transition is the longer of (1) the set-up time prior to clock L → H and (2) the sum of the set-up time prior to clock H → L and the clock LOW time.

8

IDT39C03B GUARANTEED COMMERCIAL RANGE PERFORMANCE
STANDARD FUNCTIONS AND INCREMENT BY ONE OR TWO INSTRUCTIONS (SF4)

FROM	TO											
	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_0	SIO_3	SIO_0 PARITY
A, B Addr	54	44	41	60	49	54	23	–	–	33	50	62
DA, DB	46	40	32	52	43	47	–	–	–	28	47	52
C_n	26	15	–	28	22	20	–	–	–	19	24	30
I_{8-0}	51	51	40	58	49	50	–	27	21*	40*	50*	59*
CP	46	34	35	49	43	47	18	–	18	30	43	48
SIO_0, SIO_3	19	–	–	23	–	–	–	–	–	–	23	15
$\overline{MSS}$	35	–	35	35	35	35	–	–	–	–	35	–
Y	–	–	–	14	–	–	–	–	–	–	–	–
$\overline{IEN}$	–	–	–	–	–	–	–	16	–	–	–	–
$\overline{EA}$	46	40	32	52	43	47	–	–	–	28	47	52

NOTES:

1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. Standard Functions: See Table 2, Increment SF4: $F = S + 1 + C_n$

MULTIPLY INSTRUCTIONS (SF0, SF2, SF6)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_0
A, B Addr	MSS	(54)	(44)	–	–	(49)	(54)	(23)	–	–	(33)
	IS	(54)	(44)	(41)	–	–	–	(23)	–	–	(33)
	LSS	(54)	(44)	(41)	–	–	–	(23)	–	–	(33)
DA, DB	MSS	(46)	(40)	–	–	(43)	(47)	–	–	–	(28)
	IS	(46)	(40)	(32)	–	–	–	–	–	–	(28)
	LSS	(46)	(40)	(32)	–	–	–	–	–	–	(28)
C_n	MSS	28	(15)	–	–	(22)	(20)	–	–	–	(19)
	IS	(26)	(15)	–	–	–	–	–	–	–	(19)
	LSS	(26)	(15)	–	–	–	–	–	–	–	(19)
I_{8-0}	MSS	75	60	–	–	70	70	–	–	(21)	58*
	IS	75	60	57	–	–	–	–	–	(21)	58*
	LSS	75	60	57	24	–	–	–	(27)	(21)	58*
CP	MSS	(46)	(34)	–	–	(43)	(47)	(18)	–	(18)	(30)
	IS	(46)	(34)	(35)	–	–	–	(18)	–	(18)	(30)
	LSS	72	57	54	21	–	–	(18)	–	(18)	55
Z	MSS	51	36	–	–	46	46	–	–	–	34
	IS	51	36	33	–	–	–	–	–	–	34
	LSS	–	–	–	–	–	–	–	–	–	–
SIO_0, SIO_3	Any	(19)	–	–	–	–	–	–	–	–	–

NOTES:

1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. An ( ) means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.
4. Unsigned Multiply
   SF0: $F = S + C_n$ if $Z = 0$
   $F = S + R + C_n$ if $Z = 1$
   Y = Log. F/2
   Q = Log. Q/2
   $Y_3 = C_{n+4}$ (MSS)
   $Z = Q_0$ (LSS)

   Two's Complement Multiply
   SF2: $F = S + C_n$ if $Z = 0$
   $F = R + S + C_n$ if $Z = 1$
   Y = Log. F/2
   Q = Log. Q/2
   $Y_3 = F_3 \oplus$ OVR (MSS)
   $Z = Q_0$ (LSS)

   Two's Complement Multiply Last Cycle
   SF6: $F = S + C_n$ if $Z = 0$
   $F = S - R - 1 + C_n$ if $Z = 1$
   Y = Log. F/2
   Q = Log. Q/2
   $Y_3 =$ OVR $\oplus$ (MSS)
   $Z = Q_0$ (LSS)
5. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.

IDT39C03B GUARANTEED COMMERCIAL RANGE PERFORMANCE
DIVIDE INSTRUCTIONS (SFA, SFC, SFE)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	(54)	48/(44)	–	(60)/–	(49)	(54)	(23)	–	–	50
	IS	(54)	(44)	(41)	(60)/–	–	–	(23)	–	–	(33)
	LSS	(54)	(44)	(41)	(60)/–	–	–	(23)	–	–	(33)
DA, DB	MSS	(46)	44/(40)	–	(52)/–	(43)	(47)	–	–	–	47
	IS	(46)	(40)	(32)	(52)/–	–	–	–	–	–	(28)
	LSS	(46)	(40)	(32)	(52)/–	–	–	–	–	–	(28)
C_n	MSS	(26)	26/(15)	–	(28)/–	(22)	23	–	–	–	26
	IS	(26)	(15)	–	(28)/–	–	–	–	–	–	(19)
	LSS	(26)	(15)	–	(28)/–	–	–	–	–	–	(19)
I_{8-0}	MSS	(51)/67	(51)/54	–	57/23	(49)/62	(50)/73	–	–	(21)	(50)/66*
	IS	(51)/67	(51)/54	(40)/56	57/–	–	–	–	–	(21)	(50)/66*
	LSS	(51)/67	(51)/54	(40)/56	57/–	–	–	–	(27)	(21)	(50)/66*
CP	MSS	(46)/64	37/51	–	(49)/20	(43)/53	(47)53	(18)	–	(18)	(43)/63
	IS	(46)	(34)	(35)	(49)/–	–	–	(18)	–	(18)	(43)
	LSS	(46)	(34)	(35)	(49)/–	–	–	(18)	–	(18)	(43)
Z	MSS	–	–	–	–	–	–	–	–	–	–
	IS	–/44	–/31	–/33	–	–	–	–	–	–	–/43
	LSS	–/44	–/31	–/33	–	–	–	–	–	–	–/43
SIO_0, SIO_3	Any	(19)	–	–	–	–	–	–	–	–	–

NOTES:

1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. An ( ) means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.
4. If two delays are given, the first is for 1st divide and normalization; the second is for two's complement divide and two's complement divide correction.
5. Double Length Normalize and First Divide Op
   SFA: $F = S + C_n$
   Y = Log. 2F
   Q = Log. 2Q
   $SIO_3 = F_3 \oplus R_3$(MSS)
   $C_{n+4} = F_3 \oplus F_2$ (MSS)
   $OVR = F_2 \oplus F_1$ (MSS)
   $Z = \overline{Q}_0 \overline{Q}_1 \overline{Q}_2 \overline{Q}_3 \overline{F}_0 \overline{F}_1 \overline{F}_2 \overline{F}_3$

   Two's Complement Divide
   SFC: $F = R + S + C_n$ if $Z = 0$
   $F = S - R - 1 + C_n$ if $Z = 1$
   Y = Log. 2F
   Q = Log. 2Q
   $SIO_3 = \overline{F_3 \oplus R_3}$(MSS)
   $Z = \overline{F_3 \oplus R_3}$ (MSS) from previous cycle

   Two's Complement Divide Correction and Remainder
   SFE: $F = R + S + C_n$ if $Z = 0$
   $F = S - R - 1 + C_n$ if $Z = 1$
   $Y = F$
   Q = Log. 2Q
   $Z = F_3 \oplus R_3$(MSS) from previous cycle
6. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.

8

IDT39C03B GUARANTEED COMMERCIAL RANGE PERFORMANCE
SIGN MAGNITUDE TO TWO'S COMPLEMENT CONVERSION (SF5)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	77	65	–	34	72	72	(23)	–	–	82
	IS	(54)	(44)	(41)	–	–	–	(23)	–	–	(50)
	LSS	(54)	(44)	(41)	–	–	–	(23)	–	–	(50)
DA, DB	MSS	75	60	–	30	67	67	–	–	–	78
	IS	(46)	(40)	(32)	–	–	–	–	–	–	(47)
	LSS	(46)	(40)	(32)	–	–	–	–	–	–	(47)
C_n	MSS	(26)	(15)	–	–	26	22	–	–	–	(24)
	IS	(26)	(15)	–	–	–	–	–	–	–	(24)
	LSS	(26)	(15)	–	–	–	–	–	–	–	(24)
I_{8-0}	MSS	68	54	–	23	66	58	–	–	(21)	70*
	IS	68	54	50	–	–	–	–	–	(21)	70*
	LSS	68	54	50	–	–	–	–	(27)	(21)	70*
CP	MSS	75	60	–	30	67	67	(18)	–	(18)	77
	IS	(46)	(34)	(35)	–	–	–	(18)	–	(18)	(43)
	LSS	(46)	(34)	(35)	–	–	–	(18)	–	(18)	(43)
Z	MSS	–	–	–	–	–	–	–	–	–	–
	IS	46	32	28	–	–	–	–	–	–	48
	LSS	(19)	32	28	–	–	–	–	–	–	48

NOTES:

1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. An ( ) means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.
4. SF5: $F = S + C_n$ if $Z = 0$
   $F = \overline{S} + C_n$ if $Z = 1$
   $Y_3 = S_3 \oplus F_3$ (MSS)
   $Z = S_3$ (MSS)
   $Q = Q$
   $N = F_3$ if $Z = 0$
   $N = F_3 \oplus S_3$ if $Z = 1$
5. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.

IDT39C03B GUARANTEED COMMERCIAL RANGE PERFORMANCE
SINGLE LENGTH NORMALIZATION (SF8)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	(54)	–	–	–	–	–	(23)	–	–	(50)
	IS	(54)	(44)	(41)	–	–	–	(23)	–	–	(50)
	LSS	(54)	(44)	(41)	–	–	–	(23)	–	–	(50)
DA, DB	MSS	(46)	–	–	–	–	–	–	–	–	(47)
	IS	(46)	(40)	(32)	–	–	–	–	–	–	(47)
	LSS	(46)	(40)	(32)	–	–	–	–	–	–	(47)
C_n	MSS	(26)	–	–	–	–	–	–	–	–	(24)
	IS	(26)	(15)	–	–	–	–	–	–	–	(24)
	LSS	(26)	(15)	–	–	–	–	–	–	–	(24)
I_{8-0}	MSS	(51)	30	–	23	19	19	–	–	(21)	(50)*
	IS	(51)	52	(40)	23	–	–	–	–	(21)	(50)*
	LSS	(51)	52	(40)	23	–	–	–	(27)	(21)	(50)*
CP	MSS	(46)	23	–	21	21	21	(18)	–	(18)	(43)
	IS	(46)	(34)	(35)	21	–	–	(18)	–	(18)	(43)
	LSS	(46)	(34)	(35)	21	–	–	(18)	–	(18)	(43)
Z	MSS	–	–	–	–	–	–	–	–	–	–
	IS	–	–	–	–	–	–	–	–	–	–
	LSS	–	–	–	–	–	–	–	–	–	–
SIO_0, SIO_3	Any	(19)	–	–	–	–	–	–	–	–	–

NOTES:

1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. An ( ) means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.
4. SF8: $F = S + C_n$
   $N = Q_3$ (MSS)
   $Y = F$
   Q = LOG. 2Q
   $C_{n+4} = Q_3 \oplus Q_2$ (MSS)
   $Z = \overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$
   $OVR = Q_2 \oplus Q_1$ (MSS)
5. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.

8

IDT39C03B GUARANTEED MILITARY RANGE PERFORMANCE

The tables below specify the guaranteed performance of the IDT39C03B over the military operating range of -55°C to +125°C with V_{CC} from 4.5 to 5.5V. All data are in nanoseconds, with inputs switching between 0 and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

TABLE 15. CLOCK AND WRITE PULSE CHARACTERISTICS ALL FUNCTIONS

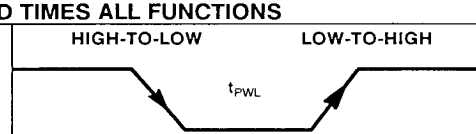
Minimum Clock Low Time	24ns
Minimum Clock High Time	24ns
Minimum Time CP and $\overline{WE}$ both Low to Write	24ns

TABLE 16. ENABLE/DISABLE TIMES ALL FUNCTIONS(1)

FROM	TO	ENABLE	DISABLE
$\overline{OE}_Y$	Y	20	17
$\overline{OE}_B$	DB	20	17
I_8	SIO	20	17
I_8	QIO	30	30
$I_{8,7,6,5}$	QIO	30	30
$I_{4,3,2,1,0}$	QIO	30	28
$\overline{LSS}$	$\overline{WRITE}$	24	20

NOTE:
1. C_L = 5pF for output disable tests. Measurement is made to a 0.5V change on the output.

TABLE 17. SET-UP AND HOLD TIMES ALL FUNCTIONS



FROM	WITH RESPECT TO	SET-UP	HOLD	SET-UP	HOLD	COMMENTS
Y	CP	Don't Care	Don't Care	11	3	Store Y in RAM/Q(1)
$\overline{WE}$ HIGH	CP	12	T_{PWL}		0	Prevent Writing
$\overline{WE}$ LOW	CP	Don't Care	Don't Care	12	0	Write into RAM
A, B Source	CP	16	3	Don't Care	Don't Care	Latch Data from RAM Out
B Destination	CP	5	T_{PWL}		3	Write Data into B Address
$QIO_{0,3}$	CP	Don't Care	Don't Care	14	3	Shift Q
$I_{8,7,6,5}$	CP	10	–	16	0	Write into Q(2)
$\overline{IEN}$ HIGH	CP	19	T_{PWL}		0	Prevent Writing into Q
$\overline{IEN}$ LOW	CP	Don't Care	Don't Care	17	0	Write into Q
$I_{4,3,2,1,0}$	CP	14	–	25	0	Write into Q(2)

NOTES:
1. The internal Y-bus to RAM set-up condition will be met 5ns after valid Y output ($\overline{OE}_Y$ = L)
2. The set-up time with respect to CP falling edge is to prevent writing. The set-up time with respect to CP rising edge is to enable writing.
3. For all other set-up conditions not specified in this table, the set-up time should be the delay to stable Y output plus the Y to RAM internal set-up time. Even if the RAM is not being loaded, this set-up condition ensures valid writing into the Q register and sign compare flip-flop.
4. $\overline{WE}$ controls writing into the RAM. $\overline{IEN}$ controls writing into Q and, indirectly, controls $\overline{WE}$ through the $\overline{WRITE}/\overline{MSS}$ output. To prevent writing, $\overline{IEN}$ and $\overline{WE}$ must go HIGH during the entire clock LOW time. They may go LOW after the clock has gone LOW to cause a write, provided the $\overline{WE}$ LOW and $\overline{IEN}$ LOW set-up times are met. Having gone LOW, they should not be returned HIGH until after the clock has gone HIGH.
5. A and B addresses must be set up prior to the clock HIGH-TO-LOW transition to latch data at the RAM output.
6. Writing occurs when CP and $\overline{WE}$ are both LOW. The B address should be stable during this entire period.
7. Because $I_{8,7,6,5}$ controls the writing or not writing of data into RAM and Q, they should be stable during the entire clock LOW time unless $\overline{IEN}$ is HIGH, which prevents writing.
8. The set-up time prior to the clock LOW-TO-HIGH transition occurs in parallel with the set-up time prior to the clock HIGH-TO-LOW transition and the clock LOW time. The actual set-up time requirement on $I_{4,3,2,1,0}$ relative to the clock LOW-TO-HIGH transition is the longer of (1) the set-up time prior to clock L → H and (2) the sum of the set-up time prior to clock H → L and the clock LOW time.

IDT39C03B GUARANTEED MILITARY RANGE PERFORMANCE
STANDARD FUNCTIONS AND INCREMENT BY ONE OR TWO INSTRUCTIONS (SF4)

FROM	TO											
	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_0	SIO_3	SIO_0 PARITY
A, B Addr	56	46	42	62	55	54	23	–	–	38	57	67
DA, DB	48	42	32	53	44	46	–	–	–	28	49	59
C_n	28	15	–	33	25	23	–	–	–	19	26	32
I_{8-0}	57	55	45	64	57	55	–	29	21	46	60	72
CP	48	33	34	54	44	46	18	–	18	33	49	53
SIO_0, SIO_3	20	–	–	23	–	–	–	–	–	–	23	15
$\overline{MSS}$	35	–	35	35	35	35	–	–	–	–	35	–
Y	–	–	–	14	–	–	–	–	–	–	–	–
$\overline{IEN}$	–	–	–	–	–	–	–	16	–	–	–	–
$\overline{EA}$	48	42	32	53	44	46	–	–	–	28	49	59

NOTES:
1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. Standard Functions: See Table 2, Increment SF4: $F = S + 1 + C_n$

MULTIPLY INSTRUCTIONS (SF0, SF2, SF6)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_0
A, B Addr	MSS	58	(46)	–	–	(55)	(54)	(23)	–	–	(38)
	IS	(56)	(46)	(42)	–	–	–	(23)	–	–	(38)
	LSS	(56)	(46)	(42)	–	–	–	(23)	–	–	(38)
DA, DB	MSS	50	(42)	–	–	(44)	(46)	–	–	–	(28)
	IS	(48)	(42)	(32)	–	–	–	–	–	–	(28)
	LSS	(48)	(42)	(32)	–	–	–	–	–	–	(28)
C_n	MSS	32	(15)	–	–	(25)	(23)	–	–	–	(19)
	IS	(28)	(15)	–	–	–	–	–	–	–	(19)
	LSS	(28)	(15)	–	–	–	–	–	–	–	(19)
I_{8-0}	MSS	86	67	–	–	78	78	–	–	(21)	65*
	IS	86	67	64	–	–	–	–	–	(21)	65*
	LSS	86	67	64	27	–	–	–	(29)	(21)	65*
CP	MSS	50	(33)	–	–	(44)	(46)	(18)	–	(18)	(33)
	IS	(48)	(33)	(34)	–	–	–	(18)	–	(18)	(33)
	LSS	83	64	59	23	–	–	(18)	–	(18)	62
Z	MSS	60	40	–	–	52	52	–	–	–	38
	IS	60	40	38	–	–	–	–	–	–	38
	LSS	–	–	–	–	–	–	–	–	–	–
SIO_0, SIO_3	Any	(20)	–	–	–	–	–	–	–	–	–

NOTES:
1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. An ( ) means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.
4. Unsigned Multiply
   SF0: $F = S + C_n$ if $Z = 0$
   $F = S + R + C_n$ if $Z = 1$
   $Y =$ Log. F/2
   $Q =$ Log. Q/2
   $Y_3 = C_{n+4}$ (MSS)
   $Z = Q_0$ (LSS)

   Two's Complement Multiply
   SF2: $F = S + C_n$ if $Z = 0$
   $F = R + S + C_n$ if $Z = 1$
   $Y =$ Log. F/2
   $Q =$ Log. Q/2
   $Y_3 = F_3 \oplus$ OVR (MSS)
   $Z = Q_0$ (LSS)

   Two's Complement Multiply Last Cycle
   SF6: $F = S + C_n$ if $Z = 0$
   $F = S - R - 1 + C_n$ if $Z = 1$
   $Y =$ Log. F/2
   $Q =$ Log. Q/2
   $Y_3 =$ OVR $\oplus$ (MSS)
   $Z = Q_0$ (LSS)
5. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.

IDT39C03B GUARANTEED MILITARY RANGE PERFORMANCE
DIVIDE INSTRUCTIONS (SFA, SFC, SFE)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO
A, B Addr	MSS	(56)	58/(46)	–	(62)/–	(55)	(54)	(23)	–	–	(57)
	IS	(56)	(46)	(42)	(62)/–	–	–	(23)	–	–	(57)
	LSS	(56)	(46)	(42)	(62)/–	–	–	(23)	–	–	(57)
DA, DB	MSS	(48)	(42)	–	(53)/–	(44)	(46)	–	–	–	(49)
	IS	(48)	(42)	(32)	(53)/–	–	–	–	–	–	(49)
	LSS	(48)	(42)	(32)	(53)/–	–	–	–	–	–	(49)
C_n	MSS	(28)	30/(15)	–	(33)/–	(25)	(23)	–	–	–	29
	IS	(28)	(15)	–	(33)/–	–	–	–	–	–	(19)
	LSS	(28)	(15)	–	(33)/–	–	–	–	–	–	(19)
I_{8-0}	MSS	(57)/77	72/63	–	(64)/–	(57)/73	(55)/73	–	–	(21)	(60)/78*
	IS	(57)/77	(55)/63	(45)/63	(64)/–	–	–	–	–	(21)	(60)/78*
	LSS	(57)/77	(55)/63	(45)/63	(64)/–	–	–	–	(29)	(21)	(60)/78*
CP	MSS	(48)/73	40/59	–	(54)/22	(44)/59	(46)/59	(18)	–	(18)	(49)/74
	IS	(48)	(33)	(34)	(54)/–	–	–	(18)	–	(18)	(49)
	LSS	(48)	(33)	(34)	(54)/–	–	–	(18)	–	(18)	(49)
Z	MSS	–	–	–	–	–	–	–	–	–	–
	IS	–/50	–/37	–/37	–	–	–	–	–	–	–/52
	LSS	–/50	–/37	–/37	–	–	–	–	–	–	–/52
SIO_0, SIO_3	Any	(20)	–	–	–	–	–	–	–	–	–

NOTES:

1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. An ( ) means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.
4. If two delays are given, the first is for first divide and normalization; the second is for two's complement divide and two's complement divide correction.
5. Double Length Normalize and First Divide Op
   SFA: $F = S + C_n$
   Y = Log. 2F
   Q = Log. 2Q
   $SIO_3 = F_3 \oplus R_3$(MSS)
   $C_{n+4} = F_3 \oplus F_2$ (MSS)
   $OVR = F_2 \oplus F_1$ (MSS)
   $Z = \overline{Q}_0 \overline{Q}_1 \overline{Q}_2 \overline{Q}_3 \overline{F}_0 \overline{F}_1 \overline{F}_2 \overline{F}_3$

   Two's Complement Divide
   SFC: $F = R + S + C_n$ if $Z = 0$
   $F = S - R - 1 + C_n$ if $Z = 1$
   Y = Log. 2F
   Q = Log. 2Q
   $SIO_3 = \overline{F_3 \oplus R_3}$(MSS)
   $Z = \overline{F_3 \oplus R_3}$ (MSS) from previous cycle

   Two's Complement Divide Correction and Remainder
   SFE: $F = R + S + C_n$ if $Z = 0$
   $F = S - R - 1 + C_n$ if $Z = 1$
   $Y = F$
   Q = Log. 2Q
   $Z = \overline{F_3 \oplus R_3}$(MSS) from previous cycle
6. This specification is not tested but is guranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.

IDT39C03B GUARANTEED MILITARY RANGE PERFORMANCE
SIGN MAGNITUDE TO TWO'S COMPLEMENT CONVERSION (SF5)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	92	76	–	39	85	85	(23)	–	–	100
	IS	(56)	(46)	(42)	–	–	–	(23)	–	–	(57)
	LSS	(56)	(46)	(42)	–	–	–	(23)	–	–	(57)
DA, DB	MSS	86	72	–	35	80	80	–	–	–	95
	IS	(48)	(42)	(32)	–	–	–	–	–	–	(49)
	LSS	(48)	(42)	(32)	–	–	–	–	–	–	(49)
C_n	MSS	29	(15)	–	–	28	(23)	–	–	–	(26)
	IS	(28)	(15)	–	–	–	–	–	–	–	(26)
	LSS	(28)	(15)	–	–	–	–	–	–	–	(26)
I_{8-0}	MSS	78	64	–	26	78	78	–	–	(21)	87*
	IS	78	64	58	–	–	–	–	–	(21)	87*
	LSS	78	64	58	–	–	–	–	(29)	(21)	87*
CP	MSS	86	72	–	34	80	80	(18)	–	(18)	95
	IS	(48)	(33)	(34)	–	–	–	(18)	–	(18)	(49)
	LSS	(48)	(33)	(34)	–	–	–	(18)	–	(18)	(49)
Z	MSS	–	–	–	–	–	–	–	–	–	–
	IS	52	37	32	–	–	–	–	–	–	60
	LSS	52	37	32	–	–	–	–	–	–	60
SIO_0, SIO_3	Any	(20)	–	–	–	–	–	–	–	–	–

NOTES:

1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. An ( ) means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.
4. SF5: $F = S + C_n$ if $Z = 0$
   $F = \overline{S} + C_n$ if $Z = 1$
   $Y_3 = S_3 \oplus F_3$ (MSS)
   $Z = S_3$ (MSS)
   $Y = F$
   $Q = Q$
   $N = F_3$ if $Z = 0$
   $N = F_3 \oplus S_3$ if $Z = 1$
5. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.

8

IDT39C03B GUARANTEED MILITARY RANGE PERFORMANCE
SINGLE LENGTH NORMALIZATION (SF8)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	(56)	–	–	–	–	–	(23)	–	–	(57)
	IS	(56)	(46)	(42)	–	–	–	(23)	–	–	(57)
	LSS	(56)	(46)	(42)	–	–	–	(23)	–	–	(57)
DA, DB	MSS	(48)	–	–	–	–	–	–	–	–	(49)
	IS	(48)	(42)	(32)	–	–	–	–	–	–	(49)
	LSS	(48)	(42)	(32)	–	–	–	–	–	–	(49)
C_n	MSS	(28)	–	–	–	–	–	–	–	–	(26)
	IS	(28)	(15)	–	–	–	–	–	–	–	(26)
	LSS	(28)	(15)	–	–	–	–	–	–	–	(26)
I_{8-0}	MSS	(57)	38	–	26	22	22	–	–	(21)	(60)*
	IS	(57)	(55)	(45)	26	–	–	–	–	(21)	(60)*
	LSS	(57)	(55)	(45)	26	–	–	–	(29)	(21)	(60)*
CP	MSS	(48)	25	–	23	20	25	(18)	–	(18)	(49)
	IS	(48)	(33)	(34)	23	–	–	(18)	–	(18)	(49)
	LSS	(48)	(33)	(34)	23	–	–	(18)	–	(18)	(49)
SIO_0, SIO_3	Any	(20)	–	–	–	–	–	–	–	–	–

NOTES:

1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. An ( ) means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.
4. SF8: $F = S + C_n$
   $N = Q_3$ (MSS)
   $Y = F$
   Q = LOG. $2Q$
   $C_{n+4} = Q_3 \oplus Q_2$ (MSS)
   $Z = \overline{Q_0}\,\overline{Q_1}\,\overline{Q_2}\,\overline{Q_3}$
   $OVR = Q_2 \oplus Q_1$ (MSS)

IDT39C03 INPUT/OUTPUT INTERFACE CIRCUITRY

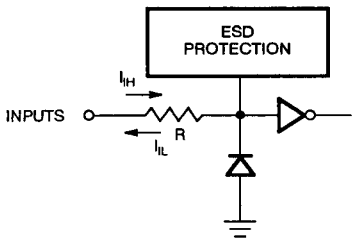


Figure 1. Input Structure (All Inputs)

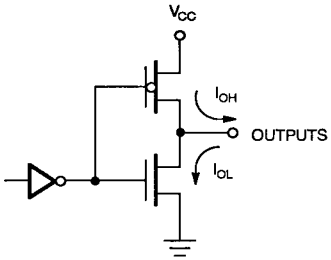


Figure 2. Output Structure (All Outputs)

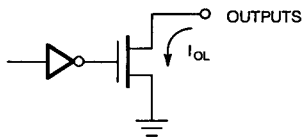
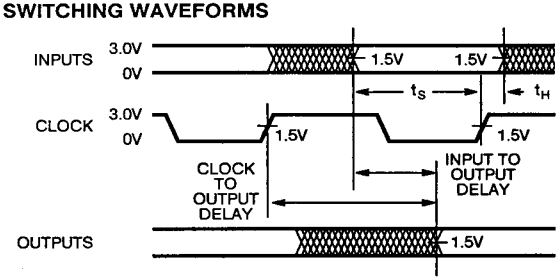


Figure 3. Open Drain Structure

AC TEST CONDITIONS

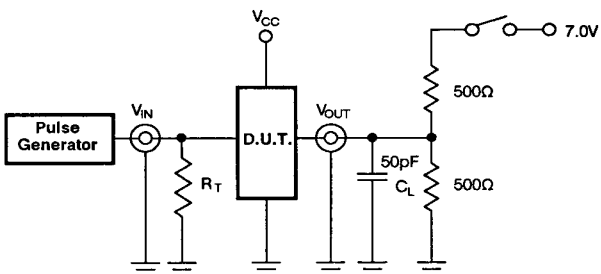
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 4

SWITCHING WAVEFORMS



8

TEST LOAD CIRCUIT



TEST	SWITCH
Open Drain Disable Low Enable Low	Closed
All other Outputs	Open

DEFINITIONS

C_L = Load capacitance: includes jig and probe capacitance

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator

Figure 4. Switching Test Circuits

ORDERING INFORMATION