Integrated Device Technology, Inc

4-BIT CMOS MICROPROGRAM SEQUENCER

IDT39C09A/B
IDT39C11A/B

MICROSLICE™ PRODUCT

FEATURES:

- Low-power CMOS
  - Commercial: 45mA (max.)
  - Military: 55mA (max.)
- Fast
  - A version meets standard speed
  - B version is 20%-50% speed upgrade
- 9-Deep stack
  - Accommodates nested loops and subroutines
- Cascadable
  - Infinitely expandable in 4-bit increments
- Available in 28-pin DIP and LCC (IDT39C09) and 20-pin DIP, LCC and SOIC (IDT39C11)
- Pin-compatible, functional enhancement for all versions of the 2909/2911
- Military product compliant to MIL-STD-883, Class B

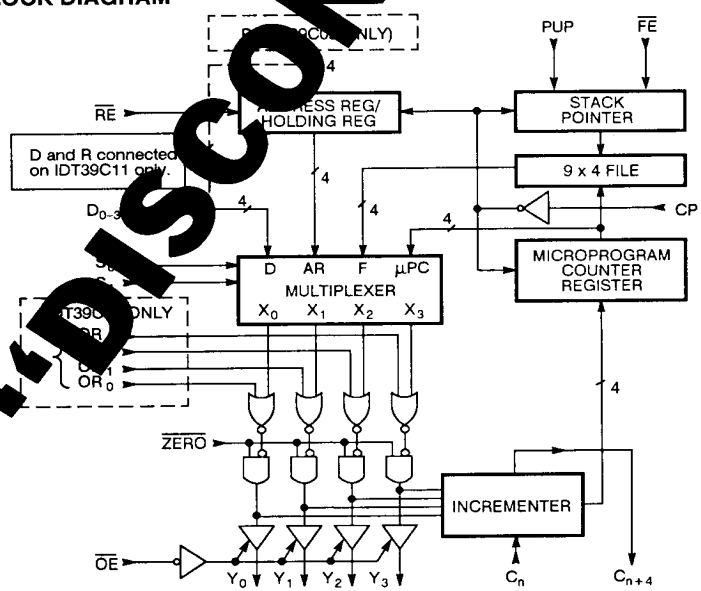
DESCRIPTION:

The IDT39C09/11 devices are high-speed, 4-bit address sequencers intended for controlling the sequence of microinstructions located in the microprogram memory. They are fully cascadable and can be expanded to any increment of 4 bits.

The IDT39C09 can select an address from any four sources: 1) external direct inputs (D); 2) external data from the R inputs, stored in an internal register; 3) 9-word deep push-pop stack; or 4) a program counter register. Also included in the stack are additional control functions which efficiently execute nested subroutine linkage. Each output can be ORed with an external input for conditional skip or branch instructions. A $\overline{ZERO}$ input line forces the outputs all zeros. All outputs are three-state and are controlled by the $\overline{OE}$ (Output Enable) pin.

The IDT39C11s operate identically to the IDT39C09s, except that the OR inputs are removed and the D and R inputs are tied together. They are fabricated using CEMOS™, CMOS technology designed for high-performance and high-reliability. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to military temperature applications demanding the highest level of performance and reliability.

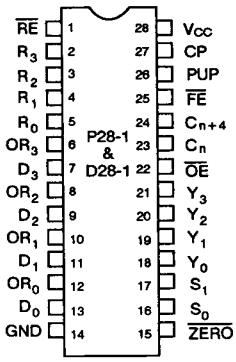
FUNCTIONAL BLOCK DIAGRAM



CEMOS and MICROSLICE are trademarks of Integrated Device Technology, Inc.

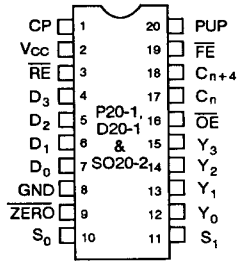
PIN CONFIGURATIONS

IDT39C09



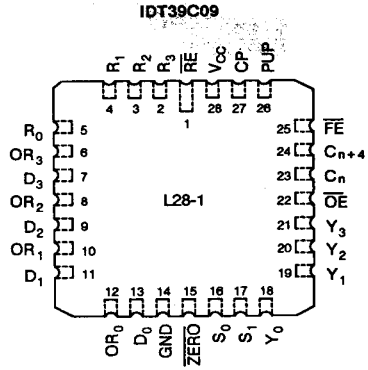
DIP
TOP VIEW

IDT39C11



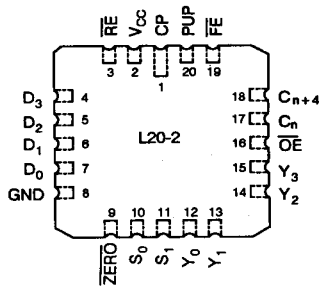
DIP/SOIC
TOP VIEW

IDT39C09



LCC
TOP VIEW

IDT39C11



LCC
TOP VIEW

PIN DESCRIPTIONS

NAME	I/O	DESCRIPTION
S_1, S_0	I	Control lines for address source selection.
$\overline{FE}$, PUP	I	Control lines for push/pop stack.
$\overline{RE}$	I	Enable line for internal address register.
OR_I	I	Logic OR inputs on each address output line. (IDT39C09 ONLY.)
$\overline{ZERO}$	I	When LOW, forces output lines to zero.
$\overline{OE}$	I	Output Enable. When $\overline{OE}$ is HIGH, the Y outputs are OFF (high impedance).
C_n	I	Carry-in to the incrementer.
R_I	I	Inputs to the internal address register. (IDT39C09 ONLY.)
D_I	I	Direct inputs to the multiplexer.
CP	I	Clock input to the AR, µPC register and Push-Pop stack.
Y_I	O	Address outputs from IDT39C09/11. (Address inputs to control memory.)
C_{n+4}	O	Carry out from the incrementer.

8

MICROPROGRAM SEQUENCER ARCHITECTURE

The IDT39C09/11's architecture consists of the following segments:

- Multiplexer
- Direct Inputs
- Address Register
- Microprogram Counter
- Stack

MULTIPLEXER

The multiplexer is controlled by the S_0 and S_1 inputs to select the address source. The two inputs control the selection of the address register, direct inputs, microprogram counter or stack as the source of the next microinstruction address.

DIRECT INPUTS

This 4-bit field of inputs (D_I) allows addresses from an external source to be output on the Y outputs. On the IDT39C11s, these inputs are also used as inputs to the register.

ADDRESS REGISTER

The Address Register (AR) consists of 4 D-type, edge-triggered flip-flops which are controlled by the Register Enable ($\overline{RE}$) input. With the address register enable LOW, new data will be entered into the register on the clock LOW-to-HIGH transition. The address register is also available as the next microinstruction address to the multiplexer.

MICROPROGRAM COUNTER

Both devices contain a microprogram counter (μPC), which consists of a 4-bit incrementer followed by a 4-bit register. The incrementer has Carry-In (C_n) and Carry-Out (C_{n+4}) for easy and simple cascading.

When the least significant carry-in to the incrementer is HIGH, the microprogram register is loaded on the next clock cycle with the current Y output word plus one ($Y + 1 \rightarrow \mu PC$). If the least significant C_n is LOW, the incrementer passes the Y output word unmodified and the microprogram register is loaded with the same Y word on the next clock cycle ($Y \rightarrow \mu PC$).

STACK

The 9-deep stack, which stores return addresses when executing microinstructions, is an input to the multiplexer. It contains a stack pointer which always points to the last word written. The added stack depth of 9 on the IDT39C09/11 allows for additional microinstruction nesting.

The stack pointer is an up/down counter controlled by File End ($\overline{FE}$) and Push/POP (PUP) inputs. When the $\overline{FE}$ input is LOW and the PUP input is HIGH, the PUSH operation is enabled. The stack pointer will then increment and the memory array is written with the microinstruction address following the subroutine jump that initiated the PUSH. A POP operation is initiated at the end of a microsubroutine to obtain the return address. A POP will occur when $\overline{FE}$ and PUP are both LOW, implying a return from a subroutine. The next LOW-to-HIGH clock transition causes the stack pointer to decrement. If the $\overline{FE}$ input is HIGH, no action is taken by the stack pointer regardless of any other input.

The $\overline{ZERO}$ is used to force the four outputs to the binary zero state. When LOW, all Y outputs are LOW regardless of any other inputs (except $\overline{OE}$). Each Y output bit also has a separate OR input such that a conditional logic one can be forced at each Y output (IDT39C09 only). This allows jumping to different microinstructions on programmed conditions.

The Output Enable ($\overline{OE}$) input controls the Y outputs. When HIGH, the outputs are programmed to a high impedance condition.

OPERATION OF THE IDT39C09/11

Figure 1 lists the select codes for the multiplexer. The two bits applied from the microword register (and additional combinational logic for branching) determine which data source contains the address for the next microinstruction. The contents of the selected source will appear on the Y outputs. Also in Figure 1 is the truth table for the output control and the push/pop stack control. S_0, S_1, $\overline{FE}$ and PUP operation is explained in Figure 2. All four define the address appearing on the Y outputs and the state of the internal registers following a clock LOW-to-HIGH transition.

The columns on the left explain the sequence of microinstructions to be executed. At address J + 2, the sequence control portion of the microinstruction contains the command "Jump to Subroutine at A". At the time T2, this instruction is in the μWR and the IDT39C09 inputs are set up to execute the jump and save the return address. The subroutine address A is applied to the D inputs from the μWR and appears on the Y outputs. The first instruction of the subroutine, I (A), is accessed and is at the inputs of the μWR. On the next clock transition, I (A) is loaded into the μWR for execution and the return address J + 3 is pushed onto the stack. The return instruction is executed at T5. Figure 4 is a similar timing chart showing one subroutine linking to a second, the latter consisting of only one microinstruction.

Figures 3 and 4 are examples of subroutine execution. The instruction being executed at any given time is the one contained in the microword register (μWR). The contents of the μWR also controls the four signals S_0, S_1, $\overline{FE}$ and PUP. The starting address of the subroutine is applied to the D inputs of the IDT39C09 at the correct time.

ADDRESS SELECTION

S_1	S_0	SOURCE FOR Y OUTPUTS	SYMBOL
L	L	Microprogram Counter	µPC
L	H	Address/Holding Register	AR
H	L	Push-Pop Stack	STK0
H	H	Direct Inputs	D_I

OUTPUT CONTROL

OR_I	$\overline{ZERO}$	$\overline{OE}$	Y_I
X	X	H	Z
X	L	L	L
H	H	L	H
L	H	L	Source selected by S_0 S_1

Z = High Impedance

SYNCHRONOUS STACK CONTROL

$\overline{FE}$	PUP	PUSH-POP STACK CHANGE
H	X	No change
L	H	Increment stack pointer, then push current PC onto STK0
L	L	Pop stack (decrement stack pointer)

H = High
L = Low
X = Don't Care

Figure 1.

CYCLE	S_0, S_1, $\overline{FE}$, PUP	µPC	REG	Y_{OUT}	COMMENT	PRINCIPAL USE
N	L L L L	J	K	J	Pop Stack	End Loop
N + 1	–	J + 1	K	–		
N	L L L H	J	K	J	Push µPC	Set-up Loop
N + 1	–	J + 1	K	–		
N	L L H X	J	K	J	Continue	Continue
N + 1	–	J + 1	K	–		
N	L H L L	J	K	K	Pop Stack; Use AR for Address	End Loop
N + 1	–	K + 1	K	–		
N	L H L H	J	K	K	Push µPC; Jump to Address in AR	JSR AR
N + 1	–	K + 1	K	–		
N	L H H X	J	K	K	Jump to Address in AR	JMP AR
N + 1	–	K + 1	K	–		
N	H L L L	J	K	Ra	Jump to Address in STK0; Pop Stack	RTS
N + 1	–	Ra + J	K	–		
N	H L L H	J	K	Ra	Jump to Address in STK0; Push µPC	
N + 1	–	Ra + 1	K	–		
N	H L H X	J	K	Ra	Jump to Address in STK0	Stack Ref (Loop)
N + 1	–	Ra + 1	K	–		
N	H H L L	J	K	D	Pop Stack; Jump to Address on D	End Loop
N + 1	–	D + 1	K	–		
N	H H L H	J	K	D	Jump to Address on D; Push µPC	JSR D
N + 1	–	D + 1	K	–		
N	H H H X	J	K	D	Jump to Address on D	JMP D
N + 1	–	D + 1	K	–		

X = Don't Care, 0 = LOW, 1 = HIGH, Assume C_N = HIGH

Figure 2. Output and Internal Next-Cycle Register States for IDT39C09/11

8

CONTROL MEMORY

EXECUTE CYCLE	MICROPROGRAM ADDRESS	MICROPROGRAM SEQUENCER INSTRUCTION
	J - 1	–
T_0	J	–
T_1	J + 1	–
T_2	J + 2	JSR A
T_6	J + 3	–
T_7	J + 4	–
	–	–
	–	–
	–	–
	–	–
	–	–
T_3	A	I (A)
T_4	A + 1	–
T_5	A + 2	RTS
	–	–
	–	–
	–	–
	–	–
	–	–
	–	–
	–	–

In the columns in figures 3 and 4, the sequence of microinstructions to be executed are shown. At address J + 2, the command "Jump to Subroutine at A" is contained in the sequence control portion of the microinstruction. At time T_2, this instruction is in the μWR and the IDT39C09 inputs are set up to execute the jump and save the return address. The subroutine address A is applied to the D inputs from the μWR and appears on the Y outputs. The first instruction of the subroutine, I (A), is accessed and is at the inputs of the μWR. On the next clock transition, I (A) is loaded into the μWR for execution and the return address J + 3 is pushed onto the stack. The return instruction is executed at T_5. Figure 4 shows a similar timing chart of one subroutine linking to a second, the latter consisting of only one microinstruction.

EXECUTE CYCLE		T_0	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9
CLOCK SIGNALS		⊓	⊓	⊓	⊓	⊓	⊓	⊓	⊓	⊓	⊓
IDT39C09/11 Inputs (from μWR)	S_1, S_0	0	0	3	0	0	2	0	0		
	$\overline{FE}$	H	H	L	H	H	L	H	H		
	PUP	X	X	H	X	X	L	X	X		
	D	X	X	A	X	X	X	X	X		
Internal Registers	μPC	J + 1	J + 2	J + 3	A + 1	A + 2	A + 3	J + 4	J + 5		
	STK0	–	–	–	J + 3	J + 3	J + 3	–	–		
	STK1	–	–	–	–	–	–	–	–		
	STK2	–	–	–	–	–	–	–	–		
	STK3	–	–	–	–	–	–	–	–		
IDT39C09/11 Output	Y	J + 1	J + 2	A	A + 1	A + 2	J + 3	J + 4	J + 5		
ROM Output	(Y)	I (J + 1)	JSR A	I (A)	I (A + 1)	RTS	I (J + 3)	I (J + 4)	I (J + 5)		
Contents of μWR (Instruction being executed)	μWR	I (J)	I (J + 1)	JSR A	I (A)	I (A + 1)	RTS	I (J + 3)	I (J + 4)		

C_n = High

Figure 3. Subroutine Execution

CONTROL MEMORY

EXECUTE CYCLE	MICROPROGRAM ADDRESS	MICROPROGRAM SEQUENCER INSTRUCTION
	J - 1	–
T_0	J	–
T_1	J + 1	–
T_2	J + 2	JSR A
T_9	J + 3	–
	–	–
	–	–
	–	–
	–	–
T_3	A	–
T_4	A + 1	–
T_5	A + 2	JSR B
T_7	A + 3	–
T_8	A + 4	RTS
	–	–
	–	–
	–	–
	–	–
T_6	B	RTS
	–	–
	–	–

EXECUTE CYCLE		T_0	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	T_9
CLOCK SIGNALS											
IDT39C09/11 Inputs (from µWR)	S_1, S_0	0	0	3	0	0	3	2	0	2	0
	$\overline{FE}$	H	H	L	H	H	L	L	H	L	H
	PUP	X	X	H	X	X	H	L	X	L	X
	D	X	X	A	X	X	B	X	X	X	X
Internal Registers	µPC	J + 1	J + 2	J + 3	A + 1	A + 2	A + 3	B + 1	A + 4	A + 5	J + 4
	STK0	–	–	–	J + 3	J + 3	J + 3	A + 3	J + 3	J + 3	–
	STK1	–	–	–	–	–	–	J + 3	–	–	–
	STK2	–	–	–	–	–	–	–	–	–	–
	STK3	–	–	–	–	–	–	–	–	–	–
IDT39C09/11 Output	Y	J + 1	J + 2	A	A + 1	A + 2	B	A + 3	A + 4	J + 3	J + 4
ROM Output	(Y)	I(J + 1)	JSR A	I(A)	I(A + 1)	JSR B	RTS	I(A + 3)	RTS	I(J + 3)	I(J + 4)
Contents of µWR (Instruction being executed)	µWR	I(J)	I(J + 1)	JSR A	I (A)	I(A + 1)	JSR B	RTS	I(A + 3)	RTS	I(J + 3)

C_n = High

Figure 4. Two Nested Subroutines. Routine B is Only One Instruction

IDT39C09/11 APPLICATIONS

The IDT39C09 and IDT39C11 are four-bit-slice sequencers which are cascaded to form a microprogram memory address generator. Both products make available to the user several lines which are used to directly control the internal holding register, multiplexer and stack. By appropriate control of these lines, the user can implement any desired set of sequence control functions; by cascading parts he can generate any desired address length. These two qualities set the IDT39C09 and IDT39C11 apart from the IDT39C10, which is architecturally similar, but is fixed at 12 bits in length and has a fixed set of 16 sequence control instructions. The IDT39C09 or IDT39C11 should be selected instead of the IDT39C10 under the following conditions: (1) address less than 8 bits and not likely to be expanded; (2) address longer than 12 bits; (3) more complex instruction set needed than is available on IDT39C10.

CONTROL UNIT ARCHITECTURE

The recommended architecture using the IDT39C09 or IDT39C11 is shown in Figure 5. The path from the pipeline register output through the next address logic, multiplexer and microprogram memory is all combinational. The pipeline register contains the current microinstruction being executed. A portion of that microinstruction consists of a sequence control command such as "continue", "loop", "return from subroutine", etc. The bits representing this sequence command are logically combined with bits representing such things as test conditions and system state to generate the required control signals to the IDT39C09 or IDT39C11.

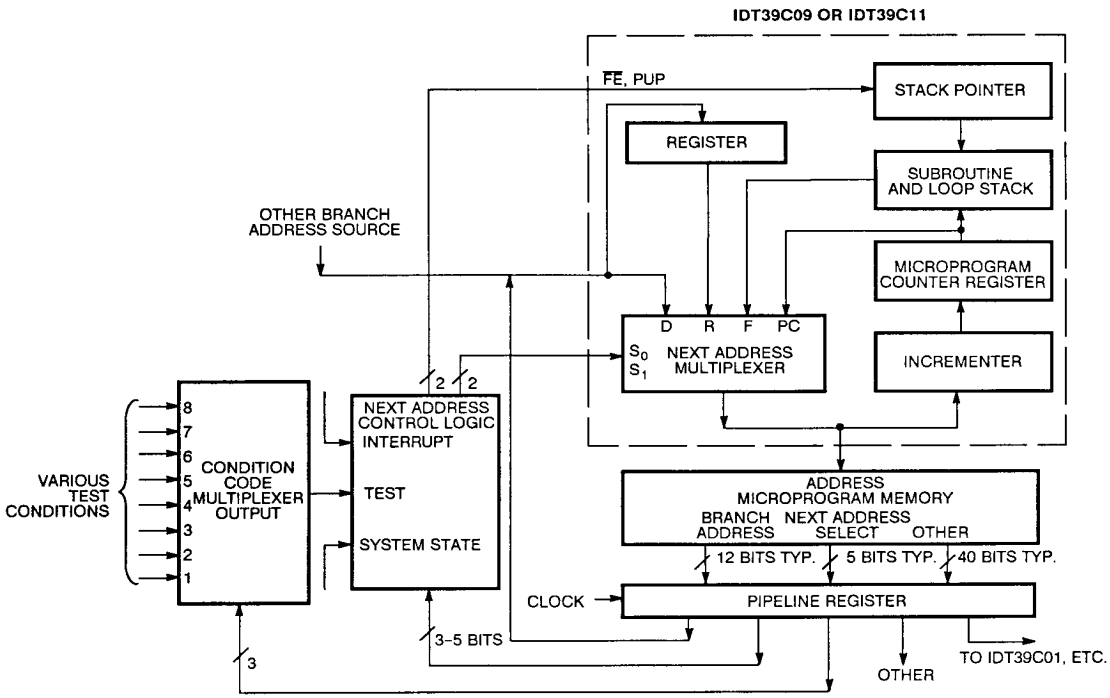


Figure 5. Recommended Computer Control Unit Architecture Using the IDT39C09A/B and IDT39C11A/B

IDT39C09/11 EXPANSION

Figure 6 shows the interconnection of three IDT39C11s to form a 12-bit sequencer. Note that the only interconnection between packages, other than the common clock and control lines, is the ripple carry between µPC incrementors. This carry path is not in the critical speed path if the IDT39C11 Y outputs drive the microprogram memory, because the ripple carry occurs in parallel with the memory access time. If, on the other hand, a microaddress register is placed at the IDT39C11 output, then the carry may lie in the critical speed path since the last carry-in must be stable for a set-up time prior to the clock.

SELECTING BETWEEN THE IDT39C09 AND IDT39C11

The difference between the IDT39C09 and the IDT39C11 involves two signals: the data inputs to the holding register and the OR inputs. In the IDT39C09, separate four-bit fields are provided for the holding register and the direct branch inputs to the multiplexer. In the IDT39C11, these fields are internally tied together. This may affect the design of the branch address system, as shown in Figure 7. Using the IDT39C09, the register inputs may be connected directly to the microprogram memory; the internal register replaces part of the pipeline register. The direct (D) inputs may be tied to the mapping logic which translates instruction op codes into microprogram addresses. While the same technique might be used with the IDT39C11, it is more common to connect the IDT39C11's D inputs to a branch address bus onto which various sources may be enabled. Shown in Figure 7 is a pipeline register and a mapping ROM. Other sources might also be applied to the same bus. The internal register is used only for temporary storage of some previous branch address.

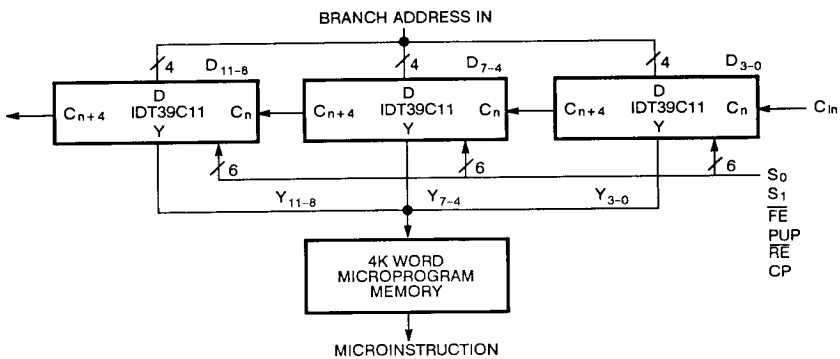


Figure 6. Twelve Bit Sequencer

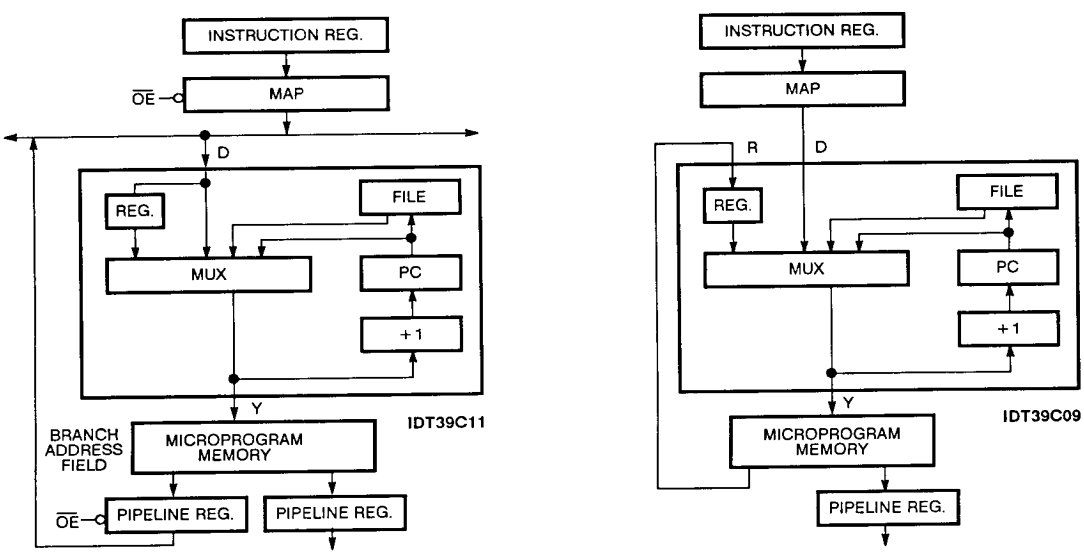


Figure 7. Branch Address Structure

The second difference between the IDT39C09 and IDT39C11 is that the IDT39C09 has OR inputs available on each address output line. These pins can be used to generate multi-way single-cycle branches by simply typing several test conditions into the OR lines (see Figure 8). Typically, a branch is taken to an address with zeros in the least significant bits. These bits are replaced with 1s or 0s by test conditions applied to the OR lines. In Figure 8, the states of the two test conditions X and Y result in a branch to 1100, 1101, 1110 or 1111.

HOW TO PERFORM COMMON FUNCTIONS WITH THE IDT39C09/11

1. CONTINUE

MUX/Y_{OUT}	STACK	C_n	S_1	S_0	$\overline{FE}$	PUP
PC	HOLD	H	L	L	H	X

Contents of PC placed on Y outputs; PC incremented.

2. BRANCH

MUX/Y_{OUT}	STACK	C_n	S_1	S_0	$\overline{FE}$	PUP
D	HOLD	H	H	H	H	X

Feed data on D inputs straight through to memory address lines.
Increment address and place in PC.

3. JUMP TO SUBROUTINE

MUX/Y_{OUT}	STACK	C_n	S_1	S_0	$\overline{FE}$	PUP
D	PUSH	H	H	H	L	H

Subroutine address fed from D inputs to memory address.
Current PC is pushed onto stack where it is saved for the return.

4. RETURN FROM SUBROUTINE

MUX/Y_{OUT}	STACK	C_n	S_1	S_0	$\overline{FE}$	PUP
STACK	POP	H	H	L	L	L

The address at the top of the stack is applied to the microprogram memory and is incremented for PC on the next cycle. The stack is popped to remove the return address.

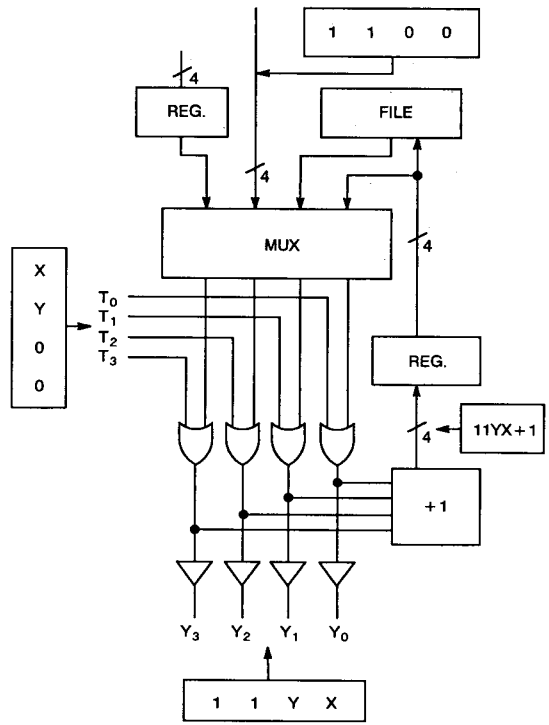


Figure 8. Use of OR Inputs to Obtain 4-Way Branch

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	30	30	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:

1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C V_{CC} = 5.0V ±5% (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ±10% (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} -0.2V

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level (4)		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level (4)		–	–	0.8	V
I_{IH}	Input High Current	V_{CC} = Max., V_{IN} = V_{CC}		–	0.1	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		–	-0.1	-5	µA
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	V
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	V
			I_{OL} = 20mA MIL.	–	0.3	0.5	
			I_{OL} = 24mA COM'L.	–	0.3	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0V	–	-0.1	-10	µA
			V_O = V_{CC} (max.)	–	0.1	10	
I_{OS}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0V (3)		-30	-50	–	mA

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. These input levels provide zero noise immunity and should only be static tested in a noise-free environment.

8

DC ELECTRICAL CHARACTERISTICS (CONT'D)

T_A = 0°C to +70°C V_{CC} = 5.0V ±5% (Commercial)
T_A = −55°C to +125°C V_{CC} = 5.0V ±10% (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} −0.2V

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQH}	Quiescent Power Supply Current CP = H (CMOS Inputs)	V_{CC} = Max. $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$ f_{CP} = 0, CP = H		—	2.5	5	mA
I_{CCQL}	Quiescent Power Supply Current CP = L (CMOS Inputs)	V_{CC} = Max. $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$ f_{CP} = 0, CP = L		—	2.5	5	mA
I_{CCT}	Quiescent Input Power Supply[5] Current (per Input @ TTL High)	V_{CC} = Max. V_{IN} = 3.4V, f_{CP} = 0		—	0.3	0.5	mA/ Input
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$ Outputs Open, $\overline{OE}$ = L	MIL.		2.0	4.0	mA/ MHz
			COM'L.		2.0	3.0	
I_{CC}	Total Power Supply Current[6]	V_{CC} = Max., f_{CP} = 10MHz Outputs Open, $\overline{OE}$ = L CP = 50% Duty cycle $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$	MIL.	—	25	45	mA
			COM'L.	—	25	35	
		V_{CC} = Max., f_{CP} = 10MHz Outputs Open, $\overline{OE}$ = L CP = 50% Duty cycle V_{IH} = 3.4V, V_{IL} = 0.4V	MIL.	—	35	55	
			COM'L.	—	35	45	

NOTES:

5. I_{CCT} is derived by measuring the total current with all the inputs tied to ...at 3.4V, subtracting out I_{CCQH}, then dividing by the total number of inputs.
6. Total Supply Current is the sum of the Quiescent current and the Dyna... ...(at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:

$I_{CC} = I_{CCQH}(CD_H) + I_{CCQL}(1 - CD_H) + I_{CCT}(N_T \times D_H) + I_{CCD}(f_{CP})$

CD_H = Clock duty cycle high period
D_H = Data duty cycle TTL high period (V_{IN} = 3.4V)
N_T = Number of dynamic inputs driven at TTL levels
f_{CP} = Clock Input frequency

CMOS TESTING CONSIDERATION

There are certain testing considerati... which ...st be taken into account when testing high-speed M... vices in an automatic environment. These are:

1) Proper decoupling at the test h... is nec...ary. Placement of the capacitor set and the value o... acitors used is critical in reducing the potential erro... fa... resulting from large V_{CC} current changes. Cap... ...d length must be short and as close to the DUT pow... ins a... ossible.
2) All input pins should b... con... to a voltage potential during testing. If left floating, t... devic... may begin to oscillate causing improper device o...ation and possible latchup.
3) Definition of input levels are very important. Since many inputs may change coincidently, significant noise at the device pins may cause the V_{IL} and V_{IH} levels not to be met until the noise has settled. To allow for this testing/board induced noise, IDT recommends using $V_{IL} \le 0V$ and $V_{IH} \ge 3V$ for AC tests.
4) Device grounding is extremely important for proper device testing. The use of multi-layer performance boards with radial decoupling between power and ground planes is required. The ground plane must be sustained from the performance board to the DUT interface board. All unused interconnect pins must be properly connected to the ground pin. Heavy gauge stranded wire should be used for power wiring and twisted pairs are recommended to minimize inductance.

IDT39C09B/IDT39C11B SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Table I, II and III below define the timing characteristics of the IDT39C09B/11B over the operating voltage and temperature ranges. The tables are divided into three types of parameters: clock characteristics, combinational delays from inputs to outputs and set-up and hold time requirements. The latter table defines the time prior to the end of the cycle (i.e., clock LOW-to-HIGH transition) that each input must be stable to guarantee that the correct data is written into one of the internal registers.

Measurements are made at 1.5V with V_{IL} = 0V and V_{IH} = 3.0V. For three-state disable tests, C_L = 5.0pF and measurement is to 0.5V change on output voltage level. All outputs have maximum DC loading.

TABLE I
CYCLE TIME AND CLOCK CHARACTERISTICS

TIME	COMMERCIAL	MILITARY
Minimum Clock LOW Time	12	12
Minimum Clock HIGH Time	12	12

TABLE II
MAXIMUM COMBINATIONAL PROPAGATION DELAYS

C_L = 50pF (except output disable test)

FROM INPUT	COMMERCIAL		MILITARY		UNIT
	Y	C_{n+4}	Y	C_{n+4}	
D_I	14	15	16	17	ns
S_0, S_1	13	15	15	17	ns
OR_I	14	14	15	15	ns
C_n	–	11	–	12	ns
$\overline{ZERO}$	14	14	15	15	ns
$\overline{OE}$ LOW (enable)	14	–	15	–	ns
$\overline{OE}$ HIGH (disable)(1)	14	–	15	–	ns
Clock ↑ $S_1 S_0$ = LH	17	17	19	19	ns
Clock ↑ $S_1 S_0$ = LL	17	17	19	19	ns
Clock ↑ $S_1 S_0$ = HL	17	17	19	19	ns

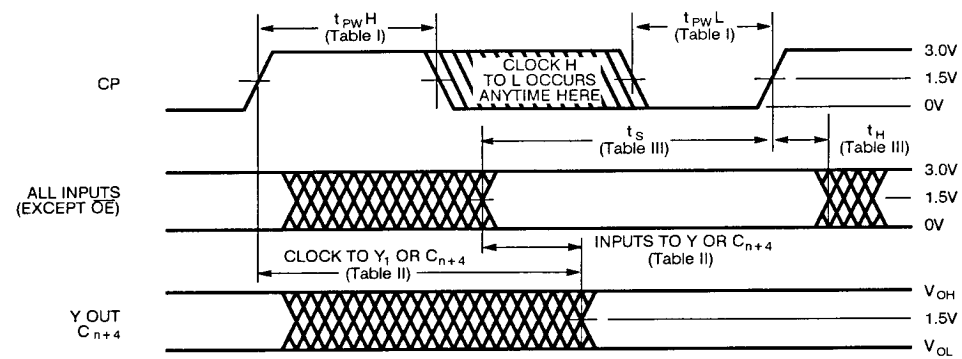
NOTE:
1. C_L = 5pF

TABLE III
GUARANTEED SET-UP AND HOLD TIMES (1)

FROM INPUT	COMMERCIAL		MILITARY		UNIT
	SET-UP TIME	HOLD TIME	SET-UP TIME	HOLD TIME	
$\overline{RE}$	6	2	7	3	ns
R_I (2)	6	2	7	3	ns
$\overline{PUP}$	9	2	10	3	ns
$\overline{FE}$	9	2	10	3	ns
C_n	6	2	7	3	ns
D_I	8	0	9	0	ns
OR_I	8	0	9	0	ns
S_0,S_1	11	0	12	0	ns
$\overline{ZERO}$	7	0	8	0	ns

NOTES:
1. All times relative to clock LOW-to-HIGH transition.
2. On IDT39C11, R_I and D_I are internally connected together and labeled D_I. Use R_I set-up and hold times when D inputs are used to load register.

8



IDT39C09A/IDT39C11A SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Table I, II and III below define the timing characteristics of the IDT39C09A/11A over the operating voltage and temperature ranges. The tables are divided into three types of parameters: clock characteristics, combinational delays from inputs to outputs and set-up and hold time requirements. The latter table defines the time prior to the end of the cycle (i.e., clock LOW-to-HIGH transition) that each input must be stable to guarantee that the correct data is written into one of the internal registers.

Measurements are made at 1.5V with V_{IL} = 0V and V_{IH} = 3.0V. For three-state disable tests, C_L = 5.0pF and measurement is to 0.5V change on output voltage level. All outputs have maximum DC loading.

TABLE I
CYCLE TIME AND CLOCK CHARACTERISTICS

TIME	COMMERCIAL	MILITARY
Minimum Clock LOW Time	20	20
Minimum Clock HIGH Time	20	20

TABLE II
MAXIMUM COMBINATIONAL PROPAGATION DELAYS

C_L = 50pF (except output disable test)

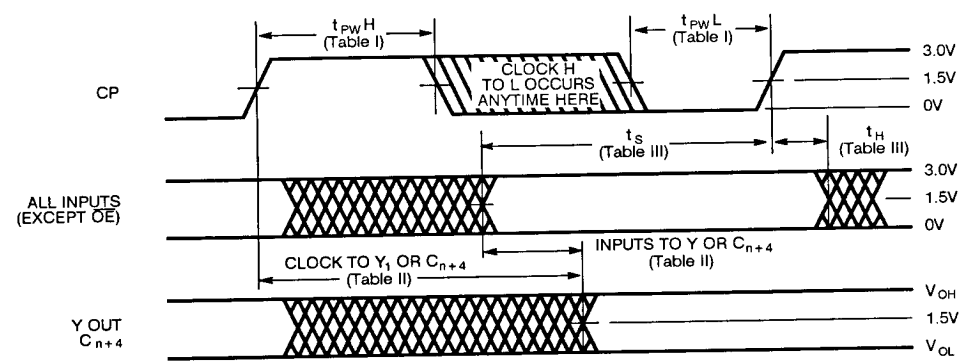
FROM INPUT	COMMERCIAL		MILITARY		UNIT
	Y	C_{n+4}	Y	C_{n+4}	
D_I	17	22	20	25	ns
S_0, S_1	29	34	29	34	ns
OR_I	17	22	20	25	ns
C_n	–	14	–	16	ns
$\overline{ZERO}$	29	34	30	35	ns
$\overline{OE}$ LOW (enable)	25	–	25	–	ns
$\overline{OE}$ HIGH (disable)(1)	25	–	25	–	ns
Clock ↑ S_1 S_0 = LH	39	44	45	50	ns
Clock ↑ S_1 S_0 = LL	39	44	45	50	ns
Clock ↑ S_1 S_0 = HL	44	49	53	58	ns

NOTE:
1. C_L = 5pF

TABLE III
GUARANTEED SET-UP AND HOLD TIMES (1)

FROM INPUT	COMMERCIAL		MILITARY		UNIT
	SET-UP TIME	HOLD TIME	SET-UP TIME	HOLD TIME	
$\overline{RE}$	19	4	19	5	ns
R_I (2)	10	4	12	5	ns
$\overline{PUP}$	25	4	27	5	ns
$\overline{FE}$	25	4	27	5	ns
C_n	18	4	18	5	ns
D_I	25	0	25	0	ns
OR_I	25	0	25	0	ns
S_0, S_1	25	0	29	0	ns
$\overline{ZERO}$	25	0	29	0	ns

NOTES:
1. All times relative to clock LOW-to-HIGH transition.
2. On IDT39C11, R_I and D_I are internally connected together and labeled D_I. Use R_I set-up and hold times when D inputs are used to load register.



TEST LOAD CIRCUIT

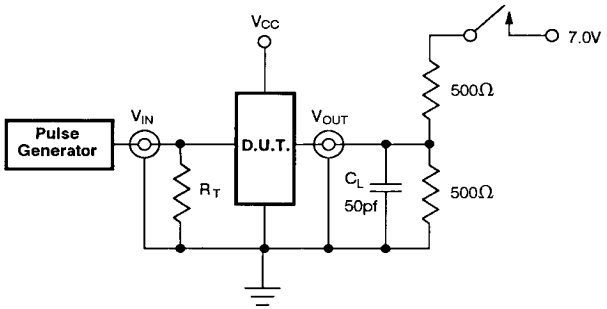


Figure 9. Switching Test Circuit (all outputs)

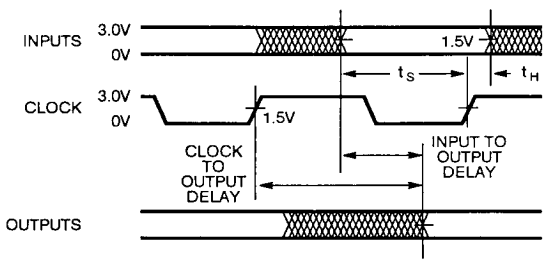
TEST	SWITCH
Open Drain Disable Low Enable Low	Closed
All other Outputs	Open

DEFINITIONS

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SWITCHING WAVEFORMS



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 9

8

INPUT/OUTPUT INTERFACE CIRCUITRY

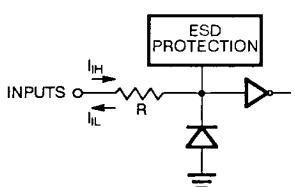


Figure 10. Input Structure

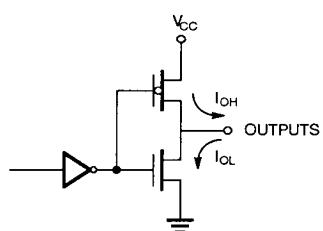


Figure 11. Output Structure

ORDERING INFORMATION