Integrated Device Technology, Inc.

4-BIT CMOS MICROPROCESSOR SLICE

IDT39C203
IDT39C203A

MICROSLICE™ PRODUCT

FEATURES:

- Fast
  - IDT39C203 matches 29203 speeds
  - IDT39C203A 20% speed upgrade
- Low-power CMOS
  - Military: 55mA (max.)
  - Commercial: 50mA (max.)
- Pin-compatible, performance-enhanced functional replacement for the 29203
- Cascadable to 8, 12, 16, etc. bits
- Infinitely expandable register file
- Improved I/O capability
  - DA, DB and Y ports are bidirectional
- Performs BCD arithmetic
  - Features automatic BCD add, subtract and conversion between binary and BCD
- On-chip parity generation and sign extension logic
- On-chip normalization logic
- On-chip multiplication division logic
- Packaged in 48-pin plastic and sidebraze DIP, 52-pin LCC
- Military product available compliant to MIL-STD-883, Class

DESCRIPTION:

The IDT39C203s are four- expandable, high-performance CMOS microprocessor slices. Along with the standard features associated with the IDT39C[illegible]d IDT39C03s, the IDT 39C203s also incorporate additio[illegible]ements for arithmetic-oriented processors.

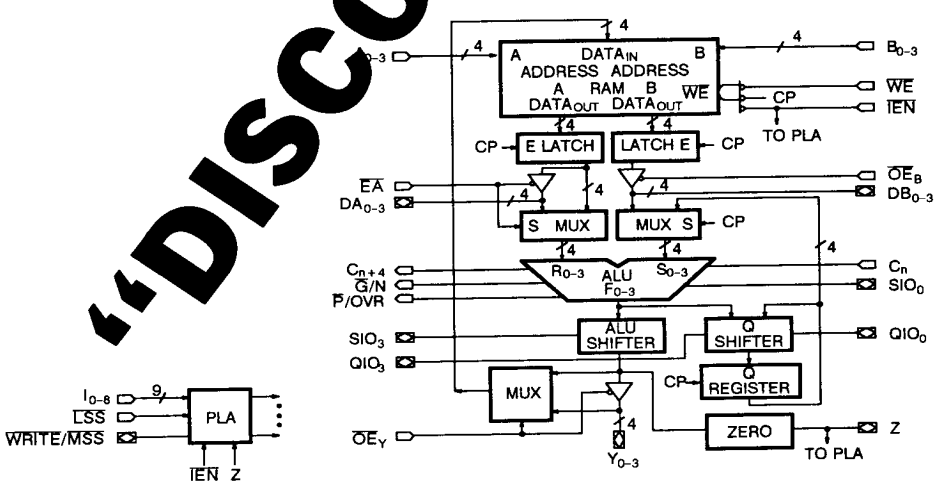
These extremely low-po[illegible]high-speed three-port three-address architectured microproc[illegible]sors consist of a 16-word by 4-bit dual-port RAM w[illegible]on both outputs, high-performance ALU and shifter, a[illegible]gister with shifter input, and nine-bit instruction de[illegible]der. A[illegible]onally, special instructions which allow the easy implen[illegible]ation of multiplication, division, normalization, BCD arith[illegible]tic an[illegible]onversion are standard on the IDT39C203s. Both devic[illegible]e e[illegible]ly expandable in 4-bit increments.

The[illegible]re p[illegible]mpatible, functional replacements for all versions of [illegible]9203. The fastest version, the IDT 39C203A, is a 20% sp[illegible] from the normal 29203 device. The IDT39C203 mee[illegible]e 29203 speeds.

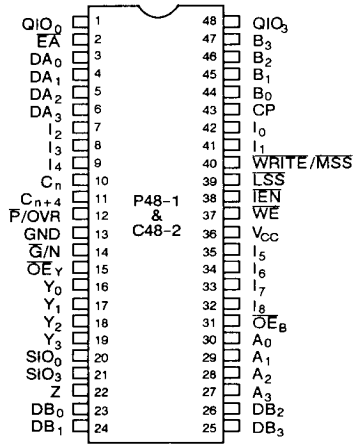
The [illegible]9C203s are fabricated using CEMOS™, CMOS technol[illegible] designed for high-performance and high-reliability.

Mi[illegible]y grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

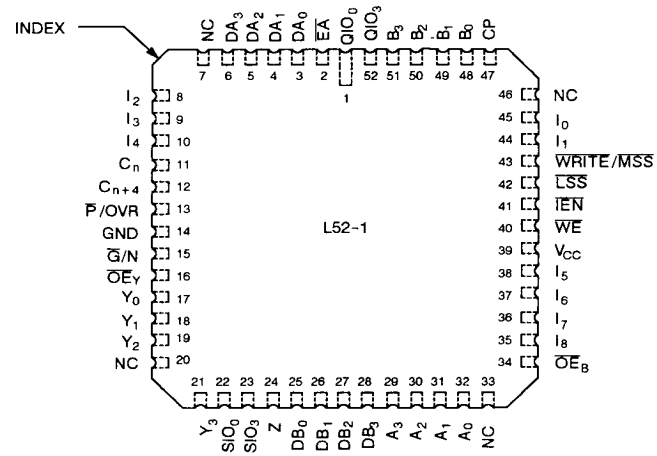
FUNCTIONAL BLOCK DIAGRAM



CEMOS and MICROSLICE are trademarks of Integrated Device Technology, Inc.



DIP
TOP VIEW



LCC
TOP VIEW

8

PIN DESCRIPTION

PIN NAME	I/O	DESCRIPTION
$A_0 - A_3$	I	Four address inputs to the RAM containing the address of the RAM word appearing at output port A.
$B_0 - B_3$	I	Four address inputs to the RAM which selects one of the words in the RAM, the contents of which is displayed through the B port. It also selects the location into which new data can be written when the $\overline{WE}$ input and CP input are low.
DA_{0-3}	I/O	Four-bit bidirectional data pins for entering external data into the ALU. The DA lines act as either RAM port A output data or as input operand R to the ALU.
DB_{0-3}	I/O	Four-bit bidirectional data pins for entering external data into the ALU. The DB lines act as either RAM port B output data or as input operand S to the ALU.
$\overline{WE}$	I	The RAM write enable input which, when LOW, causes the Y I/O port data to be written into the RAM when the CP input is low. When $\overline{WE}$ is HIGH, writing data into the RAM is inhibited.
$\overline{EA}$	I	Enable input which, when HIGH, selects DA_{0-3} as the ALU R operand and, when LOW, selects RAM output A as the ALU R operand and the DA_{0-3} output data.
$\overline{OE}_B$	I	Output enable, which, when HIGH selects DB_{0-3} as the ALU S operand, and, when LOW, selects RAM output B as the ALU S operand and the DB_{0-3} output data.
$SIO_0 - SIO_3$	I/O	Bidirectional serial shift inputs/outputs for the ALU shifter. SIO_0 is an input SIO_3 an output during a shift-up operation. SIO_3 is an input and SIO_0 an output during a shift-down operation. Refer to Tables 3 and 4 for an exact definition of of these pins.
$QIO_0 - QIO_3$	I/O	Bidirectional serial shift inputs/outputs for the ALU shifter. They operate like the SIO_0 and SIO_3 pins. Refer to Tables 3 and 4 for an exact definition of these pins.
C_n	I	Carry-in input to the ALU.
$\overline{IEN}$	I	Instruction enable input. When LOW, it enables writing into the Q register and the Sign Compare flip-flop and RAM. When HIGH, the Q register and the Sign Compare flip-flop are in hold mode. On the IDT39C203, $\overline{EIN}$ does not affect WRITE but internally disables the RAM write enable.
$\overline{LSS}$	I	Input pin, when held LOW, causes the chip to act as the Least Significant Slice ($\overline{LSS}$) of an IDT39C203 array and enables the $\overline{WRITE}$ output onto the $\overline{WRITE}/\overline{MSS}$ pin. When $\overline{LSS}$ is held HIGH, the chip acts as either an Intermediate or Most Significant Slice ($\overline{MSS}$) and the $\overline{WRITE}$ output buffer is disabled.
$\overline{WRITE}/\overline{MSS}$	I/O	The write output signal appears at this pin when $\overline{LSS}$ is held LOW. When an instruction which causes data to be written into the RAM is being executed, the $\overline{WRITE}$ signal is LOW. When $\overline{LSS}$ is HIGH, $\overline{WRITE}/\overline{MSS}$ is an input pin; holding it HIGH programs the chip to operate as an Intermediate Slice (IS) and holding it LOW programs the chip to operate as the Most Significant Slice (MSS).
C_{n+4}	O	This output indicates the carry-out of the ALU. Refer to Table 5 for an exact definition of this pin.
Z	I/O	An open collector input/out pin. When HIGH, it indicates that all outputs are LOW. Z is used as an input pin for some special functions. Refer to Table 5 for an exact definition of this pin.
$\overline{G}/N$	O	$\overline{G}$ indicates the carry generate function at the Least Significant and Intermediate slices and indicates the sign (N) of the ALU result at the Most Significant Slice. Refer to Table 5 for an exact definition of this pin.
$\overline{OE}_Y$	I	A control input pin. When LOW the ALU shifter output data is enabled onto the Y_{0-3} lines. When HIGH the Y_{0-3} three-state output buffers are disabled.
CP	I	Clock input to the IDT39C203. The Sign Compare flip-flop and the Q register are clocked on the LOW-to-HIGH transition of the CP signal. When enabled by $\overline{WE}$ and CP is LOW, data is written in the RAM.
$\overline{P}/OVR$	O	$\overline{P}$ indicates the carry propagate function at the Least Significant and Intermediate slices and indicates the conventional two's complement overflow (OVR) signal at the Most Significant Slice. Refer to Table 5 for an exact definition of this pin.
Y_{0-3}	I/O	Four data inputs/outputs of the IDT39C203. Controlled by the $\overline{OE}_Y$ input, the ALU shifter output data can be enabled onto these lines or external data is written directly into the RAM using these lines as data inputs.
I_{0-8}	I	The nine instruction inputs used to select the IDT39C203 operation to be performed.

DEVICE ARCHITECTURE

The IDT39C203 is a CMOS high-performance 4-bit microprocessor slice cascadable to any number of bits (8, 12, 16, etc.). Its versatile microinstructions allow emulation of virtually any digital computer. The ALU sources, function and destination can be selected by the 9-bit microinstruction set. Key elements which make up this 4-bit microprocessor slice are: (1) the RAM file (a 16x4 dual-port RAM) with latches on both outputs, (2) high-performance ALU with shifter, (3) a flexible Q register with shifter input and (4) a nine-bit instruction decoder.

RAM FILE

RAM data is read from the A port as controlled by the 4-bit A address field input. Simultaneously, data can be read from the B port as defined by the 4-bit B address field input. If the same address is applied at both the A input field and the B input field, identical data will appear at the two respective output ports. Data is written into the RAM when $\overline{WE}$ and $\overline{IEN}$ are both LOW and the clock CP is LOW. Both the RAM output data latches are transparent, while the clock pulse CP is HIGH and latches the data when CP is low.

New data is written into the RAM word defined by the B address field. External data at the Y I/O port can be written directly into the RAM or ALU shifter output data can be enabled onto the Y I/O port and written into the RAM. The three-state output enable $\overline{OE}_B$ allows RAM B port data to be read at the DB I/O port, while $\overline{EA}$ performs the same function for the A port data the DA I/O port.

ALU

The ALU can perform seven arithmetic and nine logic operations on the two 4-bit input words S and R. Multiplexers at the ALU inputs allow selection of various pairs of ALU source operands. The $\overline{EA}$ input selects either external DA data or RAM A-port output data as the 4-bit R source operand. The $\overline{OE}_B$ and I_0 inputs provide selection of either RAM B port output or external DB data or the Q register output as the 4-bit S source operand. Also, during certain ALU operations, zeros are forced at the ALU operand inputs. Thus, the ALU can operate on data from two external sources, from an external and an internal source or from two internal sources. Table 1 shows all possible pairs of source operands as selected by $\overline{EA}$, $\overline{OE}_B$ and I_0 inputs.

Table 1. ALU Operand Sources[1]

$\overline{EA}$	I_0	$\overline{OE}_B$	ALU OPERAND R	ALU OPERAND S
L	L	L	Ram Output A	Ram Output B
L	L	H	Ram Output A	DB_{0-3}
L	H	X	Ram Output A	Q Register
H	L	L	DA_{0-3}	Ram Output B
H	L	H	DA_{0-3}	DB_{0-3}
H	H	X	DA_{0-3}	Q Register

Note:
1. L = LOW, H = HIGH, X = DON'T CARE

The ALU performs special functions when instruction bits I_3, I_2, I_1 and I_0 are LOW. Table 4 defines these special functions and the operation which the ALU performs for each. When the ALU executes instructions other than the special functions, the operation is defined by instruction bits I_4, I_3, I_2 and I_1. Table 2 defines the operation as a function of these four instruction bits.

The IDT 39C203 may be cascaded in either a ripple carry or lookahead carry fashion. When configured as cascaded ALUs, the IDT39C203s must be programmed to be a Most Significant Slice (MSS), an Intermediate Slice (IS) or a Least Significant Slice (LSS) of the array. The carry generate ($\overline{G}$) and carry propagate ($\overline{P}$) signals that are necessary in a cascaded system are available as outputs on the IDT39C203 Least Significant and Intermediate slices.

The IDT39C203 provides a carry-out signal (C_{n+4}) which is available as an output of each slice. The carry-in (C_n) and carry-out (C_{n+4}) are both active HIGH. Two other status outputs are generated by the ALU. These are the negative (N) and the overflow (OVR). The N output indicates positive or negative results, while the OVR output indicates that the arithmetic operation performed exceeded the available two's complement range. Thus, the pins $\overline{G}$/N and $\overline{P}$/OVR indicate carry generate or propagate on the Least Significant and Intermediate slices and sign and overflow on the Most Significant Slice. Refer to Table 5 for an exact definition of these four signals.

Table 2. IDT39C203 ALU Functions[1]

I_4	I_3	I_2	I_1	I_0	ALU FUNCTIONS
L	L	L	L	L	Special Functions
L	L	L	L	H	F_i = HIGH
L	L	L	H	X	$F = S-R-1+C_n$
L	L	H	L	X	$F = R-S-1+C_n$
L	L	H	H	X	$F = R+S+C_n$
L	H	L	L	X	$F = S+C_n$
L	H	L	H	X	$F = \overline{S}+C_n$
L	H	H	L	L	Reserved Special Functions
L	H	H	L	H	$F = R+C_n$
L	H	H	H	L	Reserved Special Functions
L	H	H	H	H	$F = \overline{R}+C_n$
L	H	H	H	L	Special Functions
H	L	L	L	H	F_i = LOW
H	L	L	H	X	$F_i = \overline{Ri}$ AND S_i
H	L	H	L	X	F_i = Ri EXCLUSIVE NOR S_i
H	L	H	H	X	F_i = Ri EXCLUSIVE OR S_i
H	H	L	L	X	F_i = Ri AND S_i
H	H	L	H	X	F_i = Ri NOR S_i
H	H	H	L	X	F_i = Ri NAND S_i
H	H	H	H	X	F_i = Ri OR S_i

Note:
1. L = LOW, H = HIGH, i = 0 to 3, X = DON'T CARE

ALU SHIFTER

The ALU shifter shifts the ALU output data under instruction control. It can shift up one bit position (2F), shift down one bit position (F/2) or pass the ALU output non-shifted (F). An arithmetic shift operation shifts the data around the Most Significant (sign) Bit of the Most Significant Slice and a logical shift operation shifts the data through the Most Significant Bit. Figure 1 shows these shift patterns. The SIO_0 and SIO_3 are bidirectional serial shift input/output pins. During a shift-up operation, SIO_0 is generally an input while SIO_3 is an output; whereas, during a shift-down operation, SIO_0 is generally an output while SIO_3 acts as an input. Refer to Tables 3 and 4 for an exact definition of these pins.

The ALU shifter also provides sign extension and parity generating/checking capabilities. Under instruction control, the SIO_0 (sign) input can be extended through Y_0, Y_1, Y_2, and Y_3 and be propagated to the SIO_3 output. A cascadable, five-bit parity generator/checker generates parity for the F_0, F_1, F_2 and F_3 ALU outputs, the SIO_3 input and, under instruction control, is made

8

available at the SIO_0 output. Table 4 defines the special functions and the operation the ALU shifter performs for each instruction. For instructions other than the special functions, the ALU shifter operation is determined by instruction bits I_8, I_7, I_6 and I_5. Table 3 defines the ALU shifter operation as a function of these four bits.

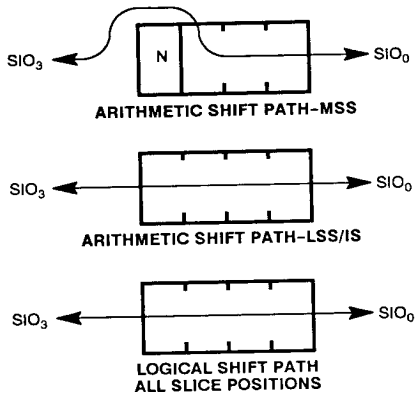


Figure 1.

Q REGISTER FILE

The Q register is a separate 4-bit file intended primarily for multiplication and division routines and can also be used as an accumulator or holding register for other types of applications. The ALU output (F) can be loaded into the Q register and/or the Q register can be selected as one of the ALU S operands. The shifter at the input to the Q register performs only logical shifts. It can shift-up the data one bit position (2Q) or down one bit position (Q/2). For a shift-up operation, QIO_0 acts as an input while QIO_3 acts as an output; whereas for a shift-down operation QIO_0 is an output and QIO_3 is an input. By connecting QIO_3 of the Most Significant Slice to SIO_0 of the Least Significant Slice, double-length arithmetic and logical shifting is possible with cascaded IDT39C203s.

Table 4 defines the special functions and the operations which the Q register and the shifter performs for selected instruction inputs. While executing instructions other than the special functions, the Q register and the shifter operation is controlled by instruction bits I_8, I_7, I_6 and I_5. Table 3 defines the Q register and shifter operation as a function of these four bits.

Table 3. ALU Destination Control for I_0 or I_1 or I_2 or I_3 = HIGH, $\overline{EN}$ = LOW (1)

I_8	I_7	I_6	I_5	HEX CODE	ALU SHIFTER FUNCTION	SIO_3 MOST SIG. SLICE	SIO_3 OTHER SLICES	Y_3 MOST SIG. SLICE	Y_3 OTHER SLICES	Y_2 MOST SIG. SLICE	Y_2 OTHER SLICES	Y_1	Y_0	SIO_0	WRITE /MSS	Q REG & SHIFTER FUNCTION	QIO_3	QIO_0
L	L	L	L	0	Arith F/2→Y	Input	Input	F_3	SIO_3	SIO_3	F_3	F_2	F_1	F_0	L	Hold	Z	Z
L	L	L	H	1	Log. F/2→Y	Input	Input	SIO_3	SIO_3	F_3	F_3	F_2	F_1	F_0	L	Hold	Z	Z
L	L	H	L	2	Arith. F/2→Y	Input	Input	F_3	SIO_3	SIO_3	F_3	F_2	F_1	F_0	L	Log. Q/2 →Q	Input	Q_0
L	L	H	H	3	Log. F/2→Y	Input	Input	SIO_3	SIO_3	F_3	F_3	F_2	F_1	F_0	L	Log. Q/2 →Q	Input	Q_0
L	H	L	L	4	F→Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	L	Hold	Z	Z
L	H	L	H	5	F→Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	H	Log. Q/2 →Q	Input	Q_0
L	H	H	L	6	F→Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	H	F→Q	Z	Z
L	H	H	H	7	F→Y	Input	Input	F_3	F_3	F_2	F_2	F_1	F_0	Parity	L	F→Q	Z	Z
H	L	L	L	8	Arith . 2F→Y	F_2	F_3	F_3	F_2	F_1	F_1	F_0	SIO_0	Input	L	Hold	Z	Z
H	L	L	H	9	Log. 2F→Y	F_3	F_3	F_2	F_2	F_1	F_1	F_0	SIO_0	Input	L	Hold	Z	Z
H	L	H	L	A	Arith. F/2→Y	F_2	F_3	F_3	F_2	F_1	F_1	F_0	SIO_0	Input	L	Log. 2Q →Q	Q_3	Input
H	L	H	H	B	Log. F/2→Y	F_3	F_3	F_2	F_2	F_1	F_1	F_0	SIO_0	Input	L	Log. 2Q →Q	Q_3	Input
H	H	L	L	C	F→Y	F_3	F_3	F_3	F_3	F_2	F_2	F_1	F_0	Z	H	Hold	Z	Z
H	H	L	H	D	F→Y	F_3	F_3	F_3	F_3	F_2	F_2	F_1	F_0	Z	H	Log. 2Q →Q	Q_3	Input
H	H	H	L	E	SIO_0→Y_0, Y_1, Y_2, Y_3	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	SIO_0	Input	L	Hold	Z	Z
H	H	H	H	F	F→Y	F_3	F_3	F_3	F_3	F_2	F_2	F_1	F_0	Z	L	Hold	Z	Z

NOTE:
1. Parity = $F_3 \oplus F_2 \oplus F_1 \oplus F_0 \oplus SIO_3$. L = LOW Z = High Impedance $\oplus$ = Exclusive OR, H = HIGH

INSTRUCTION DECODER

The internal control signals necessary for the operation of the IDT39C203 are generated by the instruction decoder as a function of the nine instruction inputs, I_{0-8}; the instruction enable input, $\overline{IEN}$; the $\overline{LSS}$ input; and the $\overline{MSS}/\overline{WRITE}$ input/output.

The $\overline{WRITE}$ output is LOW when an instruction which writes data into the RAM is executed. Refer to Tables 3 and 4 for a definition of the $\overline{WRITE}$ output as a function of the instruction inputs. When $\overline{IEN}$ is HIGH, the $\overline{WRITE}$ output is forced HIGH and the Q register and Sign Compare flip-flop contents are preserved. When $\overline{IEN}$ is LOW, the $\overline{WRITE}$ output is enabled and the Q register and Sign Compare flip-flop can be written according to the IDT39C203s instruction. The Sign Compare flip-flop shown in Figure 2 is an on-chip flip-flop which is used during a divide operation.

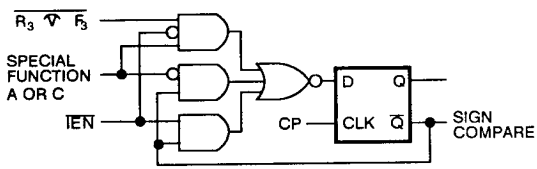


Figure 2. Sign Compare Flip-Flop

SLICE POSITION PROGRAMMING

Holding the $\overline{LSS}$ pin LOW programs the IDT39C203 slice (LSS) and enables the $\overline{WRITE}$ output signal onto the $\overline{MSS}/\overline{WRITE}$ I/O pin. When $\overline{LSS}$ is tied HIGH, the $\overline{MSS}/\overline{WRITE}$ pin becomes an input tying $\overline{MSS}/\overline{WRITE}$ LOW programs the slice to operate as the Most Significant Slice (MSS); tying it HIGH causes the slice to operate as an Intermediate Slice. The $\overline{MSS}/\overline{WRITE}$ pin should be tied HIGH through a resistor, independent of the LSS pin.

SPECIAL FUNCTIONS

Sixteen special functions are provided on the IDT39C203 which permit the implementation of the following operations:

- Single and double length normalization
- Two's complement division
- Unsigned and two's complement multiplication
- Conversion between two's complement and sign/magnitude representation
- Incrementation and decrementation by one or two
- BCD add, subtract, and divide by two
- Single and double-precision BCD-to binary and binary-to-BCD conversion

Adjusting a single-precision or double-precision floating-point number in order to bring its mantissa within a specified range can be performed using the single-length and double-length normalization operations. Three special functions can be used to perform a two's complement, non-restoring divide operation. They provide single and double-precision divide operations and can be performed in "n" clock cycles (where "n" is the number of bits in the quotient).

The unsigned multiply special function and the two two's complement multiply special functions can be used to multiply two n-bit, unsigned or two's complement numbers, respectively, in "n" clock cycles. During the last cycle of the two's complement multiplication, a conditional subtraction, rather than addition, is performed due to the fact that the sign bit of the multiplier carries negative weight.

The sign/magnitude two's complement special function can be used to convert number representation systems. A number expressed in sign/magnitude representation can be converted to the two's complement representation, and vice-versa, in one clock cycle. Incrementing an unsigned or two's complement number by one or two is easily accomplished using the increment by one or two special functions.

In addition to BCD arithmetic special functions to add or subtract two BCD numbers, a BCD divide by two adjust instructions can be used to obtain a valid BCD representation after shifting a number down by one bit. The BCD/binary conversion special function instructions permit single and double-precision algorithms to convert from BCD-to-binary and from binary-to-BCD.

8

Table 4. Special Functions [7,8]

HEX $I_8 I_7 I_6 I_5$	I_4	HEX $I_3 I_2 I_1 I_0$	SPECIAL FUNCTION	ALU FUNCTION	ALU SHIFTER FUNCTION	SIO_3 MSS	SIO_3 OTHER SLICES	SIO_0	Q REGISTER & SHIFTER FUNCTION	QIO_3	QIO_0	$\overline{WRITE}$ /MSS
0	L	0	Unsigned Multiply	$F=S+C_n$ if $Z=L$ $F=R+S+C_n$ if $Z=H$	Log F/2→Y [1]	X	Input	F_0	Log Q/2 →Q	Input	Q_0	L
1	L	0	BCD to Binary Conversion	Note 4	Log F/2→Y	Input	Input	F_0	Log Q/2 →Q	Input	Q_0	L
1	H	0	Multiprecision BCD to Binary	Note 4	Log F/2→Y	Input	Input	F_0	Hold	X	Q_0	L
2	L	0	Two's Complement Multiply	$F=S+C_n$ if $Z=L$ $F=R+S+C_n$ if $Z=H$	Log F/2→Y [2]	X	Input	F_0	Log Q/2 →Q	Input	Q_0	L
3	L	0	Decrement by One or Two	$F=S-2+C_n$	F→Y	Input	Input	Parity	Hold	X	X	L
4	L	0	Increment by One or Two	$F=S+1+C_n$	F→Y	Input	Input	Parity	Hold	X	X	L
5	L	0	Sign/Magnitude Two's Complement	$F=S+C_n$ if $Z=L$ $F=S+C_n$ if $Z=H$	F→Y [3]	Input	Input	Parity	Hold	X	X	L
6	L	0	Two's Complement Multiply, Last Cycle	$F=S+C_n$ if $Z=L$ $F=S-R-1+C_n$ if $Z=H$	L F/2→Y [2]	X	Input	F_0	Log Q/2 →Q	Input	Q_0	L
7	L	0	BCD Divide by Two	Note 4	F→Y	Input	Input	Parity	Hold	X	X	L
8	L	0	Single Length Normalize	$F=S+C_n$	F→Y	F_3	F_3	X	Log 2Q →Q	Q_3	Input	L
9	L	0	Binary to BCD Conversion	Note 5	Log 2F→Y	F_3	F_3	Input	Log 2Q →Q	Q_3	Input	L
9	H	0	Multiprecision Binary to BCD	Note 5	Log 2F→Y	F_3	F_3	Input	Hold	X	Input	L
A	L	0	Double Length Normalize and First Divide Op	$F=S+C_n$	Log 2F→Y	$R_3 \oplus F_3$	F_3	Input	Log 2Q →Q	Q_3	Input	L
B	L	0	BCD Add	$F=R+S+C_n$ BCD [6]	F→Y	0	0	X	Hold	X	X	L
C	L	0	Two's Complement Divide	$F=S+R+C_n$ if $Z=L$ $F=S-R-1+C_n$ if $Z=H$	Log 2F→Y	$R_3 \oplus F$	F_3	Input	Log 2Q →Q	Q_3	Input	L
D	L	0	BCD Subtract	$F=R-S-1+C_n$ BCD [6]	F→Y	0	0	X	Hold	X	X	L
E	L	0	Two's Complement Divide Correction and Remainder	$F=S+R+C_n$ if $Z=L$ $F=S-R-1+C_n$ if $Z=H$	F→Y	F_3	F_3	X	Log 2Q →Q	Q_3	Input	L
F	L	0	BCD Subtract	$F=S-R-1+C_n$ BCD [6]	F→Y	0	0	X	Hold	X	X	L

NOTES:

1. At the Most Significant Slice only, the C_{n+4} signal is internally gated to the Y_3 output.
2. At the Most Significant Slice only, $F_3 \oplus$ OVR is internally gated to the Y_3 output.
3. At the Most Significant Slice only, $S_3 \oplus F_3$ is generated the Y_3 output.
4. On each slice, F = S if magnitude of S_{0-3} is less than 8, and F = S minus three if magnitude of S_{0-3} is 8 or greater.
5. On each slice, F = S if magnitude of S_{0-3} is less than 5, and F = S plus three if magnitude of S_{0-3} is 5 or greater. Addition is modulo 16.
6. Additions and Subtractions are BCD adds and subtracts. Results are undefined if R or S are not in valid BCD format.
7. The Q register cannot be used explicitly as an operand for any special functions. It is defined implicitly within the functions.
8. L = LOW, H = HIGH, X = Don't Care, $\oplus$ = Exclusive OR, PARITY = $SIO_3 \oplus F_3 \oplus F_2 \oplus F_1 \oplus F_0$

Table 5. IDT39C203 Status Outputs

(HEX) I_{8-5}	(HEX) I_{4-1}	I_0	Gi (i = 0 to 3)	Pi (i = 0 to 3)	C_{n+4}	$\overline{P}$/OVR		$\overline{G}$/N		Z ($\overline{OE}_Y$ = L)		
						MOST SIG. SLICE	OTHER SLICES	MOST SIG. SLICE	OTHER SLICES	MOST SIG. SLICE	INTER-MEDIATE SLICE	LEAST SIG. SLICE
X	0	H	0	1	0	0	0	F_3	G	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	1	X	$\overline{R}_i \wedge S_i$	$\overline{R}_i \vee S_i$	G V PC_n	$C_{n+3} \vee C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	2	X	$R_i \wedge \overline{S}_i$	$R_i \vee \overline{S}_i$	G V PC_n	$C_{n+3} \vee C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	3	X	$R_i \wedge S_i$	$R_i \vee S_i$	G V PC_n	$C_{n+3} \vee C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	4	X	0	S_i	G V PC_n	$C_{n+3} \vee C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	5	X	0	$\overline{S}_i$	G V PC_n	$C_{n+3} \vee C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	6	H	0	R_i	G V PC_n	$C_{n+3} \vee C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	7	H	0	$\overline{R}_i$	G V PC_n	$C_{n+3} \vee C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	8	H	0	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	9	X	$\overline{R}_i \wedge S_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	A	X	$R_i \wedge S_i$	$R_i \vee S_i$	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	B	X	$\overline{R}_i \wedge S_i$	$R_i \vee S_i$	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	C	X	$R_i \wedge S_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	D	X	$\overline{R}_i \wedge \overline{S}_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	E	X	$R_i \wedge S_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
X	F	X	$\overline{R}_i \wedge \overline{S}_i$	1	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
0	0	L	0 if Z = L $R_i \wedge S_i$ if Z = H	S_i if Z = L $R_i \vee S_i$ if Z = H	G V PC_n	$C_{n+3} \vee C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Input	Input	Q_0
1	0	L	0	S_i	G V PC_n	$C_{n+3} \vee C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
1	8	L	0	S_i	0	0	0	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
2	0	L	0 if Z = L $R_i \wedge S_i$ if Z = H	S_i if Z = L $R_i \vee S_i$ if Z = H	G V PC_n	$C_{n+3} \vee C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Input	Input	Q_0
3	0	L	Note 6	Note 7	G V PC_n	$C_{n+3} \vee C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
4	0	L	Note 1	Note 2	G V PC_n	$C_{n+3} \vee C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
5	0	L	0	S_i if Z = L S_i if Z = H	G V PC_n	$C_{n+3} \vee C_{n+4}$	$\overline{P}$	F_3 if Z = L $F_3 \vee S_3$ if Z = H	$\overline{G}$	S_3	Input	Input
6	0	L	0 if Z = L $\overline{R}_i \wedge S_i$ if Z = H	S_i if Z = L $R_i \vee S_i$ if Z = H	G V PC_n	$C_{n+3} \vee C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Input	Input	Q_0
7	0	L	0	S_i	G V PC_n	$C_{n+3} \vee C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
8	0	L	0	S_i	Note 3	$Q_2 \vee Q_1$	$\overline{P}$	Q_3	$\overline{G}$	$\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$	$\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$	$\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$
9	0	L	0	S_i	G V PC_n	$C_{n+3} \vee C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$	$\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$	$\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$
9	8	L	0	S_i	0	0	0	F_3	$\overline{G}$	$\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$	$\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$	$\overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$
A	0	L	0	S_i	Note 4	$F_2 \vee F_1$	$\overline{P}$	F_3	$\overline{G}$	Note 5	Note 5	Note 5
B	0	L	$R_i \wedge S_i$	$R_i \vee S_i$	G V PC_n	Note 8	Note 8	Note 9	Note 9	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
C	0	L	$R_i \wedge S_i$ if Z = L $\overline{R}_i \wedge S_i$ if Z = H	$R_i \vee S_i$ if Z = L $\overline{R}_i \vee S_i$ if Z = H	G V PC_n	$C_{n+3} \vee C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Sign Compare FF Output	Input	Input
D	0	L	$R_i \wedge \overline{S}_i$	$R_i \vee \overline{S}_i$	G V PC_n	$C_{n+3} \vee C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$
E	0	L	$R_i \wedge S_i$ if Z = L $\overline{R}_i \wedge S_i$ Z = H	$R_i \vee S_i$ if Z = L $\overline{R}_i \vee S_i$ Z = H	G V PC_n	$C_{n+3} \vee C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	Sign Compare FF Output	Input	Input
F	0	L	$\overline{R}_i \wedge S_i$	$\overline{R}_i \vee S_i$	G V PC_n	$C_{n+3} \vee C_{n+4}$	$\overline{P}$	F_3	$\overline{G}$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$	$\overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3$

Notes on next page

8

NOTES:

1. If $\overline{LSS}$ is LOW, $G_0 = S_0$ and $G_{1,2,3} = 0$. If $\overline{LSS}$ is HIGH, $G_{0,1,2,3} = 0$.
2. If $\overline{LSS}$ is LOW, $P_0 = 1$ and $P_{1,2,3} = S_{1,2,3}$. If $\overline{LSS}$ is HIGH, $P_I = S_I$.
3. At the most significant slice, $C_{n+4} = Q_3 \forall Q_2$. At other slices $C_{n+4} = G \vee PC_n$.
4. At the most significant slice, $C_{n+4} = F_3 \forall F_2$. At other slices $C_{n+4} = G \vee PC_n$.
5. $Z = \overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3\,\overline{F}_0\overline{F}_1\overline{F}_2\overline{F}_3$.
6. If $\overline{LSS}$ is LOW, $G_0 = 0$ and $G_{1,2,3} = S_{1,2,3}$. If $\overline{LSS}$ is HIGH, $G_{0,1,2,3} = S_{0,1,2,3}$.
7. If $\overline{LSS}$ is LOW, $P_0 = S$ and $P_{1,2,3} = S$. If $\overline{LSS}$ is HIGH, $P_{0,1,2,3} = 1$.
8. On all slices $\overline{P} = (\overline{P}_0 + \overline{P}_3)(\overline{P}_0 + \overline{P}_2)(\overline{P}_0 + \overline{G}_1 + \overline{P}_2)$.
9. On all slices $\overline{G} = \overline{G}_3(\overline{G}_0 + \overline{G}_1 + \overline{P}_2)(\overline{G}_0 + \overline{G}_1)(\overline{P}_1 + \overline{G}_2)(\overline{P}_3 + \overline{P}_1 \bullet \overline{P}_2 \bullet \overline{G}_0)$.
10. L = LOW = 0, H = HIGH = 1, V = OR, $\wedge$ = AND, $\forall$ = EXCLUSIVE OR, $P = P_3P_2P_1P_0$, $G = G_3 \vee G_2P_3 \vee G_1P_2P_3 \vee G_1P_1P_2P_3$, $C_{n+3} = G_2 \vee G_1P_2 \vee G_0P_1P_2 \vee C_nP_0P_1P_2 \vee C_nP_0P_1P_2$

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 5%

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:

1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level (4)		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level (4)		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		–	0.1	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		–	-0.1	-5	µA
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	V
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	V
			I_{OL} = 20mA MIL.	–	0.3	0.5	
			I_{OL} = 24mA COM'L.	–	0.3	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0V	–	-0.1	-10	µA
			V_O = V_{CC}	–	0.1	10	
I_{OS}	Output Short Circuit Current	V_{CC} = Min., V_{OUT} = 0V (3)		-30	–	–	mA
I_{CCQH}	Quiescent Power Supply Current CP = H (CMOS Inputs)	V_{CC} = Max. $V_{HC} \leq V_{IN}$, $V_{IN} \leq V_{LC}$ f_{CP} = 0, $\overline{CP}$ = H		–	5	15	mA
I_{CCQL}	Quiescent Power Supply Current CP = L (CMOS Inputs)	V_{CC} = Max. $V_{HC} \leq V_{IN}$, $V_{IN} \leq V_{LC}$ f_{CP} = 0, $\overline{CP}$ = L		–	5	15	mA
I_{CCT}	Quiescent Input Power Supply (5) Current (per Input @ TTL High)	V_{CC} = Max. V_{IN} = 3.4V, f_{CP} = 0		–	0.25	0.5	mA/ Input
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. $V_{HC} \leq V_{IN}$, $V_{IN} \leq V_{LC}$ Outputs Open, $\overline{OE}$ = L	MIL.	–	0.5	2.0	mA/ MHZ
			COM'L.	–	0.5	1.5	
I_{CC}	Total Power Supply Current(6)	V_{CC} = Max., f_{CP} = 10MHz Outputs Open, $\overline{OE}$ = L CP = 50% Duty cycle $V_{HC} \leq V_{IN}$, $V_{IN} \leq V_{LC}$	MIL.	–	10	35	mA
			COM'L.	–	10	30	
		V_{CC} = Max., f_{CP} = 10MHz Outputs Open, $\overline{OE}$ = L CP = 50% Duty cycle V_{IH} = 3.4V, V_{IL} = 0.4V	MIL.	–	20	55	
			COM'L.	–	20	50	

NOTES:

1. For conditions shown as max. or min. use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. These input levels provide zero noise immunity and should only be static tested in a noise-free environment.
5. I_{CCT} is derived by measuring the total current with all the inputs tied together at 3.4V, subtracting out I_{CCQH}, then dividing by the total number of inputs.
6. Total Supply Current is the sum of the Quiescent current and the Dynamic current (at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:

$$I_{CC} = I_{CCQH}(CD_H) + I_{CCQL}(1 - CD_H) + I_{CCT}(N_T \times D_H) + I_{CCD}(f_{CP})$$

CD_H = Clock duty cycle high period.
D_H = Data duty cycle TTL high period (V_{IN} = 3.4V).
N_T = Number of dynamic inputs driven at TTL levels.
f_{CP} = Clock input frequency.

8

IDT39C203A GUARANTEED COMMERCIAL RANGE PERFORMANCE

The tables below specify the guaranteed performance of the IDT39C203A over the commercial operating range of 0 to +70°C with V_{CC} from 4.75 to 5.25V. All data are in nanoseconds, with inputs switching between 0 and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

Table 12. Clock and Write Pulse Characteristics All Functions

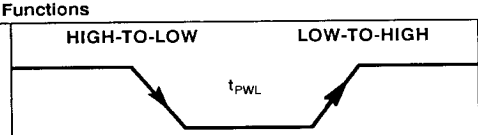
Minimum Clock Low Time	24ns
Minimum Clock High Time	24ns
Minimum Time CP and $\overline{WE}$ both Low to Write	12ns

Table 13. Enable/Disable Times All Functions (1)

FROM	TO	ENABLE	DISABLE
$\overline{OE}_Y$	Y	20	17
$\overline{OE}_B$	DB	20	17
$\overline{EA}$	DA	20	17
I_8	SIO	20	17
I_8	QIO	30	30
$I_{8,7,6,5}$	QIO	30	30
$I_{4,3,2,1,0}$	QIO	30	28
$\overline{LSS}$	$\overline{WRITE}$	20	17

NOTE:
1. C_L = 5.0pF for output disable tests. Measurement is made to a 0.5V change on the output.

Table 14. Set-up and Hold Times All Functions



FROM	WITH RESPECT TO	SET-UP	HOLD	SET-UP	HOLD	COMMENTS
Y	CP	Don't Care	Don't Care	11	3	Store Y in RAM/Q (1)
$\overline{WE}$ HIGH	CP	12	T_{PWL}		0	Prevent Writing
$\overline{WE}$ LOW	CP	Don't Care	Don't Care	12	0	Write into RAM
A, B Source	CP	16	3	Don't Care	Don't Care	Latch Data from RAM Out
B Destination	CP	5	T_{PWL}		3	Write Data into B Address
$QIO_{0,3}$	CP	Don't Care	Don't Care	14	3	Shift Q
$I_{8,7,6,5}$	CP	10	–	16	0	Write into Q (2)
$\overline{IEN}$ HIGH	CP	19	T_{PWL}		0	Prevent Writing into Q
$\overline{IEN}$ LOW	CP	Don't Care	Don't Care	17	0	Write into Q
$I_{4,3,2,1,0}$	CP	14	–	26	0	Write into Q (2)

NOTES:
1. The internal Y-bus to RAM set-up condition will be met 5ns after valid Y output ($\overline{OE}_Y$ = L)
2. The set-up time with respect to CP falling edge is to prevent writing. The set-up time with respect to CP rising edge is to enable writing.
3. For all other set-up conditions not specified in this table, the set-up time should be the delay to stable Y output plus the Y to RAM internal set-up time. Even if the RAM is not being loaded, this set-up condition ensures valid writing into the Q register and sign compare flip-flop.
4. $\overline{WE}$ controls writing into the RAM. IEN controls writing into Q and, indirectly, controls $\overline{WE}$ through the $\overline{WRITE}/\overline{MSS}$ output. To prevent writing, $\overline{IEN}$ and $\overline{WE}$ must go HIGH during the entire clock LOW time. They may go LOW after the clock has gone LOW to cause a write, provided the $\overline{WE}$ LOW and $\overline{IEN}$ LOW set-up times are met. Having gone LOW, they should not be returned HIGH until after the clock has gone HIGH.
5. A and B addresses must be set up prior to the clock HIGH-TO-LOW transition to latch data at the RAM output.
6. Writing occurs when CP and $\overline{WE}$ are both LOW. The B address should be stable during this entire period.
7. Because $I_{8,7,6,5}$ controls the writing or not writing of data into RAM and Q, they should be stable during the entire clock LOW time unless $\overline{IEN}$ is HIGH, which prevents writing.
8. The set-up time prior to the clock LOW-TO-HIGH transition occurs in parallel with the set-up time prior to the clock HIGH-TO-LOW transition and the clock LOW time. The actual set-up time requirement on $I_{4,3,2,1,0}$ relative to the clock LOW-TO-HIGH transition is the longer of (1) the set-up time prior to clock L ⟶ H and (2) the sum of the set-up time prior to clock H ⟶ L and the clock LOW time.

IDT39C203A GUARANTEED COMMERCIAL RANGE PERFORMANCE
STANDARD FUNCTIONS AND INCREMENT/DECREMENT BY ONE OR TWO INSTRUCTIONS (SF3, SF4)

FROM	TO											
	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DA, DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_0	SIO_3	SIO_0 PARITY
A, B Addr	54	44	42	59	49	54	22	–	–	33	50	62
DA, DB	46	40	32	52	43	46	–	–	–	28	47	52
C_n	26	14	–	28	22	22	–	–	–	18	24	30
I_{8-0}	51	51	40	58	49	50	–	27	21	40	50	59
CP	46	34	34	49	43	46	18	–	18	30	43	48
SIO_0, SIO_3	18	–	–	23	–	–	–	–	–	–	23	15
$\overline{MSS}$	35	–	35	35	35	35	–	–	–	–	35	–
$\overline{EA}$	46	40	32	52	43	46	–	–	–	28	47	52

NOTES:
1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output..
3. Standard Functions: See Table 2, Increment SF4: $F = S + 1 + C_n$ and Decrement SFD: $F = S - 2 + C_n$

MULTIPLY INSTRUCTIONS (SF0, SF2, SF6)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DA, DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_0
A, B Addr	MSS	(54)	(44)	–	–	(49)	(54)	(22)	–	–	(33)
	IS	(54)	(44)	(42)	–	–	–	(22)	–	–	(33)
	LSS	(54)	(44)	(42)	–	–	–	(22)	–	–	(33)
DA, DB	MSS	(46)	(40)	–	–	(43)	(46)	–	–	–	(28)
	IS	(46)	(40)	(32)	–	–	–	–	–	–	(28)
	LSS	(46)	(40)	(32)	–	–	–	–	–	–	(28)
C_n	MSS	28	(14)	–	–	(22)	(22)	–	–	–	(18)
	IS	(26)	(14)	–	–	–	–	–	–	–	(18)
	LSS	(26)	(14)	–	–	–	–	–	–	–	(18)
I_{8-0}	MSS	75	60	–	–	70	70	–	–	(21)	58
	IS	75	60	57	–	–	–	–	–	(21)	58
	LSS	75	60	57	24	–	–	–	(27)	(21)	58
CP	MSS	(46)	(34)	–	–	(43)	(46)	(18)	–	(18)	(30)
	IS	(46)	(34)	(34)	–	–	–	(18)	–	(18)	(30)
	LSS	75	60	57	24	–	–	(18)	–	(18)	58
Z	MSS	51	36	–	–	46	46	–	–	–	34
	IS	51	36	33	–	–	–	–	–	–	34
	LSS	–	–	–	–	–	–	–	–	–	–
SIO_0, SIO_3	Any	(18)	–	–	–	–	–	–	–	–	–

NOTES:
1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. A number is parentheses means the delay path is the same as specified in the Standard Functions and Increment by One or Two Instructions Table. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.
4. Unsigned Multiply
   SF0: $F = S + C_n$ if $Z = 0$
   $F = S + R + C_n$ if $Z = 1$
   Y = Log. F/2
   Q = Log. Q/2
   $Y_3 = C_{n+4}$ (MSS)
   $Z = Q_0$ (LSS)

   Two's Complement Multiply
   SF2: $F = S + C_n$ if $Z = 0$
   $F = R + S + C_n$ if $Z = 1$
   Y = Log. F/2
   Q = Log. Q/2
   $Y_3 = F_3 \oplus$ OVR (MSS)
   $Z = Q_0$ (LSS)

   Two's Complement Multiply Last Cycle
   SF6: $F = S + C_n$ if $Z = 0$
   $F = S - R - 1 + C_n$ if $Z = 1$
   Y = Log. F/2
   Q = Log. Q/2
   Y_3 = OVR $\oplus$ F_3 (MSS)
   $Z = Q_0$ (LSS)

8

IDT39C203A GUARANTEED COMMERCIAL RANGE PERFORMANCE DIVIDE INSTRUCTIONS (SFA, SFC, SFE)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DA, DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	(54)	49/(44)	–	(59)/–	(49)	(54)	(22)	–	–	(50)
	IS	(54)	(44)	(42)	(59)/–	–	–	(22)	–	–	(50)
	LSS	(54)	(44)	(42)	(59)/–	–	–	(22)	–	–	(50)
DA, DB	MSS	(46)	44/40	–	(52)/–	(43)	(46)	–	–	–	(47)
	IS	(46)	(40)	(32)	(52)/–	–	–	–	–	–	(47)
	LSS	(46)	(40)	(32)	(52)/–	–	–	–	–	–	(47)
C_n	MSS	(26)	26/(14)	–	(28)/–	(22)	(22)	–	–	–	26
	IS	(26)	(14)	–	(28)/–	–	–	–	–	–	(24)
	LSS	(26)	(14)	–	(28)/–	–	–	–	–	–	(24)
I_{8-0}	MSS	(51)/67	60/54	–	(58)/23	(49)/62	(50)/62	–	–	(21)	(50)/66
	IS	(51)/67	(51)/54	(40)/(56)	(58)/–	–	–	–	–	(21)	(50)/66
	LSS	(51)/67	(51)/54	(40)/(56)	(58)/–	–	–	–	(27)	(21)	(50)/66
CP	MSS	(46)/68	37/55	–	(49)/24	(43)/53	(46)/53	(18)	–	(18)	(43)/63
	IS	(46)	(34)	(34)	(49)/–	–	–	(18)	–	(18)	(43)
	LSS	(46)	(34)	(34)	(49)/–	–	–	(18)	–	(18)	(43)
Z	MSS	–	–	–	–	–	–	–	–	–	–
	IS	–/44	–/31	–/33	–	–	–	–	–	–	–/43
	LSS	–/44	–/31	–/33	–	–	–	–	–	–	–/43
SIO_0, SIO_3	Any	(18)	–	–	–	–	–	–	–	–	–

NOTES:

1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. A number is parentheses means the delay path is the same as specified in the Standard Functions and Increment by One or Two Instructions Table. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.
4. If two delays are given, the first is for 1st divide and normalization; the second is for two's complement divide and two's complement divide correction.
5. Double Length Normalize and First Divide Op
   SFA: $F = S + C_n$
   Y = Log. 2F
   Q = Log. 2Q
   $SIO_3 = F_3 \oplus R_3$ (MSS)
   $C_{n+4} = \overline{F}_3 \oplus \overline{F}_2$ (MSS)
   $OVR = \overline{F}_2 \oplus \overline{F}_1$ (MSS)
   $Z = \overline{Q}_0 \overline{Q}_1 \overline{Q}_2 \overline{Q}_3 \overline{F}_0 \overline{F}_1 \overline{F}_2 \overline{F}_3$

   Two's Complement Divide
   SFC: $F = R + S + C_n$ if $Z = 0$
   $F = S - R - 1 + C_n$ if $Z = 1$
   Y = Log. 2F
   Q = Log. 2Q
   $SIO_3 = \overline{F}_3 \oplus R_3$ (MSS)
   $Z = \overline{F}_3 \oplus R_3$ (MSS) from previous cycle

   Two's Complement Divide Correction and Remainder
   SFE: $F = R + S + C_n$ if $Z = 0$
   $F = S - R - 1 + C_n$ if $Z = 1$
   $Y = F$
   Q = Log. 2Q
   $Z = F_3 \oplus R_3$ (MSS) from previous cycle

IDT39C203A GUARANTEED COMMERCIAL RANGE PERFORMANCE BCD INSTRUCTIONS (SF1, SF7, SF9, SFB, SFD, SFF)

FROM	TO												
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DA, DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_0	SIO_3	SIO_0 PARITY
A, B Addr	MSS	58	48	–	(59)	54	54	(22)	–	–	44	(50)	(62)
	IS	58	48	44	(59)	–	–	(22)	–	–	44	(50)	(62)
	LSS	58	48	44	(59)	–	–	(22)	–	–	44	(50)	(62)
DA, DB	MSS	49	42	–	(52)	47	47	–	–	–	36	(47)	(52)
	IS	49	42	38	(52)	–	–	–	–	–	36	(47)	(52)
	LSS	49	42	38	(52)	–	–	–	–	–	36	(47)	(52)
C_n	MSS	29	18	–	30	26	26	–	–	–	24	29	35
	IS	29	18	–	30	–	–	–	–	–	24	29	35
	LSS	29	18	–	30	–	–	–	–	–	24	29	35
I_{8-0}	MSS	58	(51)	–	(58)/36	50	(50)	–	–	(21)	(40)	(50)	(59)
	IS	58	(51)	50	(58)/36	–	–	–	–	(21)	(40)	(50)	(59)
	LSS	58	(51)	50	(58)/36	–	–	–	(27)	(21)	(40)	(50)	(59)
CP	MSS	50	42	–	54/24	50	50	(18)	–	(18)	31	48	52
	IS	50	42	40	54/24	–	–	(18)	–	(18)	31	48	52
	LSS	50	42	40	54/24	–	–	(18)	–	(18)	31	48	52
SIO_{0-3}	Any	(18)	–	–	–	–	–	–	–	–	–	–	–

NOTES:

1. Binary-to-BCD and multiprecision Binary-to-BCD instructions only.
2. BCD-to-binary conversion (SF1), Binary-to-BCD conversion (SF9), BCD subtract (SFD, SFF), BCD divide by two (SF7), BCD add (SFB)
3. A "–" means the delay path does not exist.
4. A number in parentheses means the delay path is the same as specified in the Standard Functions and Increment by One or Two Instructions Table. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.
5. If two delays are given, the first is for 1st divide and normalization; the second is for two's complement divide and two's divide correction.

8

IDT39C203A GUARANTEED COMMERCIAL RANGE PERFORMANCE SIGN MAGNITUDE TO TWO'S COMPLEMENT CONVERSION (SF5)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DA, DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	78	67	–	36	71	71	(22)	–	–	84
	IS	(54)	(44)	(42)	–	–	–	(22)	–	–	(50)
	LSS	(54)	(44)	(42)	–	–	–	(22)	–	–	(50)
DA, DB	MSS	75	63	–	32	67	67	–	–	–	80
	IS	(46)	(40)	(32)	–	–	–	–	–	–	(47)
	LSS	(46)	(40)	(32)	–	–	–	–	–	–	(47)
C_n	MSS	(26)	(14)	–	–	26	(21)	–	–	–	(24)
	IS	(26)	(14)	–	–	–	–	–	–	–	(24)
	LSS	(26)	(14)	–	–	–	–	–	–	–	(24)
I_{8-0}	MSS	68	54	–	22	66	58	–	–	(21)	70*
	IS	68	54	50	–	–	–	–	–	(21)	70*
	LSS	68	54	50	–	–	–	–	(27)	(21)	70*
CP	MSS	75	63	–	32	67	67	(18)	–	(18)	80
	IS	(46)	(34)	(34)	–	–	–	(18)	–	(18)	(43)
	LSS	(46)	(34)	(34)	–	–	–	(18)	–	(18)	(43)
Z	MSS	–	–	–	–	–	–	–	–	–	–
	IS	46	31	28	–	–	–	–	–	–	48
	LSS	46	31	28	–	–	–	–	–	–	48
SIO_0, SIO_3	Any	(18)	–	–	–	–	–	–	–	–	–

NOTES:

1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. A number is parentheses means the delay path is the same as specified in the Standard Functions and Increment by One or Two Instructions Table. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.
4. SF5: $F = S + C_n$ if $Z = 0$, $F = \overline{S} + C_n$ if $Z = 1$, $Y_3 = S_3 \oplus F_3$(MSS), $Z = S_3$(MSS), $Q = Q$, $N = F_3$ if $Z = 0$, $N = F_3 \oplus S_3$ if $Z = 1$

IDT39C203A GUARANTEED COMMERCIAL RANGE PERFORMANCE SINGLE LENGTH NORMALIZATION (SF8)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DA, DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	(54)	–	–	–	–	–	(22)	–	–	(50)
	IS	(54)	(44)	(42)	–	–	–	(22)	–	–	(50)
	LSS	(54)	(44)	(42)	–	–	–	(22)	–	–	(50)
DA, DB	MSS	(46)	–	–	–	–	–	–	–	–	(47)
	IS	(46)	(40)	(32)	–	–	–	–	–	–	(47)
	LSS	(46)	(40)	(32)	–	–	–	–	–	–	(47)
C_n	MSS	(26)	–	–	–	–	–	–	–	–	(24)
	IS	(26)	(14)	–	–	–	–	–	–	–	(24)
	LSS	(26)	(14)	–	–	–	–	–	–	–	(24)
I_{8-0}	MSS	(51)	30	–	23	19	19	–	–	(21)	(50)*
	IS	(51)	(51)	(40)	23	–	–	–	–	(21)	(50)*
	LSS	(51)	(51)	(40)	23	–	–	–	(27)	(21)	(50)*
CP	MSS	(46)	23	–	24	21	21	(18)	–	(18)	(43)
	IS	(46)	(34)	(34)	24	–	–	(18)	–	(18)	(43)
	LSS	(46)	(34)	(34)	24	–	–	(18)	–	(18)	(43)
SIO_0, SIO_3	Any	(18)	–	–	–	–	–	–	–	–	–

NOTES:

1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. A number is parentheses means the delay path is the same as specified in the Standard Functions and Increment by One or Two Instructions Table. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.
4. SF8: $F = S + C_n$ $C_{n+4} = Q_3 \oplus Q_2$ (MSS) $OVR = Q_2 \oplus Q_1$ (MSS)
   $N = Q_3$ (MSS) $Z = \overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$
   $Y = F$
   Q = Log. 2Q

8

IDT39C203A GUARANTEED MILITARY RANGE PERFORMANCE

The tables below specify the guaranteed performance of the IDT39C203A over the military operating range of -55 °C to +125°C with V_{CC} from 4.5 to 5.5V. All data are in nanoseconds, with inputs switching between 0 and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

Table 15. Clock and Write Pulse Characteristics All Functions

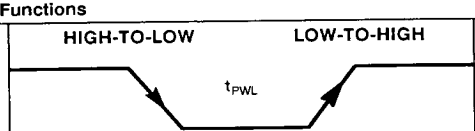
Minimum Clock Low Time	24ns
Minimum Clock High Time	24ns
Minimum Time CP and $\overline{WE}$ both Low to Write	24ns

Table 16. Enable/Disable Times All Functions (1)

FROM	TO	ENABLE	DISABLE
$\overline{OE}_Y$	Y	20	17
$\overline{OE}_B$	DB	20	17
$\overline{EA}$	DA	20	17
I_8	SIO	20	17
I_8	QIO	30	30
$I_{8,7,6,5}$	QIO	30	30
$I_{4,3,2,1,0}$	QIO	30	28
$\overline{LSS}$	$\overline{WRITE}$	24	20

NOTE:
1. C_L = 5.0pF for output disable tests. Measurement is made to a 0.5V change on the output.

Table 17. Set-up and Hold Times All Functions



FROM	WITH RESPECT TO	SET-UP	HOLD	SET-UP	HOLD	COMMENTS
Y	CP	Don't Care	Don't Care	11	3	Store Y in RAM/Q (1)
$\overline{WE}$ HIGH	CP	12	T_{PWL}		0	Prevent Writing
$\overline{WE}$ LOW	CP	Don't Care	Don't Care	12	0	Write into RAM
A, B Source	CP	16	3	Don't Care	Don't Care	Latch Data from RAM Out
B Destination	CP	5	T_{PWL}		3	Write Data into B Address
$QIO_{0,3}$	CP	Don't Care	Don't Care	14	3	Shift Q
$I_{8,7,6,5}$	CP	10	–	16	0	Write into Q(2)
$\overline{IEN}$ HIGH	CP	19	T_{PWL}		0	Prevent Writing into Q
$\overline{IEN}$ LOW	CP	Don't Care	Don't Care	17	0	Write into Q
$I_{4,3,2,1,0}$	CP	14	–	26	0	Write into Q(2)

NOTES:
1. The internal Y-bus to RAM set-up condition will be met 5ns after valid Y output ($\overline{OE}_Y$ = L)
2. The set-up time with respect to CP falling edge is to prevent writing. The set-up time with respect to CP rising edge is to enable writing.
3. For all other set-up conditions not specified in this table, the set-up time should be the delay to stable Y output plus the Y to RAM internal set-up time. Even if the RAM is not being loaded, this set-up condition ensures valid writing into the Q register and sign compare flip-flop.
4. $\overline{WE}$ controls writing into the RAM. IEN controls writing into Q and, indirectly, controls $\overline{WE}$ through the $\overline{WRITE}/\overline{MSS}$ output. To prevent writing, $\overline{IEN}$ and $\overline{WE}$ must go HIGH during the entire clock LOW time. They may go LOW after the clock has gone LOW to cause a write, provided the $\overline{WE}$ LOW and $\overline{IEN}$ LOW set-up times are met. Having gone LOW, they should not be returned HIGH until after the clock has gone HIGH.
5. A and B addresses must be set up prior to the clock HIGH-TO-LOW transition to latch data at the RAM output.
6. Writing occurs when CP and $\overline{WE}$ are both LOW. The B address should be stable during this entire period.
7. Because $I_{8,7,6,5}$ controls the writing or not writing of data into RAM and Q, they should be stable during the entire clock LOW time unless $\overline{IEN}$ is HIGH, which prevents writing.
8. The set-up time prior to the clock LOW-TO-HIGH transition occurs in parallel with the set-up time prior to the clock HIGH-TO-LOW transition and the clock LOW time. The actual set-up time requirement on $I_{4,3,2,1,0}$ relative to the clock LOW-TO-HIGH transition is the longer of (1) the set-up time prior to clock L ⟶ H and (2) the sum of the set-up time prior to clock H ⟶ L and the clock LOW time.

IDT39C203A GUARANTEED MILITARY RANGE PERFORMANCE
STANDARD FUNCTIONS AND INCREMENT/DECREMENT BY ONE OR TWO INSTRUCTIONS (SF3, SF4)

FROM	TO											
	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DA, DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_0	SIO_3	SIO_0 PARITY
A, B Addr	56	46	42	62	54	54	22	–	–	38	57	67
DA, DB	48	42	32	53	44	46	–	–	–	28	49	59
C_n	28	15	–	33	25	23	–	–	–	18	26	32
I_{8-0}	58	55	45	64	57	55	–	29	21	46	60	71
CP	48	34	34	54	44	46	18	–	18	33	49	53
SIO_0, SIO_3	21	–	–	23	–	–	–	–	–	–	23	15
$\overline{MSS}$	35	–	35	35	35	35	–	–	–	–	35	–
$\overline{EA}$	48	42	32	53	44	46	–	–	–	28	49	59

NOTES:
1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output..
3. Standard Functions: See Table 2, Increment SF4: $F = S + 1 + C_n$ and Decrement SF3: $F = S - 2 + C_n$

MULTIPLY INSTRUCTIONS (SF0, SF2, SF6)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DA, DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_0
A, B Addr	MSS	(56)	(46)	–	–	(54)	(54)	(22)	–	–	(38)
	IS	(56)	(46)	(42)	–	–	–	(22)	–	–	(38)
	LSS	(56)	(46)	(42)	–	–	–	(22)	–	–	(38)
DA, DB	MSS	(48)	(42)	–	–	(44)	(46)	–	–	–	(28)
	IS	(48)	(42)	(32)	–	–	–	–	–	–	(28)
	LSS	(48)	(42)	(32)	–	–	–	–	–	–	(28)
C_n	MSS	32	(15)	–	–	(25)	(23)	–	–	–	(18)
	IS	(28)	(15)	–	–	–	–	–	–	–	(18)
	LSS	(28)	(15)	–	–	–	–	–	–	–	(18)
I_{8-0}	MSS	86	67	–	–	78	78	–	–	(21)	65*
	IS	86	67	64	–	–	–	–	–	(21)	65*
	LSS	86	67	64	26	–	–	–	(29)	(21)	65*
CP	MSS	(48)	(34)	–	–	(44)	(46)	(18)	–	(18)	(33)
	IS	(48)	(34)	(34)	–	–	–	(18)	–	(18)	(33)
	LSS	87	68	63	27	–	–	(18)	–	(18)	66
Z	MSS	60	41	–	–	52	52	–	–	–	38
	IS	60	41	38	–	–	–	–	–	–	38
	LSS	–	–	–	–	–	–	–	–	–	–
SIO_0, SIO_3	Any	(21)	–	–	–	–	–	–	–	–	–

NOTES:
1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. A number in parenthesis means the delay path is the same as specified in the Standard Functions and Increment by One or Two Instructions Table. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Tests.
4. Unsigned Multiply
   SF0: $F = S + C_n$ if $Z = 0$
   $F = S + R + C_n$ if $Z = 1$
   $Y_3 = C_{n+4}$ (MSS)
   $Z = Q_0$ (LSS)
   Y = Log. F/2
   Q = Log. Q/2

   Two's Complement Multiply
   SF2: $F = S + C_n$ if $Z = 0$
   $F = R + S + C_n$ if $Z = 1$
   $Y_3 = F_3 \oplus$ OVR (MSS)
   $Z = Q_0$ (LSS)
   Y = Log. F/2
   Q = Log. Q/2

   Two's Complement Multiply Last Cycle
   SF6: $F = S + C_n$ if $Z = 0$
   $F = S - R - 1 + C_n$ if $Z = 1$
   $Y_3 =$ OVR $\oplus F_3$ (MSS)
   $Z = Q_0$ (LSS)
   Y = Log. F/2
   Q = Log. Q/2

IDT39C203A GUARANTEED MILITARY RANGE PERFORMANCE DIVIDE INSTRUCTIONS (SFA, SFC, SFE)

FROM		TO									
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DA, DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	(56)	58/(46)	–	(62)/–	(54)	(54)	(22)	–	–	(57)
	IS	(56)	(46)	(42)	(62)/–	–	–	(22)	–	–	(57)
	LSS	(56)	(46)	(42)	(62)/–	–	–	(22)	–	–	(57)
DA, DB	MSS	(48)	53/(42)	–	(53)/–	(44)	(46)	–	–	–	(49)
	IS	(48)	(42)	(32)	(53)/–	–	–	–	–	–	(49)
	LSS	(48)	(42)	(32)	(53)/–	–	–	–	–	–	(49)
C_n	MSS	(28)	30/(15)	–	(33)/–	(25)	(23)	–	–	–	29
	IS	(28)	(15)	–	(33)/–	–	–	–	–	–	(26)
	LSS	(28)	(15)	–	(33)/–	–	–	–	–	–	(26)
I_{8-0}	MSS	(58)/77	71/63	–	(64)/26	(57)/73	(55)/73	–	–	(21)	61/78*
	IS	(58)/77	(55)/63	(45)/63	(64)	–	–	–	–	(21)	(60)/78*
	LSS	(58)/77	(55)/63	(45)/63	(64)	–	–	–	(29)	(21)	(60)/78*
CP	MSS	(48)/78	41/64	–	(54)/27	(44)/59	(46)/59	(18)	–	(18)	(49)/74
	IS	(48)	(34)	(34)	(54)	–	–	(18)	–	(18)	(49)
	LSS	(48)	(34)	(34)	(54)	–	–	(18)	–	(18)	(49)
Z	MSS	–	–	–	–	–	–	–	–	–	–
	IS	–/50	–/37	–/37	–	–	–	–	–	–	–/52
	LSS	–/50	–/37	–/37	–	–	–	–	–	–	–/52
SIO_0, SIO_3	Any	(21)	–	–	–	–	–	–	–	–	–

NOTES:

1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. A number is parentheses means the delay path is the same as specified in the Standard Functions and Increment by One or Two Instructions Table. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.
4. If two delays are given, the first is for 1st divide and normalization; the second is for two's complement divide and two's complement divide correction.
5. Double Length Normalize and First Divide Op
   SFA: $F = S + C_n$
   $SIO_3 = F_3 \oplus R_3$ (MSS)
   $C_{n+4} = F_3 \oplus F_2$ (MSS)
   $OVR = F_2 \oplus F_1$ (MSS)
   $Z = \overline{Q}_0 \overline{Q}_1 \overline{Q}_2 \overline{Q}_3 \overline{F}_0 \overline{F}_1 \overline{F}_2 \overline{F}_3$
   Y = Log. 2F
   Q = Log. 2Q

   Two's Complement Divide
   SFC: $F = R + S + C_n$ if $Z = 0$
   $F = S - R - 1 + C_n$ if $Z = 1$
   Y = Log. 2F
   Q = Log. 2Q
   $SIO_3 = \overline{F_3 \oplus R_3}$ (MSS)
   $Z = \overline{F_3 \oplus R_3}$ (MSS) from previous cycle

   Two's Complement Divide Correction and Remainder
   SFE: $F = R + S + C_n$ if $Z = 0$
   $F = S - R - 1 + C_n$ if $Z = 1$
   $Y = F$
   Q = Log. 2Q
   $Z = F_3 \oplus R_3$ (MSS) from previous cycle

IDT39C203A GUARANTEED MILITARY RANGE PERFORMANCE BCD INSTRUCTIONS (SF1, SF7, SF9, SFB, SFD, SFF)

FROM	TO												
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DA, DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_0	SIO_3	SIO_0 PARITY
A, B Addr	MSS	60	52	–	(62)	56	56	(22)	–	–	48	(57)	(67)
	IS	60	52	46	(62)	–	–	(22)	–	–	48	(57)	(67)
	LSS	60	52	46	(62)	–	–	(22)	–	–	48	(57)	(67)
DA, DB	MSS	50	43	–	(53)	51	51	–	–	–	40	(49)	(59)
	IS	50	43	40	(53)	–	–	–	–	–	40	(49)	(59)
	LSS	50	43	40	(53)	–	–	–	–	–	40	(49)	(59)
C_n	MSS	31	21	–	35	30	30	–	–	–	27	31	38
	IS	31	21	–	35	–	–	–	–	–	27	31	38
	LSS	31	21	–	35	–	–	–	–	–	27	31	38
I_{8-0}	MSS	61	(55)	–	(64)/40[1]	58	58	–	–	(21)	(46)	(60)	(71)
	IS	61	(55)	56	(64)/40[1]	–	–	–	–	(21)	(46)	(60)	(71)
	LSS	61	(55)	56	(64)/40[1]	–	–	–	(29)	(21)	(46)	(60)	(71)
CP	MSS	54	43	–	56/27[1]	53	53	(18)	–	(18)	34	50	59
	IS	54	43	42	56/27[1]	–	–	(18)	–	(18)	34	50	59
	LSS	54	43	42	56/27[1]	–	–	(18)	–	(18)	34	50	59
SIO_{0-3}	Any	(21)	–	–	–	–	–	–	–	–	–	–	–

NOTES:

1. Binary-to-BCD and multiprecision Binary-to-BCD instructions only.
2. BCD-to-binary conversion (SF1), Binary-to-BCD conversion (SF9), BCD subtract (SFD, SFF), BCD divide by two (SF7), BCD add (SFB)
3. A "–" means the delay path does not exist.
4. A number in parentheses means the delay path is the same as specified in the Standard Functions and Increment by One or Two Instructions Table. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.
5. If two delays are given, the first is for 1st divide and normalization; the second is for two's complement divide and two's complement divide cor rection.

8

IDT39C203A GUARANTEED MILITARY RANGE PERFORMANCE
SIGN MAGNITUDE TO TWO'S COMPLEMENT CONVERSION (SF5)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DA, DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	91	78	–	42	85	85	(22)	–	–	102
	IS	(56)	(46)	(42)	–	–	–	(22)	–	–	(57)
	LSS	(56)	(46)	(42)	–	–	–	(22)	–	–	(57)
DA, DB	MSS	86	74	–	37	81	81	–	–	–	90
	IS	(48)	(42)	(32)	–	–	–	–	–	–	(49)
	LSS	(48)	(42)	(32)	–	–	–	–	–	–	(49)
C_n	MSS	29	(15)	–	–	28	(23)	–	–	–	(26)
	IS	(28)	(15)	–	–	–	–	–	–	–	(26)
	LSS	(28)	(15)	–	–	–	–	–	–	–	(26)
I_{8-0}	MSS	78	63	–	26	78	70	–	–	(21)	87*
	IS	78	63	58	–	–	–	–	–	(21)	87*
	LSS	78	63	58	–	–	–	–	(29)	(21)	87*
CP	MSS	85	74	–	37	81	81	(18)	–	(18)	98
	IS	(48)	(34)	(34)	–	–	–	(18)	–	(18)	(49)
	LSS	(48)	(34)	(34)	–	–	–	(18)	–	(18)	(49)
Z	MSS	–	–	–	–	–	–	–	–	–	–
	IS	52	37	32	–	–	–	–	–	–	61
	LSS	52	37	32	–	–	–	–	–	–	61
SIO_0, SIO_3	Any	(21)	–	–	–	–	–	–	–	–	–

NOTES:

1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. A number is parentheses means the delay path is the same as specified in the Standard Functions and Increment by One or Two Instructions Table. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.
4. SF5: $F = S + C_n$ if $Z = 0$, $F = \overline{S} + C_n$ if $Z = 1$, $Y_3 = S_3 \oplus F_3$ (MSS), $Z = S_3$ (MSS), $Y = F$, $Q = Q$, $N = F_3$ if $Z = 0$, $N = F_3 \oplus S_3$ if $Z = 1$

IDT39C203A GUARANTEED MILITARY RANGE PERFORMANCE SINGLE LENGTH NORMALIZATION (SF8)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DA, DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	(56)	–	–	–	–	–	(22)	–	–	(57)
	IS	(56)	(46)	(42)	–	–	–	(22)	–	–	(57)
	LSS	(56)	(46)	(42)	–	–	–	(22)	–	–	(57)
DA, DB	MSS	(48)	–	–	–	–	–	–	–	–	(49)
	IS	(48)	(42)	(32)	–	–	–	–	–	–	(49)
	LSS	(48)	(42)	(32)	–	–	–	–	–	–	(49)
C_n	MSS	(28)	–	–	–	–	–	–	–	–	(26)
	IS	(28)	(15)	–	–	–	–	–	–	–	(26)
	LSS	(28)	(15)	–	–	–	–	–	–	–	(26)
I_{8-0}	MSS	(58)	38	–	26	22	22	–	–	(21)	60*
	IS	(58)	(55)	(45)	26	–	–	–	–	(21)	60*
	LSS	(58)	(55)	(45)	26	–	–	–	(29)	(21)	60*
CP	MSS	(48)	25	–	27	21	25	(18)	–	(18)	(49)
	IS	(48)	(34)	(34)	27	–	–	(18)	–	(18)	(49)
	LSS	(48)	(34)	(34)	27	–	–	(18)	–	(18)	(49)
SIO_0, SIO_3	Any	(21)	–	–	–	–	–	–	–	–	–

NOTES:

1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. A number is parentheses means the delay path is the same as specified in the Standard Functions and Increment by One or Two Instructions Table. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.
4. SF8: $F = S + C_n$ $C_{n+4} = Q_3 \oplus Q_2$ (MSS) $OVR = Q_2 \oplus Q_1$ (MSS)
   $N = Q_3$ (MSS) $Z = \overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$
   $Y = F$
   Q = Log. 2Q

8

IDT39C203 GUARANTEED COMMERCIAL RANGE PERFORMANCE

The tables below specify the guaranteed performance of the IDT39C203 over the commercial operating range of 0 to 70°C with V_{CC} from 4.75 to 5.25V. All data are in nanoseconds, with inputs switching between 0 and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

Table 6. Clock and Write Pulse Characteristics All Functions

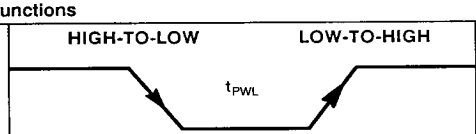
Minimum Clock Low Time	30ns
Minimum Clock High Time	30ns
Minimum Time CP and $\overline{WE}$ both Low to Write	15ns

Table 7. Enable/Disable Times All Functions (1)

FROM	TO	ENABLE	DISABLE
$\overline{OE}_Y$	Y	25	21
$\overline{OE}_B$	DB	25	21
$\overline{EA}$	DA	25	21
I_8	SIO	25	21
I_8	QIO	38	38
$I_{8,7,6,5}$	QIO	38	38
$I_{4,3,2,1,0}$	QIO	38	35
$\overline{LSS}$	$\overline{WRITE}$	25	21

NOTE:
1. C_L = 5pF for output disable tests. Measurement is made to a 0.5V change on the output.

Table 8. Set-up and Hold Times All Functions



FROM	WITH RESPECT TO	SET-UP	HOLD	SET-UP	HOLD	COMMENTS
Y	CP	Don't Care	Don't Care	14	3	Store Y in RAM/Q (1)
$\overline{WE}$ HIGH	CP	15	T_{PWL}		0	Prevent Writing
$\overline{WE}$ LOW	CP	Don't Care	Don't Care	15	0	Write into RAM
A, B Source	CP	20	3	Don't Care	Don't Care	Latch Data from RAM Out
B Destination	CP	6	T_{PWL}		3	Write Data into B Address
$QIO_{0,3}$	CP	Don't Care	Don't Care	17	3	Shift Q
$I_{8,7,6,5}$	CP	12	–	20	0	Write into Q(2)
$\overline{IEN}$ HIGH	CP	24	T_{PWL}		0	Prevent Writing into Q
$\overline{IEN}$ LOW	CP	Don't Care	Don't Care	21	0	Write into Q
$I_{4,3,2,1,0}$	CP	18	–	32	0	Write into Q(2)

NOTES:
1. The internal Y-bus to RAM set-up condition will be met 5ns after valid Y output ($\overline{OE}_Y$ = L)
2. The set-up time with respect to CP falling edge is to prevent writing. The set-up time with respect to CP rising edge is to enable writing.
3. For all other set-up conditions not specified in this table, the set-up time should be the delay to stable Y output plus the Y to RAM internal set-up time. Even if the RAM is not being loaded, this set-up condition ensures valid writing into the Q register and sign compare flip-flop.
4. $\overline{WE}$ controls writing into the RAM. IEN controls writing into Q and, indirectly, controls $\overline{WE}$ through the $\overline{WRITE}/\overline{MSS}$ output. To prevent writing, $\overline{IEN}$ and $\overline{WE}$ must go HIGH during the entire clock LOW time. They may go LOW after the clock has gone LOW to cause a write, provided the $\overline{WE}$ LOW and $\overline{IEN}$ LOW set-up times are met. Having gone LOW, they should not be returned HIGH until after the clock has gone HIGH.
5. A and B addresses must be set up prior to the clock HIGH-TO-LOW transition to latch data at the RAM output.
6. Writing occurs when CP and $\overline{WE}$ are both LOW. The B address should be stable during this entire period.
7. Because $I_{8,7,6,5}$ controls the writing or not writing of data into RAM and Q, they should be stable during the entire clock LOW time unless $\overline{IEN}$ is HIGH, which prevents writing.
8. The set-up time prior to the clock LOW-TO-HIGH transition occurs in parallel with the set-up time prior to the clock HIGH-TO-LOW transition and the clock LOW time. The actual set-up time requirement on $I_{4,3,2,1,0}$ relative to the clock LOW-TO-HIGH transition is the longer of (1) the set-up time prior to clock L → H and (2) the sum of the set-up time prior to clock H → L and the clock LOW time.

IDT39C203 GUARANTEED COMMERCIAL RANGE PERFORMANCE
STANDARD FUNCTIONS AND INCREMENT/DECREMENT BY ONE OR TWO INSTRUCTIONS (SF3, SF4)

FROM	TO											
	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DA, DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_0	SIO_3	SIO_0 PARITY
A, B Addr	67	55	52	74	61	67	28	–	–	41	62	78
DA, DB	58	50	40	65	54	58	–	–	–	35	59	65
C_n	33	18	–	35	28	27	–	–	–	23	30	38
I_{8-0}	64	64	50	72	61	62	–	34	26*	50*	62*	74*
CP	58	42	43	61	54	58	22	–	22	37	54	60
SIO_0, SIO_3	23	–	–	29	–	–	–	–	–	–	29	19
$\overline{MSS}$	44	–	44	44	44	44	–	–	–	–	44	–
$\overline{EA}$	58	50	40	65	54	58	–	–	–	35	59	65

NOTES:
1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. Standard Functions: See Table 2, Increment SF4: $F = S + 1 + C_n$ and Decrement SF3: $F = S - 2 + C_n$

MULTIPLY INSTRUCTIONS (SF0, SF2, SF6)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DA, DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_0
A, B Addr	MSS	(67)	(55)	–	–	(61)	(67)	(28)	–	–	(41)
	IS	(67)	(55)	(52)	–	–	–	(28)	–	–	(41)
	LSS	(67)	(55)	(52)	–	–	–	(28)	–	–	(41)
DA, DB	MSS	(58)	(50)	–	–	(54)	(58)	–	–	–	(35)
	IS	(58)	(50)	(40)	–	–	–	–	–	–	(35)
	LSS	(58)	(50)	(40)	–	–	–	–	–	–	(35)
C_n	MSS	35	(18)	–	–	(28)	(27)	–	–	–	(23)
	IS	(33)	(18)	–	–	–	–	–	–	–	(23)
	LSS	(33)	(18)	–	–	–	–	–	–	–	(23)
I_{8-0}	MSS	94	75	–	–	88	88	–	–	(26)*	73*
	IS	94	75	71	–	–	–	–	–	(26)*	73*
	LSS	94	75	71	30	–	–	–	(34)	(26)*	73*
CP	MSS	(58)	(42)	–	–	(54)	(58)	(22)	–	(22)	(37)
	IS	(58)	(42)	(43)	–	–	–	(22)	–	(22)	(37)
	LSS	94	75	71	30	–	–	(22)	–	(22)	73
Z	MSS	64	45	–	–	58	58	–	–	–	43
	IS	64	45	41	–	–	–	–	–	–	43
	LSS	–	–	–	–	–	–	–	–	–	–
SIO_0, SIO_3	Any	(23)	–	–	–	–	–	–	–	–	–

NOTES:
1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output. An "*" shown without a number means the output is disabled by the input or it is enabled but the delay to correct data is determined by something else.
3. A number in parentheses means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instructions Test.
4. Unsigned Multiply
   SF0: $F = S + C_n$ if $Z = 0$
   $F = S + R + C_n$ if $Z = 1$
   Y = Log. F/2
   Q = Log. Q/2
   $Y_3 = C_{n+4}$ (MSS)
   $Z = Q_0$ (LSS)

   Two's Complement Multiply
   SF2: $F = S + C_n$ if $Z = 0$
   $F = R + S + C_n$ if $Z = 1$
   Y = Log. F/2
   Q = Log. Q/2
   $Y_3 = F_3 \oplus$ OVR (MSS)
   $Z = Q_0$ (LSS)

   Two's Complement Multiply Last Cycle
   SF6: $F = S + C_n$ if $Z = 0$
   $F = S - R - 1 + C_n$ if $Z = 1$
   Y = Log. F/2
   Q = Log. Q/2
   $Y_3 =$ OVR $\oplus$ (MSS)
   $Z = Q_0$ (LSS)

8

IDT39C203 GUARANTEED COMMERCIAL RANGE PERFORMANCE DIVIDE INSTRUCTIONS (SFA, SFC, SFE)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DA, DB	$\overline{WRITE}/\overline{MSS}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	(67)	61/(55)	–	(74)/–	(61)	(67)	(28)	–	–	62
	IS	(67)	(55)	(52)	(74)/–	–	–	(28)	–	–	62
	LSS	(67)	(55)	(52)	(74)/–	–	–	(28)	–	–	62
DA, DB	MSS	(58)	55/(50)	–	(65)/–	(54)	(58)	–	–	–	59
	IS	(58)	(50)	(40)	(65)/–	–	–	–	–	–	59
	LSS	(58)	(50)	(40)	(65)/–	–	–	–	–	–	59
C_n	MSS	(33)	33/(18)	–	(35)/–	(28)	(27)	–	–	–	32
	IS	(33)	(18)	–	(35)/–	–	–	–	–	–	30
	LSS	(33)	(18)	–	(35)/–	–	–	–	–	–	30
I_{8-0}	MSS	(64)/84	75/68	–	(72)/29	(61)/77	(62)/77	–	–	(26)*	63/83*
	IS	(64)/84	(64)/68	(50)/70	(72)/–	–	–	–	–	(26)*	(62)/83*
	LSS	(64)/84	(64)/68	(50)70	(72)/–	–	–	–	(34)	(26)*	(62)/83*
CP	MSS	(58)/85	46/69	–	(61)/30	(54)/66	(58)/66	(22)	–	(22)	(54)/79*
	IS	(58)	(42)	(43)	(61)/–	–	–	(22)	–	(22)	(54)
	LSS	(58)	(42)	(43)	(61)/–	–	–	(22)	–	(22)	(54)
Z	MSS	–	–	–	–	–	–	–	–	–	–
	IS	–/55	–/39	–/41	–	–	–	–	–	–	–/54
	LSS	–/55	–/39	–/41	–	–	–	–	–	–	–/54
SIO_0, SIO_3	Any	(23)	–	–	–	–	–	–	–	–	–

NOTES:

1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.
3. A number is parentheses means the delay path is the same as specified in the Standard Functions and Increment by One or Two Instructions Table. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.
4. If two delays are given, the first is for 1st divide and normalization; the second is for two's complement divide and two's complement divide correction.
5. Double Length Normalize and First Divide Op
   SFA: $F = S + C_n$
   Y = Log. 2F
   Q = Log. 2Q
   $SIO_3 = F_3 \oplus R$ (MSS)
   $C_{n+4} = F_3 \oplus F_2$ (MSS)
   $OVR = F_2 \oplus F_1$ (MSS)
   $Z = \overline{Q}_0 \overline{Q}_1 \overline{Q}_2 \overline{Q}_3 \overline{F}_0 \overline{F}_1 \overline{F}_2 \overline{F}_3$

   Two's Complement Divide
   SFC: $F = R + S + C_n$ if $Z = 0$
   $F = S - R - 1 + C_n$ if $Z = 1$
   Y = Log. 2F
   Q = Log. 2Q
   $SIO_3 = F_3 \oplus \overline{R}_3$(MSS)
   $Z = \overline{F_3 \oplus R_3}$ (MSS) from previous cycle

   Two's Complement Divide Correction and Remainder
   SFE: $F = R + S + C_n$ if $Z = 0$
   $F = S - R - 1 + C_n$ if $Z = 1$
   $Y = F$
   Q = Log. 2Q
   $Z = F_3 \oplus R_3$(MSS) from previous cycle

IDT39C203 GUARANTEED COMMERCIAL RANGE PERFORMANCE BCD INSTRUCTIONS (SF1, SF7, SF9, SFB, SFD, SFF)

FROM	TO												
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DA, DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_0	SIO_3	SIO_0 PARITY
A, B Addr	MSS	72	60	–	(74)	68	68	(28)	–	–	55	(62)	(78)
	IS	72	60	55	(74)	–	–	(28)	–	–	55	(62)	(78)
	LSS	72	60	55	(74)	–	–	(28)	–	–	55	(62)	(78)
DA, DB	MSS	61	52	–	(65)	59	59	–	–	–	45	(59)	(65)
	IS	61	52	48	(65)	–	–	–	–	–	45	(59)	(65)
	LSS	61	52	48	(65)	–	–	–	–	–	45	(59)	(65)
C_n	MSS	36	23	–	37	33	33	–	–	–	30	36	44
	IS	36	23	–	37	–	–	–	–	–	30	36	44
	LSS	36	23	–	37	–	–	–	–	–	30	36	44
I_{8-0}	MSS	72	(64)	–	(72)/45[1]	62	(62)	–	–	(26)	(50)	(62)	(74)
	IS	72	(64)	63	(72)/45[1]	–	–	–	–	(26)	(50)	(62)	(74)
	LSS	72	(64)	63	(72)/45[1]	–	–	–	(34)	(26)	(50)	(62)	(74)
CP	MSS	62	53	–	68/30[1]	62	62	(22)	–	(22)	39	60	65
	IS	62	53	50	68/30[1]	–	–	(22)	–	(22)	39	60	65
	LSS	62	53	50	68/30[1]	–	–	(22)	–	(22)	39	60	65
SIO_{0-3}	Any	(23)	–	–	–	–	–	–	–	–	–	–	–

NOTES:

1. Binary-to-BCD and multiprecision Binary-to-BCD instructions only.
2. BCD-to-binary conversion (SF1), Binary-to-BCD conversion (SF9), BCD subtract (SFD, SFF), BCD divide by two (SF7), BCD add (SFB)
3. A number in parentheses means the delay path is the same as specified in the Standard Functions and Increment by One or Two Instructions Table. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.

8

IDT39C203 GUARANTEED COMMERCIAL RANGE PERFORMANCE
SIGN MAGNITUDE TO TWO'S COMPLEMENT CONVERSION (SF5)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DA, DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	97	84	–	45	89	89	(28)	–	–	105
	IS	(67)	(55)	(52)	–	–	–	(28)	–		(62)
	LSS	(67)	(55)	(52)	–	–	–	(28)	–		(62)
DA, DB	MSS	94	79	–	40	84	84	–	–		100
	IS	(58)	(50)	(40)	–	–	–	–	–		(59)
	LSS	(58)	(50)	(40)	–	–	–	–	–		(59)
C_n	MSS	(33)	(18)	–	–	32	(27)	–	–		(30)
	IS	(33)	(18)	–	–	–	–	–	–		(30)
	LSS	(33)	(18)	–	–	–	–	–	–		(30)
I_{8-0}	MSS	85	67	–	28	82	73	–	–	(26)	88*
	IS	85	67	63	–	–	–	–	–	(26)	88*
	LSS	85	67	63	–	–	–	–	(34)	(26)	88*
CP	MSS	94	79	–	40	84	84	(22)	–	(22)	100
	IS	(58)	(42)	(43)	–	–	–	(22)	–	(22)	(54)
	LSS	(58)	(42)	(43)	–	–	–	(22)	–	(22)	(54)
Z	MSS	–	–	–	–	–	–	–	–	–	–
	IS	57	39	35	–	–	–	–	–	–	60
	LSS	57	39	35	–	–	–	–	–	–	60
SIO_0, SIO_3	Any	(23)	–	–	–	–	–	–	–	–	–

NOTES:

1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.
3. A number in parentheses means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.
4. SF5: $F = S + C_n$ if $Z = 0$, $Y_3 = S_3 \oplus F_3$(MSS), $Q = Q$
   $F = \overline{S} + C_n$ if $Z = 1$, $Z = S_3$(MSS), $N = F_3$ if $Z = 0$
   $N = F_3 \oplus S_3$ if $Z = 1$

IDT39C203 COMMERCIAL RANGE PERFORMANCE SINGLE LENGTH NORMALIZATION (SF8)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DA, DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	(67)	–	–	–	–	–	(28)	–	–	(62)
	IS	(67)	(55)	(52)	–	–	–	(28)	–	–	(62)
	LSS	(67)	(55)	(52)	–	–	–	(28)	–	–	(62)
DA, DB	MSS	(58)	–	–	–	–	–	–	–	–	(59)
	IS	(58)	(50)	(40)	–	–	–	–	–	–	(59)
	LSS	(58)	(50)	(40)	–	–	–	–	–	–	(59)
C_n	MSS	(33)	–	–	–	–	–	–	–	–	(30)
	IS	(33)	(18)	–	–	–	–	–	–	–	(30)
	LSS	(33)	(18)	–	–	–	–	–	–	–	(30)
I_{8-0}	MSS	(64)	37	–	29	24	24	–	–	(26)	(62)*
	IS	(64)	(64)	(50)	29	–	–	–	–	(26)	(62)*
	LSS	(64)	(64)	(50)	29	–	–	–	(34)	(26)	(62)*
CP	MSS	(58)	29	–	30	26	29	(22)	–	(22)	(54)
	IS	(58)	(42)	(43)	30	–	–	(22)	–	(22)	(54)
	LSS	(58)	(42)	(43)	30	–	–	(22)	–	(22)	(54)
SIO_0, SIO_3	Any	(23)	–	–	–	–	–	–	–	–	–

NOTES:

1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.
3. A number is parantheses means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.
4. SF8: $F = S + C_n$ $C_{n+4} = Q_3 \oplus Q_2$ (MSS) $OVR = Q_2 \oplus Q_1$ (MSS)
   $N = Q_3$ (MSS) $Z = \overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$
   $Y = F$
   $Q = LOG\ 2Q$

8

IDT39C203 GUARANTEED MILITARY RANGE PERFORMANCE

The tables below specify the guaranteed performance of the IDT39C203 over the military operating range of -55°C to + 125°C with V_{CC} from 4.5 to 5.5V. All data are in nanoseconds, with inputs switching between 0 and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

Table 9. Clock and Write Pulse Characteristics All Functions

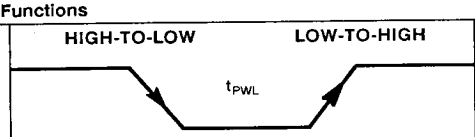
Minimum Clock Low Time	30ns
Minimum Clock High Time	30ns
Minimum Time CP and $\overline{WE}$ both Low to Write	30ns

Table 10. Enable/Disable Times All Functions[1]

FROM	TO	ENABLE	DISABLE
$\overline{OE}_Y$	Y	25	21
$\overline{OE}_B$	DB	25	21
$\overline{EA}$	DA	25	21
I_8	SIO	25	21
I_8	QIO	38	38
$I_{8,7,6,5}$	QIO	38	38
$I_{4,3,2,1,0}$	QIO	38	35
$\overline{LSS}$	$\overline{WRITE}$	30	25

NOTE:
1. C_L = 5.0pF for output disable tests. Measurement is made to a 0.5V change on the output.

Table 11. Set-up and Hold Times All Functions



FROM	WITH RESPECT TO	SET-UP	HOLD	SET-UP	HOLD	COMMENTS
Y	CP	Don't Care	Don't Care	14	3	Store Y in RAM/Q[1]
$\overline{WE}$ HIGH	CP	15	T_{PWL}		0	Prevent Writing
$\overline{WE}$ LOW	CP	Don't Care	Don't Care	15	0	Write into RAM
A, B Source	CP	20	3	Don't Care	Don't Care	Latch Data from RAM Out
B Destination	CP	6	T_{PWL}		3	Write Data into B Address
$QIO_{0,3}$	CP	Don't Care	Don't Care	17	3	Shift Q
$I_{8,7,6,5}$	CP	12	–	20	0	Write into Q[2]
$\overline{IEN}$ HIGH	CP	24	T_{PWL}		0	Prevent Writing into Q
$\overline{IEN}$ LOW	CP	Don't Care	Don't Care	21	0	Write into Q
$I_{4,3,2,1,0}$	CP	18	–	32	0	Write into Q[2]

NOTES:
1. The internal Y-bus to RAM set-up condition will be met 5ns after valid Y output ($\overline{OE}_Y$= L)
2. The set-up time with respect to CP falling edge is to prevent writing. The set-up time with respect to CP rising edge is to enable writing.
3. For all other set-up conditions not specified in this table, the set-up time should be the delay to stable Y output plus the Y to RAM internal set-up time. Even if the RAM is not being loaded, this set-up condition ensures valid writing into the Q register and sign compare flip-flop.
4. $\overline{WE}$ controls writing into the RAM. IEN controls writing into Q and, indirectly, controls $\overline{WE}$ through the $\overline{WRITE}/\overline{MSS}$ output. To prevent writing, $\overline{IEN}$ and $\overline{WE}$ must go HIGH during the entire clock LOW time. They may go LOW after the clock has gone LOW to cause a write, provided the $\overline{WE}$ LOW and $\overline{IEN}$ LOW set-up times are met. Having gone LOW, they should not be returned HIGH until after the clock has gone HIGH.
5. A and B addresses must be set up prior to the clock HIGH-TO-LOW transition to latch data at the RAM output.
6. Writing occurs when CP and $\overline{WE}$ are both LOW. The B address should be stable during this entire period.
7. Because $I_{8,7,6,5}$ controls the writing or not writing of data into RAM and Q, they should be stable during the entire clock LOW time unless $\overline{IEN}$ is HIGH, which prevents writing.
8. The set-up time prior to the clock LOW-TO-HIGH transition occurs in parallel with the set-up time prior to the clock HIGH-TO-LOW transition and the clock LOW time. The actual set-up time requirement on $I_{4,3,2,1,0}$ relative to the clock LOW-TO-HIGH transition is the longer of (1) the set-up time prior to clock L → H and (2) the sum of the set-up time prior to clock H → L and the clock LOW time.

IDT39C203 GUARANTEED MILITARY RANGE PERFORMANCE
STANDARD FUNCTIONS AND INCREMENT/DECREMENT BY ONE OR TWO INSTRUCTIONS (SF3, SF4)

FROM	TO											
	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DA, DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_0	SIO_3	SIO_0 PARITY
A, B Addr	70	58	52	78	68	67	28	–	–	47	71	84
DA, DB	60	52	40	66	55	58	–	–	–	35	61	74
C_n	35	19	–	41	31	29	–	–	–	23	33	40
I_{8-0}	72	69	56	80	71	69	–	36	26*	58*	75*	89*
CP	60	42	43	67	55	58	22	–	22	41	61	66
SIO_0, SIO_3	26	–	–	29	–	–	–	–	–	–	29	19
$\overline{MSS}$	44	–	44	44	44	44	–	–	–	–	44	–
$\overline{EA}$	60	52	40	66	55	58	–	–	–	35	61	74

NOTES:
1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output.
3. Standard Functions: See Table 2, Increment SF4: $F = S + 1 + C_n$ and Decrement SF3: $F = S - 2 + C_n$

MULTIPLY INSTRUCTIONS (SF0, SF2, SF6)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DA, DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_0
A, B Addr	MSS	(70)	(58)	–	–	(68)	(67)	(28)	–	–	(47)
	IS	(70)	(58)	(52)	–	–	–	(28)	–	–	(47)
	LSS	(70)	(58)	(52)	–	–	–	(28)	–	–	(47)
DA, DB	MSS	(60)	(52)	–	–	(55)	(58)	–	–	–	(35)
	IS	(60)	(52)	(40)	–	–	–	–	–	–	(35)
	LSS	(60)	(52)	(40)	–	–	–	–	–	–	(35)
C_n	MSS	40	(19)	–	–	(31)	(29)	–	–	–	(23)
	IS	(35)	(19)	–	–	–	–	–	–	–	(23)
	LSS	(35)	(19)	–	–	–	–	–	–	–	(23)
I_{8-0}	MSS	108	84	–	–	98	98	–	–	(26)	81*
	IS	108	84	80	–	–	–	–	–	(26)	81*
	LSS	108	84	80	33	–	–	–	(36)	(26)	81*
CP	MSS	62	(42)	–	–	(55)	(58)	(22)	–	(22)	(41)
	IS	(60)	(42)	(43)	–	–	–	(22)	–	(22)	(41)
	LSS	109	85	79	34	–	–	(22)	–	(22)	82
Z	MSS	75	51	–	–	65	65	–	–	–	48
	IS	75	51	47	–	–	–	–	–	–	48
	LSS	–	–	–	–	–	–	–	–	–	–
SIO_0, SIO_3	Any	(26)	–	–	–	–	–	–	–	–	–

NOTES:
1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.
3. A number in parentheses means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.
4. Unsigned Multiply
   SF0: $F = S + C_n$ if $Z = 0$
   $F = S + R + C_n$ if $Z = 1$
   Y = Log. F/2
   Q = Log. Q/2
   $Y_3 = C_{n+4}$ (MSS)
   $Z = Q_0$ (LSS)

   Two's Complement Multiply
   SF2: $F = S + C_n$ if $Z = 0$
   $F = R + S + C_n$ if $Z = 1$
   Y = Log. F/2
   Q = Log. Q/2
   $Y_3 = F_3 \oplus$ OVR (MSS)
   $Z = Q_0$ (LSS)

   Two's Complement Multiply Last Cycle
   SF6: $F = S + C_n$ if $Z = 0$
   $F = S - R - 1 + C_n$ if $Z = 1$
   Y = Log. F/2
   Q = Log. Q/2
   $Y_3 =$ OVR $\oplus$ F_3(MSS)
   $Z = Q_0$ (LSS)

8

IDT39C203 GUARANTEED MILITARY RANGE PERFORMANCE DIVIDE INSTRUCTIONS (SFA, SFC, SFE)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DA, DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	(70)	72/(58)	–	(78)/–	(68)	(67)	(28)	–	–	(71)
	IS	(70)	(58)	(52)	(78)/–	–	–	(28)	–	–	(71)
	LSS	(70)	(58)	(52)	(78)/–	–	–	(28)	–	–	(71)
DA, DB	MSS	(60)	66/(52)	–	(66)/–	(55)	(58)	–	–	–	(61)
	IS	(60)	(52)	(40)	(66)/–	–	–	–	–	–	(61)
	LSS	(60)	(52)	(40)	(66)/–	–	–	–	–	–	(61)
C_n	MSS	(35)	37/(19)	–	(41)/–	(31)	(29)	–	–	–	36
	IS	(35)	(19)	–	(41)/–	–	–	–	–	–	(33)
	LSS	(35)	(19)	–	(41)/–	–	–	–	–	–	(33)
I_{8-0}	MSS	(72)/96	89/79	–	(80)/33	(71)/91	(69)/91	–	–	(26)	76/98
	IS	(72)/96	(69)/79	(56)/79	(80)/–	–	–	–	–	(26)	(75)/98*
	LSS	(72)/96	(69)/79	(56)/79	(80)/–	–	–	–	(36)	(26)	(75)/98*
CP	MSS	(60)/97	51/80	–	(67)/34	(55)/74	(58)/74	(22)	–	(22)	(61)/93
	IS	(60)	(42)	(43)	(67)/–	–	–	(22)	–	(22)	(61)
	LSS	(60)	(42)	(43)	(67)/–	–	–	(22)	–	(22)	(61)
Z	MSS	–	–	–	–	–	–	–	–	–	–
	IS	–/63	–/46	–/46	–	–	–	–	–	–	–/65
	LSS	–/63	–/46	–/46	–	–	–	–	–	–	–/65
SIO_0, SIO_3	Any	(26)	–	–	–	–	–	–	–	–	–

NOTES:

1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.
3. A number in parentheses means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.
4. Double Length Normalize and First Divide Op
   SFA: $F = S + C_n$
   Y = Log. 2F
   Q = Log. 2Q
   $SIO_3 = F_3 \oplus R_3$ (MSS)
   $C_{n+4} = \overline{F_3} \oplus \overline{F_2}$ (MSS)
   $OVR = F_2 \oplus F_1$ (MSS)
   $Z = \overline{Q_0}\,\overline{Q_1}\,\overline{Q_2}\,\overline{Q_3}\,\overline{F_0}\,\overline{F_1}\,\overline{F_2}\,\overline{F_3}$

   Two's Complement Divide
   SFC: $F = R + S + C_n$ if $Z = 0$
   $F = S - R - 1 + C_n$ if $Z = 1$
   Y = Log. 2F
   Q = Log. 2Q
   $SIO_3 = \overline{F_3} \oplus \overline{R_3}$ (MSS)
   $Z = \overline{F_3} \oplus \overline{R_3}$ (MSS) from previous cycle

   Two's Complement Divide Correction and Remainder
   SFE: $F = R + S + C_n$ if $Z = 0$
   $F = S - R - 1 + C_n$ if $Z = 1$
   $Y = F$
   Q = Log. 2Q
   $Z = F_3 \oplus R_3$ (MSS) from previous cycle

IDT39C203 GUARANTEED MILITARY RANGE PERFORMANCE BCD INSTRUCTIONS (SF1, SF7, SF9, SFB, SFD, SFF)

FROM	TO												
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DA, DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_0	SIO_3	SIO_0 PARITY
A, B Addr	MSS	75	65	–	(78)	70	70	(28)	–	–	60	(71)	(84)
	IS	75	65	57	(78)	–	–	(28)	–	–	60	(71)	(84)
	LSS	75	65	57	(78)	–	–	(28)	–	–	60	(71)	(84)
DA, DB	MSS	62	54	–	70	64	64	–	–	–	50	(61)	(74)
	IS	62	54	50	70	–	–	–	–	–	50	(61)	(74)
	LSS	62	54	50	70	–	–	–	–	–	50	(61)	(74)
C_n	MSS	39	26	–	(41)	37	37	–	–	–	34	39	48
	IS	39	26	–	(41)	–	–	–	–	–	34	39	48
	LSS	39	26	–	(41)	–	–	–	–	–	34	39	48
I_{8-0}	MSS	76	72	–	(80)/50[1]	73	73	–	–	(26)	(58)	(75)	(89)
	IS	76	72	70	(80)/50[1]	–	–	–	–	(26)	(58)	(75)	(89)
	LSS	76	72	70	(80)/50[1]	–	–	–	(36)	(26)	(58)	(75)	(89)
CP	MSS	67	54	–	70/34[1]	66	66	(22)	–	(22)	43	63	74
	IS	67	54	52	70/34[1]	–	–	(22)	–	(22)	43	63	74
	LSS	67	54	52	70/34[1]	–	–	(22)	–	(22)	43	63	74
SIO_{0-3}	Any	(26)	–	–	–	–	–	–	–	–	–	–	–

NOTES:

1. Binary-to-BCD and multiprecision Binary-to-BCD instructions only.
2. BCD-to-binary conversion (SF1), Binary-to-BCD conversion (SF9), BCD subtract (SFD, SFF), BCD divide by two (SF7), BCD add (SFB)
3. A number is parentheses means the delay path is the same as specified in the Standard Functions and Increment by One or Two Instructions Table. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.

8

IDT39C203 GUARANTEED MILITARY RANGE PERFORMANCE
SIGN MAGNITUDE TO TWO'S COMPLEMENT CONVERSION (SF5)

FROM	TO										
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DA, DB	$\overline{WRITE}$/ MSS	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	114	98	–	52	106	106	(28)	–	–	128
	IS	(70)	(58)	(52)	–	–	–	(28)	–		(71)
	LSS	(70)	(58)	(52)	–	–	–	(28)			(71)
DA, DB	MSS	108	92	–	46	101	101	–		–	112
	IS	(60)	(52)	(40)	–	–	–	–	–	–	(61)
	LSS	(60)	(52)	(40)	–	–	–	–	–	–	(61)
C_n	MSS	36	(19)	–	–	35	(29)	–	–	–	(33)
	IS	(35)	(19)	–	–	–	–	–	–	–	(33)
	LSS	(35)	(19)	–	–	–	–	–	–	–	(33)
I_{8-0}	MSS	98	79	–	33	97	88	–	–	(26)	109*
	IS	98	79	73	–	–	–	–	–	(26)	109*
	LSS	98	79	73	–	–	–	–	(36)	(26)	109*
CP	MSS	108	92	–	46	101	101	(22)	–	(22)	122
	IS	(60)	(42)	(43)	–	–	–	(22)	–	(22)	(61)
	LSS	(60)	(42)	(43)	–	–	–	(22)	–	(22)	(61)
Z	MSS	–	–	–	–	–	–	–	–	–	–
	IS	65	46	40	–	–	–	–	–	–	76
	LSS	65	46	40	–	–	–	–	–	–	76
SIO_0, SIO_3	Any	(26)	–	–	–	–	–	–	–	–	–

NOTES:

1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.
3. A number is parentheses means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.
4. SF5: $F = S + C_n$ if $Z = 0$, $F = \overline{S} + C_n$ if $Z = 1$. $Y_3 = S_3 \oplus F_3$(MSS), $Z = S_3$(MSS), $Y = F$. $Q = Q$, $N = F$ if $Z = 0$, $N = \overline{S}$ if $Z = 1$.

IDT39C203 GUARANTEED MILITARY RANGE PERFORMANCE SINGLE LENGTH NORMALIZATION (SF8)

FROM		TO									
	SLICE	Y	C_{n+4}	$\overline{G}, \overline{P}$	Z	N	OVR	DA, DB	$\overline{WRITE}$	$QIO_{0,3}$	SIO_3
A, B Addr	MSS	(70)	–	–	–	–	–	(28)	–	–	(71)
	IS	(70)	(58)	(52)	–	–	–	(28)	–	–	(71)
	LSS	(70)	(58)	(52)	–	–	–	(28)	–	–	(71)
DA, DB	MSS	(60)	–	–	–	–	–	–	–	–	(61)
	IS	(60)	(52)	(40)	–	–	–	–	–	–	(61)
	LSS	(60)	(52)	(40)	–	–	–	–	–	–	(61)
C_n	MSS	(35)	–	–	–	–	–	–	–	–	(33)
	IS	(35)	(19)	–	–	–	–	–	–	–	(33)
	LSS	(35)	(19)	–	–	–	–	–	–	–	(33)
I_{8-0}	MSS	(72)	47	–	33	27	27	–	–	(26)	(75)*
	IS	(72)	(69)	(56)	33	–	–	–	–	(26)	(75)*
	LSS	(72)	(69)	(56)	33	–	–	–	(36)	(26)	(75)*
CP	MSS	(60)	31	–	34	26	31	(22)	–	(22)	(61)
	IS	(60)	(42)	(43)	34	–	–	(22)	–	(22)	(61)
	LSS	(60)	(42)	(43)	34	–	–	(22)	–	(22)	(61)
Z	MSS	–	–	–	–	–	–	–	–	–	–
	IS	–	–	–	–	–	–	–	–	–	–
	LSS	–	–	–	–	–	–	–	–	–	–
SIO_0, SIO_3	Any	(26)	–	–	–	–	–	–	–	–	–

NOTES:

1. A "–" means the delay path does not exist.
2. An "*" means the output is enabled or disabled by the input. See enable and disable times. A number shown with an "*" is the delay to correct data on an enabled output. This specification is not tested but is guaranteed by correlation to the Standard Function and Increment by One or Two Instruction Test.
3. A number in parentheses means the delay is the same as in the Standard Functions and Increment by One or Two Instructions Table.
4. SF8: $F = S + C_n$ $C_{n+4} = Q_3 \oplus Q_2$ (MSS) $OVR = Q_2 \oplus Q_1$ (MSS)
   $N = Q_3$ (MSS) $Z = \overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3$
   $Y = F$
   Q = Log. 2Q

8

IDT39C203 INPUT/OUTPUT INTERFACE CIRCUITRY

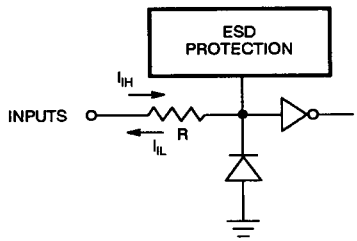


Figure 3. Input Structure (All Inputs)

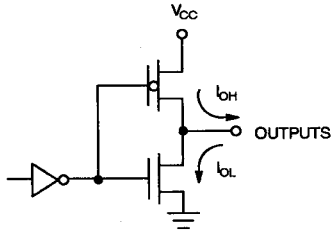


Figure 4. Output Structure (All Outputs)

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 6

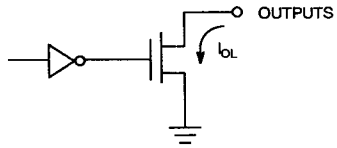


Figure 5. Open Drain Structure

TEST LOAD CIRCUIT

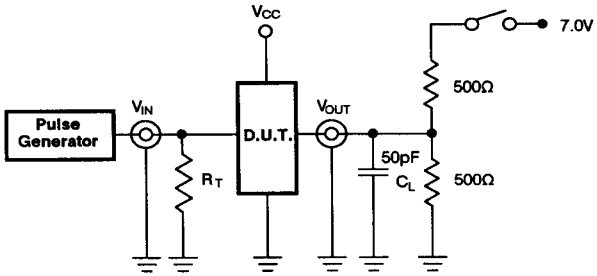


Figure 6. Switching Test Circuits (All Outputs)

SWITCH POSITION

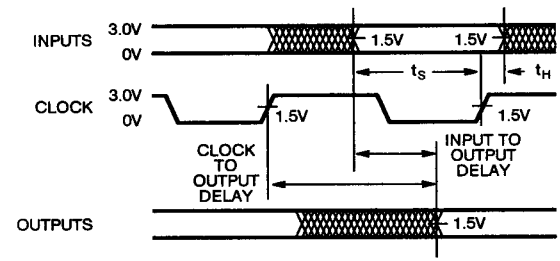
TEST	SWITCH
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

DEFINITIONS

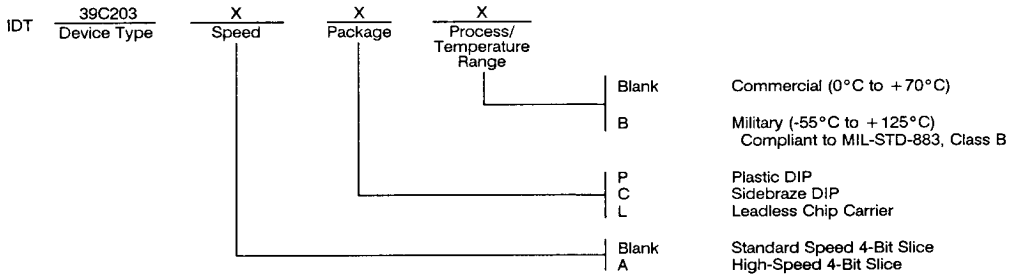
C_L = Load capacitance: includes jig and probe capacitance

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator

SWITCHING WAVEFORMS



ORDERING INFORMATION



8