



Integrated Device Technology, Inc.

## 16-BIT CMOS ERROR DETECTION AND CORRECTION UNIT

IDT39C60  
IDT39C60-1  
IDT39C60A  
IDT39C60B

### FEATURES:

- Low-power CMOS Technology
- Fast
  - Data In to Error Detect  
IDT39C60B: 18ns (max.), IDT39C60A: 20ns (max.)  
IDT39C60-1: 25ns (max.), IDT39C60: 32ns (max.)
  - Data In to Corrected Data Out  
IDT39C60B: 25ns (max.), IDT39C60A: 30ns (max.)  
IDT39C60-1: 52ns (max.), IDT39C60: 65ns (max.)
- Improves system memory reliability
  - Corrects all single-bit errors, detects all double and some triple-bit errors
- Cascadable
  - Data words up to 64 bits
- Built-in diagnostics
  - Capable of verifying proper EDC operation via software control
- Simplifies byte operations
  - Fast byte writes possible with separate byte enables
- Available in 48-pin DIP, 48 pin ceramic flatpack, 52-pin PLCC
- Pin-compatible to all versions of the AMD2960
- Military product available compliant to MIL-STD-883, Class B
- Standard Military Drawing #5962-88613 available

### DESCRIPTION:

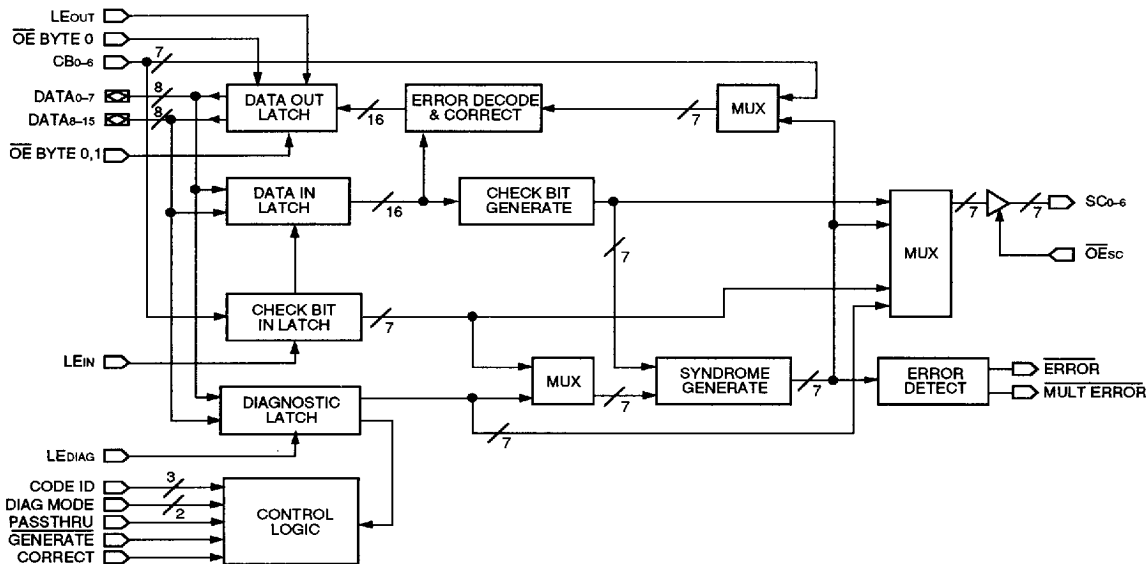
The IDT39C60 family are high-speed, low-power, 16-bit Error Detection and Correction Units which generate checkbits on a 16-bit data field according to a modified Hamming Code and correct the data word when checkbits are supplied. When performing a read operation from memory, the IDT39C60s will correct 100% of all single-bit errors and will detect all double-bit errors and some triple bit errors.

The IDT39C60s are easily cascadable from 16-bits up to 64-bits. Sixteen-bit systems use 6 check bits, 32-bit systems use 7 check bits and 64-bit systems use 8 check bits. For all three configurations, the error syndrome is made available.

All parts have 2 built-in diagnostic modes. Both simplify testing by allowing diagnostic data to be entered into the device to execute system diagnostic functions.

The IDT39C60s are pin-compatible, performance-enhanced functional replacements for all versions of the AMD 2960. They are fabricated using advanced dual metal CMOS technology. Military grade product is manufactured in compliance to the latest revision of MIL-STD-883, Class B.

### FUNCTIONAL BLOCK DIAGRAM



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MILITARY AND COMMERCIAL TEMPERATURE RANGES

APRIL 1994

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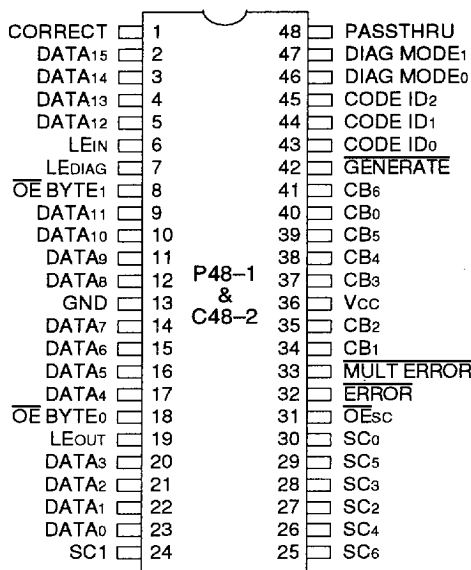
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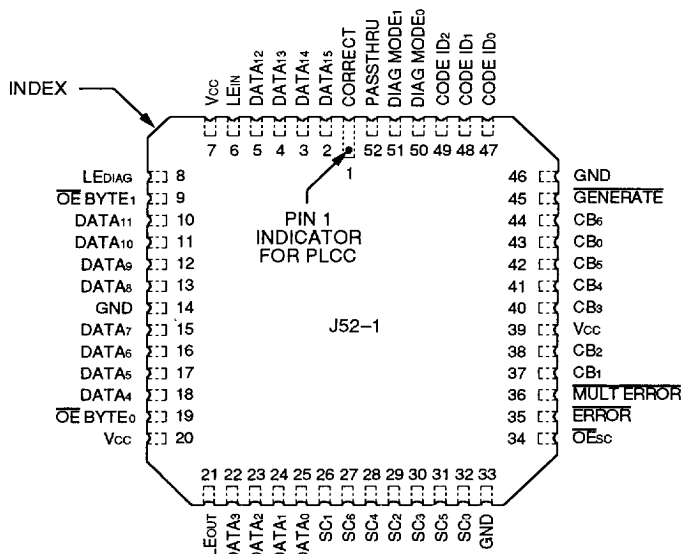
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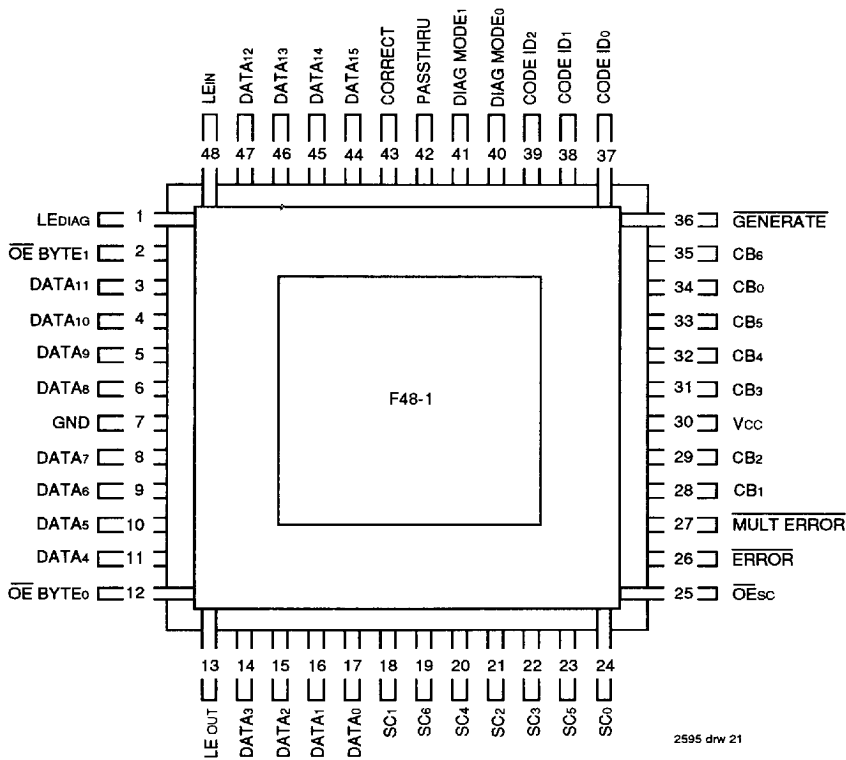
## PIN CONFIGURATIONS



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2595 drw 03



FLATPACK  
TOP VIEW

## PIN DESCRIPTIONS

| Pin Name                   | I/O | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|----------------------------|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| DATA0-15                   | I/O | 16 bidirectional data lines provide input to the Data Input Latch and receive output from the Data Output Latch. DATA0 is the least significant bit; DATA15 the most significant bit.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| CB0-6                      | I   | Seven check bit input lines are used to input check bits for error detection. Also used to input syndrome bits for error correction in 32- and 64-bit configurations.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| LEIN                       | I   | Latch Enable — Data Input Latch. Controls latching of the input data. When HIGH, the Data Input Latch and Check Bit Input Latch follow the input data and input check bits. When LOW, the Data Input Latch and Check Bit Input Latch are latched to their previous state.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| GENERATE                   | I   | Generate Check Bits input. When this input is LOW, the EDC is in the Check Bit Generate mode. When HIGH, the EDC is in the Detect mode or Correct mode. In the Generate mode, the circuit generates the check bits or partial check bits specific to the data in the Data Input Latch. The generated check bits are placed on the SC outputs. In the Detect or Correct modes the EDC detects single and multiple errors and generates syndrome bits based upon the contents of the Data Input Latch and Check Bit Input Latch. In Correct mode, single-bit errors are also automatically corrected — corrected data is placed at the input of the Data Output Latch. The syndrome result is placed on the SC outputs and indicates, in a coded form, the number of errors and the bit-in-error. |
| SC0-6                      | O   | Syndrome/Check Bit outputs hold the check/partial check bits when the EDC is in Generate mode and will hold the syndrome/partial syndrome bits when the device is in Detect or Correct modes. These are 3-state outputs.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| OE <sub>SC</sub>           | I   | Output Enable — Syndrome/Check Bits. When LOW, the 3-state output lines SC0-6 are enabled. When HIGH, the SC outputs are in the high impedance state.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| ERROR                      | O   | Error Detected output. When the EDC is in Detect or Correct mode, this output will go LOW if one or more syndrome bits are asserted, meaning there are one or more bit errors in the data or check bits. If no syndrome bits are asserted, there are no errors detected and the output will be HIGH. In Generate mode, ERROR is forced HIGH. (In a 64-bit configuration, ERROR must be implemented externally.)                                                                                                                                                                                                                                                                                                                                                                                 |
| MULT ERROR                 | O   | Multiple Errors Detected output. When the EDC is in Detect or Correct mode this output, if LOW, indicates that there are two or more bit errors that have been detected. If HIGH, this indicates that either one or no errors have been detected. In Generate mode, MULT ERROR is forced HIGH. (In a 64-bit configuration, MULT ERROR must be implemented externally.)                                                                                                                                                                                                                                                                                                                                                                                                                          |
| CORRECT                    | I   | Correct input. When HIGH, this signal allows the correction network to correct any single-bit error in the Data Input Latch (by complementing the bit-in-error) before putting it into the Data Output Latch. When LOW, the EDC will drive data directly from the Data Input Latch to the Data Output Latch without correction.                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| LEOUT                      | I   | Latch Enable — Data Output Latch. Controls the latching of the Data Output Latch. When LOW, the Data Output Latch is latched to its previous state. When HIGH, the Data Output Latch follows the output of the Data Input Latch as modified by the correction logic network. In Correct mode, single-bit errors are corrected by the network before loading into the Data Output Latch. In Detect mode, the contents of the Data Input Latch are passed through the correction network unchanged into the Data Output Latch. The inputs to the Data Output Latch are disabled with its contents unchanged if the EDC is in Generate mode.                                                                                                                                                       |
| OE BYTE0<br>OE BYTE1       | I   | Output Enable — Bytes 0 and 1. Data Output Latch controls the 3-state outputs for each of the two bytes of the Data Output Latch. When LOW, these lines enable the Data Output Latch and, when HIGH, these lines force the Data Output Latch into the high impedance state. The two enable lines can be separately activated to enable only one byte of the Data Output at a time.                                                                                                                                                                                                                                                                                                                                                                                                              |
| PASSTHRU                   | I   | PASSTHRU input, when HIGH, forces the contents of the Check Bit Input Latch onto the Syndrome/Check Bit outputs (SC0-6) and the unmodified contents of the Data Input Latch onto the inputs of the Data Output Latch.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| DIAG MODE0-1<br>CODE ID0-2 | I   | Diagnostic Mode Select controls the initialization and diagnostic operation of the EDC. Code Identification inputs identify the size of the total data word to be processed and which 16-bit slice of larger data words a particular EDC is processing. The three allowable data word sizes are 16/32- and 64-bits and their respective modified Hamming Codes are designated 16/22, 32/39 and 64/72. Special CODE ID input 001 (ID2, ID1, ID0) is also used to instruct the EDC that the signals CODE ID0-2, DIAG MODE0-1, CORRECT and PASSTHRU are to be taken from the diagnostic latch rather than the control lines.                                                                                                                                                                       |
| LEDIAG                     | I   | Latch Enable — Diagnostic Latch. The Diagnostic Latch follows the 16-bit data on the input lines when HIGH. When LOW, the outputs of the Diagnostic Latch are latched to their previous states. The Diagnostic Latch holds diagnostic check bits and internal control signals for CODE ID0-2, DIAG MODE0-1, CORRECT and PASSTHRU.                                                                                                                                                                                                                                                                                                                                                                                                                                                               |

2595 tbi 01

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## PRODUCT DESCRIPTION

The IDT39C60 EDC Unit is a powerful 16-bit cascaded slice used for check bit generation, error detection, error correction and diagnostics. As shown in the Functional Block Diagram, the device consists of the following:

- Data Input Latch
- Data Output Latch
- Diagnostic Latch
- Check Bit Input Latch
- Check Bit Generation Logic
- Syndrome Generation Logic
- Error Detection Logic
- Error Correction Logic
- Control Logic

## DATA INPUT/OUTPUT/DIAGNOSTIC LATCHES

The LEIN, Latch Enable input, controls the Data Input which can load 16 bits of data from the bidirectional DATA lines. The input data is used for either check bit generation or error detection/correction.

The 16 bits of data from the DATA lines can be loaded into the Diagnostic Latch under control of the Diagnostic Latch Enable, LEDIAG, giving check bit information in one byte and control information in the other byte. The Diagnostic Latch is used when in Internal Control mode or in one of the Diagnostics modes.

The Data Output Latch is split into two bytes and enabled onto the DATA lines through separate byte control lines. The Data Output Latch stores the result of an error correction operation or is loaded directly from the Data Input Latch under control of the Latch Enable Out (LEOUT). The PASSTHRU control input determines which data is loaded.

## CHECK BIT GENERATION LOGIC

This block of combinational logic generates 7 check bits using a modified Hamming Code from the 16 bits of data input from the Data Input Latch.

## SYNDROME GENERATION LOGIC

This logic compares the check bits generated through the Check Bit Generator with either the check bits in the Check Bit Input Latch or 7 bits assigned in the Diagnostic Latch.

Syndrome bits are produced by an exclusive-OR of the two sets of bits. A match indicates no errors. If errors occur, the syndrome bits can be decoded to indicate the bit in error, whether 2 errors were detected or 3 or more errors.

## ERROR DETECTION/CORRECTION LOGIC

The syndrome bits generated by the Syndrome Logic are decoded and used to control the ERROR and MULTERROR outputs. If one or more errors are detected,

ERROR goes low. If two or more errors are detected, both ERROR and MULTERROR go low. Both outputs remain high when there are no errors detected.

For single bit errors, the correction logic will complement (correct) the bit in error, which can then be loaded into the Data Out Latches under the LEOUT control. If check bit errors need to be corrected, then the device must be operated in the Generate mode.

## CONTROL LOGIC

The control logic determines the specific mode of operation, usually from external control signals. However, the Internal Control mode allows these signals to be provided from the Diagnostic Latch.

## DETAILED PRODUCT DESCRIPTION

The IDT39C60 EDC unit contains the logic necessary to generate check bits on a 16-bit data input according to a modified Hamming Code. The EDC can compare internally generated check bits against those read with the 16-bit data to correct any single bit data error and detection of all double and some triple bit errors. The IDT39C60 can be used for 16-bit data words (6 check bits), 32-bit data words (7 check bits) or 64-bit data words (8 check bits).

## CODE AND BYTE SELECTION

The 3 code identification pins, ID0-2, are used to determine the data word size from 16, 32 or 64 bits and the byte position of each 16-bit IDT39C60 EDC device.

Code 16/22 refers to a 16-bit data field with 6 check bits.

Code 32/39 refers to a 32-bit data field with 7 check bits.

Code 64/72 refers to a 64-bit data field with 8 check bits.

The ID0-2 of 001 is used to place the device in the Internal Control mode as described later in this section.

Table 1 defines all possible identification codes.

## CHECK AND SYNDROME BITS

The IDT39C60 provides either check bits or syndrome bits on the three-state output pins, SC0-6. Check bits are generated from a combination of the Data Input bits, while syndrome bits are an Exclusive-OR of the check bits generated from read data with the read check bits stored with the data. Syndrome bits can be decoded to determine the single bit-in-error or that a double error was detected. Some triple bit errors are also detected. The check bits are labeled:

|                                |                              |
|--------------------------------|------------------------------|
| Co, C1, C2, C3, C4             | for the 8-bit configuration  |
| Co, C1, C2, C3, C4, C5         | for the 16-bit configuration |
| Co, C1, C2, C3, C4, C5, C6     | for the 32-bit configuration |
| Co, C1, C2, C3, C4, C5, C6, C7 | for the 64-bit configuration |

Syndrome bits are similarly labeled So through S7.

## CONTROL MODE SELECTION

Tables 2 and 3 describe the 9 operating modes of the IDT39C60. The Diagnostic mode pins, DIAG MODE<sub>0-1</sub>, define 4 basic areas of operation, with GENERATE, CORRECT and PASSTHRU, further dividing operation into 8 functions with the ID<sub>0-2</sub> defining the ninth mode as the Internal mode.

Generate mode is used to display the check bits on the outputs SC<sub>0-6</sub>. The Diagnostic Generate mode displays check bits as stored in the Diagnostic Latch.

Detect mode provides an indication of errors or multiple errors on the outputs ERROR and MULTERROR. Single bit errors are not corrected in this mode. The syndrome bits are provided on the outputs SC<sub>0-6</sub>. For the Diagnostic Detect mode, the syndrome bits are generated by comparing the internally generated check bits from the Data In Latch with check bits stored in the diagnostic latch rather than with the check bit latch contents.

Correct mode is similar to the Detect mode except that

single bit errors will be complemented (corrected) and made available as input to the Data Out Latch. Again, the Diagnostic Correct mode will correct single bit errors as determined by syndrome bits generated from the Data Input and contents of the Diagnostic Latch.

The Initialize mode provides check bits for all zero bit data. Data In Latch is set and latched to a logic zero and made available as input to the Data Out Latch.

The Internal mode disables the external control pins DIAG MODE<sub>0-1</sub>, CORRECT, PASSTHRU and CODE ID to be defined by the Diagnostic Latch. When in the internal control mode, the data loaded into the diagnostic latch should have the CODE ID different from 001 as this would represent an invalid operation.

| CODE ID <sub>2</sub> | CODE ID <sub>1</sub> | CODE ID <sub>0</sub> | Hamming Code and Slice Selected |
|----------------------|----------------------|----------------------|---------------------------------|
| 0                    | 0                    | 0                    | Code 16/22                      |
| 0                    | 0                    | 1                    | Internal Control Mode           |
| 0                    | 1                    | 0                    | Code 32/39, Byte 0 and 1        |
| 0                    | 1                    | 1                    | Code 32/39, Byte 2 and 3        |
| 1                    | 0                    | 0                    | Code 64/72, Byte 0 and 1        |
| 1                    | 0                    | 1                    | Code 64/72, Byte 2 and 3        |
| 1                    | 1                    | 0                    | Code 64/72, Byte 4 and 5        |
| 1                    | 1                    | 1                    | Code 64/72, Byte 6 and 7        |

2595 tbl 02

Table 1. Hamming Code and Slice Identification

| DIAG MODE <sub>1</sub> | DIAG MODE <sub>2</sub> | Diagnostic Mode Selected                                                                                                                                                                                                                |
|------------------------|------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0                      | 0                      | <b>Non-diagnostic mode.</b> The EDC functions normally in all modes.                                                                                                                                                                    |
| 0                      | 1                      | <b>Diagnostic Generate.</b> The contents of the Diagnostic Latch are substituted for the normally generated check bits when in the Generate mode. The EDC functions normally in the Detect or Correct modes.                            |
| 1                      | 0                      | <b>Diagnostic Detect/Correct.</b> In the Detect or Correct mode, the contents of the Diagnostic Latch are substituted for the check bits normally read from the Check Bit Input Latch. The EDC functions normally in the Generate mode. |
| 1                      | 1                      | <b>Initialize.</b> The outputs of the Data Input Latch are forced to zeroes and the check bits generated correspond to the all zero data. The latch is not reset, a functional difference from the Am2960.                              |

2595 tbl 03

Table 2. Diagnostic Mode Control

| Operating Mode      | DM <sub>1</sub>                                                                                                                                   | DM <sub>0</sub>  | GENERATE | CORRECT | PASS-THRU | DATA <sub>OUT</sub> Latch (LE <sub>OUT</sub> = High) | SC <sub>0-6</sub> (OE <sub>SC</sub> = Low)                | ERROR<br>MULT ERROR      |
|---------------------|---------------------------------------------------------------------------------------------------------------------------------------------------|------------------|----------|---------|-----------|------------------------------------------------------|-----------------------------------------------------------|--------------------------|
| Generate            | 0<br>1                                                                                                                                            | 0<br>0           | 0        | X       | 0         | —                                                    | Check Bits Generated from DATA <sub>IN</sub> Latch        | High                     |
| Detect              | 0<br>0                                                                                                                                            | 0<br>1           | 1        | 0       | 0         | DATA <sub>IN</sub> Latch                             | Syndrome Bits DATA <sub>IN</sub> / Check Bit Latch        | Error Dep <sup>(1)</sup> |
| Correct             | 0<br>0                                                                                                                                            | 0<br>1           | 1        | 1       | 0         | DATA <sub>IN</sub> Latch with Single Bit Correction  | Syndrome Bits DATA <sub>IN</sub> / Check Bit Latch        | Error Dep                |
| PASSTHRU            | 0<br>0<br>1<br>1                                                                                                                                  | 0<br>1<br>1<br>0 | X        | X       | 1         | DATA <sub>IN</sub> Latch                             | Check Bit Latch                                           | High                     |
| Diagnostic Generate | 0                                                                                                                                                 | 1                | 0        | X       | 0         | —                                                    | Check Bits from Diagnostic Latch                          | High                     |
| Diagnostic Detect   | 1                                                                                                                                                 | 0                | 1        | 0       | 0         | DATA <sub>IN</sub> Latch                             | Syndrome Bits DATA <sub>IN</sub> / Diagnostic Latch       | Error Dep                |
| Diagnostic Correct  | 1                                                                                                                                                 | 0                | 1        | 1       | 0         | DATA <sub>IN</sub> Latch with Single Bit Correction  | Syndrome Bits DATA <sub>IN</sub> / Diagnostic Latch       | Error Dep                |
| Initialization Mode | 1                                                                                                                                                 | 1                | X        | X       | X         | DATA <sub>IN</sub> Latch Set to 0000                 | Check Bits Generated from DATA <sub>IN</sub> Latch (0000) | —                        |
| Internal Mode       | ID <sub>0-2</sub> = 001 (Control Signals ID <sub>0-2</sub> , DIAG MODE <sub>0-1</sub> , CORRECT and PASSTHRU are taken from the Diagnostic Latch) |                  |          |         |           |                                                      |                                                           |                          |

NOTE:

1. Error Dep (Error Dependent): ERROR will be low for single or multiple errors, with MULTERROR low for double or multiple errors. Both signals are high for no errors.

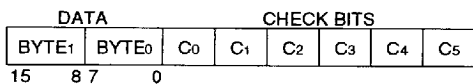
2595 tbl 04

Table 3. IDT39C60 Operating Modes

## 16-BIT DATA WORD CONFIGURATION

Figure 1 indicates the 22-bit data format for two bytes of data and 6 check bits.

A single IDT39C60 EDC unit, connected as shown in Figure 2, provides all the logic needed for single bit error correction and double bit error detection of a 16-bit data field. The identification code 16/22 indicates 6 check bits are required. The CB6 pin is, therefore, a "Don't Care" and ID2, ID1, ID0 = 000.



2595 drw 04

Uses Modified Hamming Code 16/22  
16 Data Bits with 6 Check Bits

Figure 1. 16-Bit Data Format

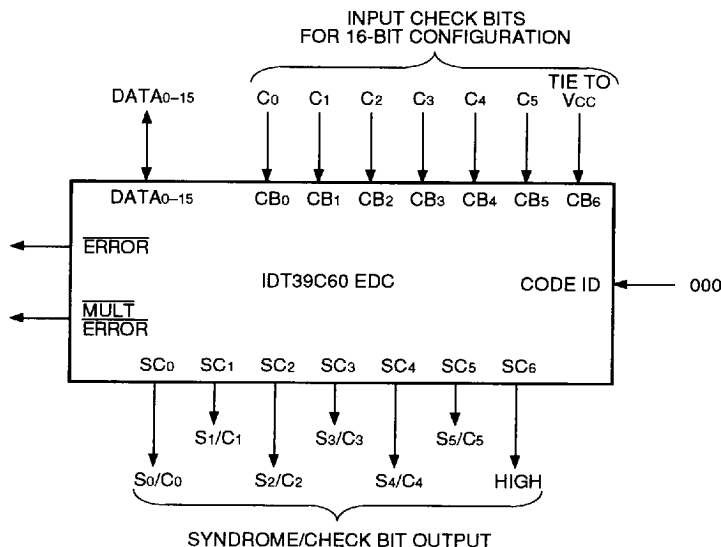


Figure 2. 16-Bit Configuration

Table 3 describes the operating modes available. The output pin SC6, is forced high for either syndrome or check bits since only 6 check bits are used for the 16/22 code.

Table 4 indicates the data bits participating in the check bit generation. For example, check bit C0 is the Exclusive-OR function of the 8 data input bits marked with an X. Check bits are generated and output in the Generate and Initialization Mode. Check bits are passed as stored in the PASSTHRU or Diagnostic Generate Mode.

Syndrome bits are generated by an Exclusive-OR of the generated check bits with the read check bits. For example, SX is the XOR of check bits CX from those read with those generated. Table 5 indicates the decoding of the six

syndrome bits to indicate the bit-in-error for a single bit error, or whether a double or triple bit error was detected. The all zero case indicates no errors detected.

In the Correct Mode, the syndrome bits are used to complement (correct) single bit errors in the data bits. For double or multiple error detection, the data available as input to the Data Out Latch is not defined.

Table 6 defines the bit definition for the Diagnostic Latch. As defined in Table 3, several modes will use the diagnostic check bits to determine syndrome bits or to pass as check bits to the SC0-5 outputs. The Internal Mode substitutes the indicated bit position for the external control signals.



| Generated<br>Check Bits | Participating Data Bits <sup>(1)</sup> |   |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |
|-------------------------|----------------------------------------|---|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|
|                         | Parity                                 | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| C <sub>0</sub>          | Even (XOR)                             |   | X | X | X |   | X |   |   | X | X |    | X  |    |    | X  |    |
| C <sub>1</sub>          | Even (XOR)                             | X | X | X |   | X |   | X |   | X |   | X  |    | X  |    |    |    |
| C <sub>2</sub>          | Odd (XNOR)                             | X |   |   | X | X |   |   | X |   | X | X  |    |    | X  |    | X  |
| C <sub>3</sub>          | Odd (XNOR)                             | X | X |   |   |   | X | X | X |   |   |    | X  | X  | X  |    |    |
| C <sub>4</sub>          | Even (XOR)                             |   |   | X | X | X | X | X | X |   |   |    |    |    |    | X  | X  |
| C <sub>5</sub>          | Even (XOR)                             |   |   |   |   |   |   |   |   | X | X | X  | X  | X  | X  | X  | X  |

NOTE:  
1. The check bit is generated as either an XOR or XNOR of the eight data bits noted by an "X" in the table.

2595 tbl 05

Table 4. 16-Bit Modified Hamming Code — Check Bit Encode Chart

| Hex | Syndrome Bits  |                |                |                | Hex                              | 0 | 1              | 2              | 3  |
|-----|----------------|----------------|----------------|----------------|----------------------------------|---|----------------|----------------|----|
|     | S <sub>3</sub> | S <sub>2</sub> | S <sub>1</sub> | S <sub>0</sub> | S <sub>5</sub><br>S <sub>4</sub> | 0 | 1              | 2              | 3  |
| 0   | 0              | 0              | 0              | 0              |                                  | * | C <sub>4</sub> | C <sub>5</sub> | T  |
| 1   | 0              | 0              | 0              | 1              | C <sub>0</sub>                   | T | T              | T              | 14 |
| 2   | 0              | 0              | 1              | 0              | C <sub>1</sub>                   | T | T              | T              | M  |
| 3   | 0              | 0              | 1              | 1              | T                                | 2 | 8              | T              |    |
| 4   | 0              | 1              | 0              | 0              | C <sub>2</sub>                   | T | T              | 15             |    |
| 5   | 0              | 1              | 0              | 1              | T                                | 3 | 10             | T              |    |
| 6   | 0              | 1              | 1              | 0              | T                                | 4 | 9              | T              |    |
| 7   | 0              | 1              | 1              | 1              | M                                | T | T              | M              |    |
| 8   | 1              | 0              | 0              | 0              | C <sub>3</sub>                   | T | T              | M              |    |
| 9   | 1              | 0              | 0              | 1              | T                                | 5 | 11             | T              |    |
| A   | 1              | 0              | 1              | 0              | T                                | 6 | 12             | T              |    |
| B   | 1              | 0              | 1              | 1              | 1                                | T | T              | M              |    |
| C   | 1              | 1              | 0              | 0              | T                                | 7 | 13             | T              |    |
| D   | 1              | 1              | 0              | 1              | M                                | T | T              | M              |    |
| E   | 1              | 1              | 1              | 0              | 0                                | T | T              | M              |    |
| F   | 1              | 1              | 1              | 1              | T                                | M | M              | T              |    |

NOTES:  
\* = No errors detected  
Number = The number of the single bit-in-error  
T = Two errors detected  
M = Three or more errors detected

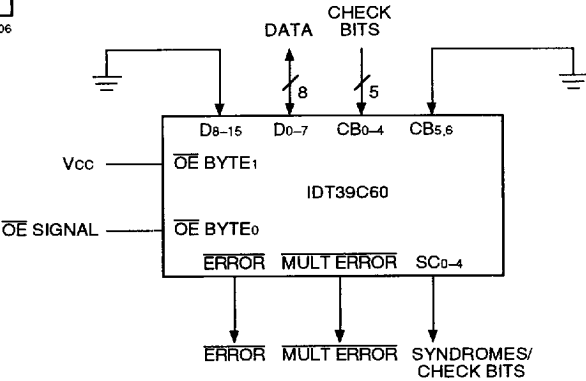
2595 tbl 06

Table 5. Syndrome Decode to Bit-In-Error (16-Bit Configuration)

| Data Bit | Internal Function                 |
|----------|-----------------------------------|
| 0        | Diagnostic Check Bit <sub>0</sub> |
| 1        | Diagnostic Check Bit <sub>1</sub> |
| 2        | Diagnostic Check Bit <sub>2</sub> |
| 3        | Diagnostic Check Bit <sub>3</sub> |
| 4        | Diagnostic Check Bit <sub>4</sub> |
| 5        | Diagnostic Check Bit <sub>5</sub> |
| 6, 7     | Don't Care                        |
| 8        | CODE ID <sub>0</sub>              |
| 9        | CODE ID <sub>1</sub>              |
| 10       | CODE ID <sub>2</sub>              |
| 11       | DIAG MODE <sub>0</sub>            |
| 12       | DIAG MODE <sub>1</sub>            |
| 13       | CORRECT                           |
| 14       | PASSTHRU                          |
| 15       | Don't Care                        |

2595 tbl 07

Table 6. Diagnostic Latch Loading — 16-Bit Format



2595 drw 06

Figure 3. 8-Bit Configuration

**32-BIT DATA WORD CONFIGURATION**

Two IDT39C60 EDC units, connected as shown in Figure 5, provide all the logic needed for single bit error correction and double bit error detection of a 32-bit data field. The identification code 32/39 indicates 7 check bits are required. Table 1 gives the ID2, ID1, ID0 values needed for distinguishing the byte 0/1 from byte 2/3. Valid syndrome, check bits and the **ERROR** and **MULTERROR** signal come from the byte 2/3 unit. Control signals not indicated are connected to both units in parallel. The  $\overline{OE}$  always enables the SC0-6 outputs of byte 0/1, but must be used to select data check bits or syndrome bits fed back from the byte 2/3 for data correction modes.

Data In bits 0 through 15 are connected to the same numbered inputs of the byte 0/1 EDC unit, while Data In bits 16 through 31 are connected to byte 2/3 Data Inputs 0 to 15, respectively.

Figure 4 indicates the 39-bit data format for 4 bytes of data and 7 check bits. Check bits are input to the byte 0/1 unit through a tri-state buffer unit such as the IDT74FCT244. Correction of single bit errors of the 32-bit configuration requires a feedback of syndrome bits from byte 2/3 into the byte 0/1 unit. The MUX shown on the functional block diagram is used to select the CB0-6 pins as the syndrome bits rather than internally generated syndrome bits.

Table 3 describes the operating mode available for the 32/39 configuration.

Syndrome bits are generated by an Exclusive-OR of the generated check bits with the read check bits. For example,  $S_n$  is the XOR of check bits  $C_n$  from those read with those generated. Table 7 indicates the decoding of the seven syndrome bits to determine the bit-in-error for a single bit error, or whether a double or triple bit error was detected. The all zero case indicates no errors detected.

In the Correct Mode, the syndrome bits are used to complement (correct) single bit errors in the data bits. For double or multiple error detection, the data available as input to the Data Out Latch is not defined.

Performance data is provided in Table 8 in relating a single IDT39C60 EDC with the two cascaded units of Figure 5. As indicated, a summation of propagation delays is required from the cascading arrangement of EDC units.

Table 9 defines the bit definition for the Diagnostic Latch. As defined in Table 3, several modes will use the Diagnostic check bits to determine syndrome bits or to pass as check bits to the SC0-6 outputs. The Internal Mode substitutes the indicated bit position for the external control signals.

Table 10 indicates the data bits participating in the check bit generation. For example, check bit  $C_0$  is the Exclusive-OR function of the 16 data input bits marked with an X. Check bits are generated and output in the Generate and Initialization Mode. Check bits are passed as stored in the PASSTHRU or Diagnostic Generate Mode.

|               |    |    |    |    | Hex | 0  | 1  | 2  | 3  | 4 | 5  | 6  | 7 |
|---------------|----|----|----|----|-----|----|----|----|----|---|----|----|---|
| Syndrome Bits |    |    |    |    | S6  | 0  | 0  | 0  | 0  | 1 | 1  | 1  | 1 |
|               |    |    |    |    | S5  | 0  | 0  | 1  | 1  | 0 | 0  | 1  | 1 |
|               |    |    |    |    | S4  | 0  | 1  | 0  | 1  | 0 | 1  | 0  | 1 |
| Hex           | S3 | S2 | S1 | S0 |     |    |    |    |    |   |    |    |   |
| 0             | 0  | 0  | 0  | 0  | *   | C4 | C5 | T  | C6 | T | T  | 30 |   |
| 1             | 0  | 0  | 0  | 1  | C0  | T  | T  | 14 | T  | M | M  | T  |   |
| 2             | 0  | 0  | 1  | 0  | C1  | T  | T  | M  | T  | 2 | 24 | T  |   |
| 3             | 0  | 0  | 1  | 1  | T   | 18 | 8  | T  | M  | T | T  | M  |   |
| 4             | 0  | 1  | 0  | 0  | C2  | T  | T  | 15 | T  | 3 | 25 | T  |   |
| 5             | 0  | 1  | 0  | 1  | T   | 19 | 9  | T  | M  | T | T  | 31 |   |
| 6             | 0  | 1  | 1  | 0  | T   | 20 | 10 | T  | M  | T | T  | M  |   |
| 7             | 0  | 1  | 1  | 1  | M   | T  | T  | M  | T  | 4 | 26 | M  |   |
| 8             | 1  | 0  | 0  | 0  | C3  | T  | T  | M  | T  | 5 | 27 | T  |   |
| 9             | 1  | 0  | 0  | 1  | T   | 21 | 11 | T  | M  | T | T  | M  |   |
| A             | 1  | 0  | 1  | 0  | T   | 22 | 12 | T  | 1  | T | T  | M  |   |
| B             | 1  | 0  | 1  | 1  | 17  | T  | T  | M  | T  | 6 | 28 | T  |   |
| C             | 1  | 1  | 0  | 0  | T   | 23 | 13 | T  | M  | T | T  | M  |   |
| D             | 1  | 1  | 0  | 1  | M   | T  | T  | M  | T  | 7 | 29 | T  |   |
| E             | 1  | 1  | 1  | 0  | 16  | T  | T  | M  | T  | M | M  | T  |   |
| F             | 1  | 1  | 1  | 1  | T   | M  | M  | T  | 0  | T | T  | M  |   |

**NOTES:**

\* = No errors detected

Number = The number of the single bit-in-error

T = Two errors detected

M = Three or more errors detected

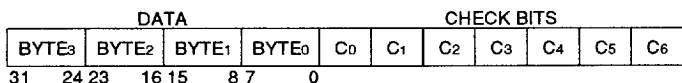
2595 tbl 08

**Table 7. Syndrome Decode to Bit-In-Error (32-Bit Configuration)**

| 32-Bit Propagation Delay |                       | Component Delay From IDT39C60                                     |
|--------------------------|-----------------------|-------------------------------------------------------------------|
| From                     | To                    |                                                                   |
| DATA                     | Check Bits Out        | (DATA to SC) + (CB to SC, CODE ID 011)                            |
| DATA                     | Corrected DATAout     | (DATA to SC) + (CB to SC, CODE ID 011) + CB to DATA, CODE ID 010) |
| DATA                     | Syndromes Out         | (DATA to SC) + (CB to SC, CODE ID 011)                            |
| DATA                     | ERROR for 32 Bits     | (DATA to SC) + (CB to ERROR, CODE ID011)                          |
| DATA                     | MULTERROR for 32 Bits | (DATA to SC) + (CB to MULT ERROR, CODE ID 011)                    |

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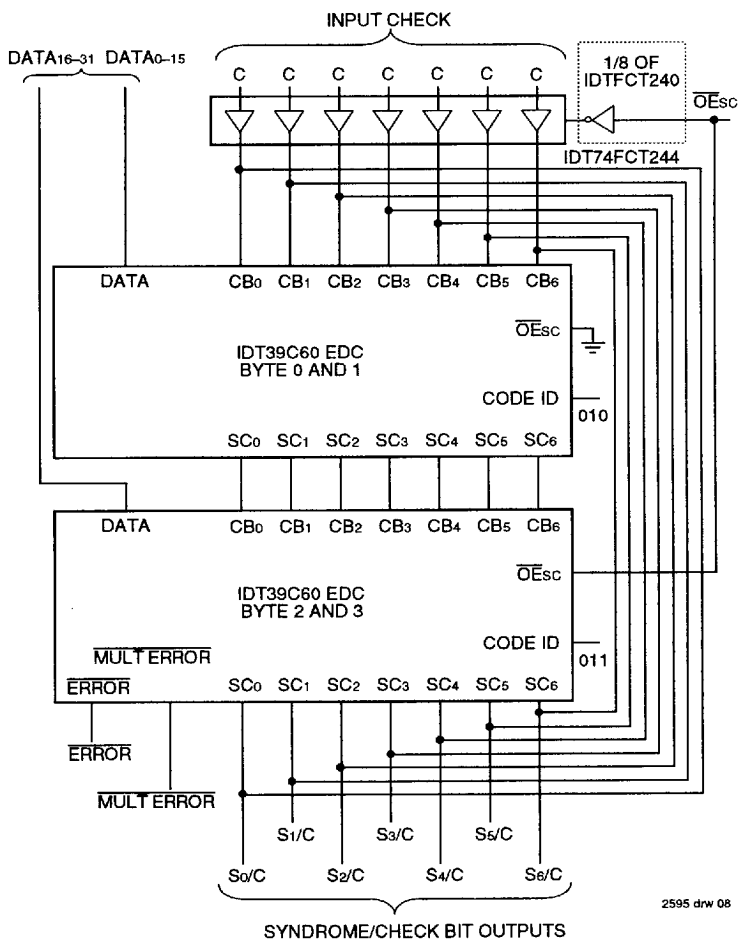
**Table 8. Key AC Calculations for the 32-Bit Configuration**



Uses Modified Hamming Code 32/39  
32 Data Bits with 7 Check Bits

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Figure 4. 32-Bit Data Format



| Data Bit | Internal Function                  |
|----------|------------------------------------|
| 0        | Diagnostic Check Bit0              |
| 1        | Diagnostic Check Bit1              |
| 2        | Diagnostic Check Bit2              |
| 3        | Diagnostic Check Bit3              |
| 4        | Diagnostic Check Bit4              |
| 5        | Diagnostic Check Bit5              |
| 6        | Diagnostic Check Bit6              |
| 7        | Don't Care                         |
| 8        | Slice 0/1 — CODE ID <sub>0</sub>   |
| 9        | Slice 0/1 — CODE ID <sub>1</sub>   |
| 10       | Slice 0/1 — CODE ID <sub>2</sub>   |
| 11       | Slice 0/1 — DIAG MODE <sub>0</sub> |
| 12       | Slice 0/1 — DIAG MODE <sub>1</sub> |
| 13       | Slice 0/1 — CORRECT                |
| 14       | Slice 0/1 — PASSTHRU               |
| 15       | Don't Care                         |
| 16-23    | Don't Care                         |
| 24       | Slice 2/3 — CODE ID <sub>0</sub>   |
| 25       | Slice 2/3 — CODE ID <sub>1</sub>   |
| 26       | Slice 2/3 — CODE ID <sub>2</sub>   |
| 27       | Slice 2/3 — DIAG MODE <sub>0</sub> |
| 28       | Slice 2/3 — DIAG MODE <sub>1</sub> |
| 29       | Slice 2/3 — CORRECT                |
| 30       | Slice 2/3 — PASSTHRU               |
| 31       | Don't Care                         |

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Table 9. Diagnostic Latch Loading — 32-Bit Format

| Generated<br>Check Bits | Parity     | Participating Data Bits |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |
|-------------------------|------------|-------------------------|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|
|                         |            | 0                       | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| C <sub>0</sub>          | Even (XOR) | X                       |   |   |   | X |   | X | X | X | X |    | X  |    |    | X  |    |
| C <sub>1</sub>          | Even (XOR) | X                       | X | X |   | X |   | X |   | X |   | X  |    | X  |    |    |    |
| C <sub>2</sub>          | Odd (XNOR) | X                       |   |   | X | X |   |   | X |   | X | X  |    |    | X  |    | X  |
| C <sub>3</sub>          | Odd (XNOR) | X                       | X |   |   |   | X | X | X |   |   |    | X  | X  | X  |    |    |
| C <sub>4</sub>          | Even (XOR) |                         |   | X | X | X | X | X | X |   |   |    |    |    |    | X  | X  |
| C <sub>5</sub>          | Even (XOR) |                         |   |   |   |   |   |   |   | X | X | X  | X  | X  | X  | X  | X  |
| C <sub>6</sub>          | Even (XOR) | X                       | X | X | X | X | X | X | X |   |   |    |    |    |    |    |    |

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| Generated Check Bits | Parity     | Participating Data Bits |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|----------------------|------------|-------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|                      |            | 16                      | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 |
| C <sub>0</sub>       | Even (XOR) |                         | X  | X  | X  |    | X  |    |    |    |    | X  |    | X  | X  |    | X  |
| C <sub>1</sub>       | Even (XOR) | X                       | X  | X  |    | X  |    | X  |    | X  |    | X  |    | X  |    |    |    |
| C <sub>2</sub>       | Odd (XNOR) | X                       |    |    | X  | X  |    |    | X  |    | X  | X  |    |    | X  |    | X  |
| C <sub>3</sub>       | Odd (XNOR) | X                       | X  |    |    |    | X  | X  | X  |    |    |    | X  | X  | X  |    |    |
| C <sub>4</sub>       | Even (XOR) |                         |    | X  | X  | X  | X  | X  | X  |    |    |    |    |    |    | X  | X  |
| C <sub>5</sub>       | Even (XOR) |                         |    |    |    |    |    |    |    | X  | X  | X  | X  | X  | X  | X  | X  |
| C <sub>6</sub>       | Even (XOR) |                         |    |    |    |    |    |    |    | X  | X  | X  | X  | X  | X  | X  | X  |

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Table 10. 32-Bit Modified Hamming Code — Check Bit Encode Chart

## 64-BIT DATA WORD CONFIGURATION

The IDT39C60 EDC units connected with the MSI gates, as shown in Figure 7, provide all the logic needed for single bit error detection and double bit error detection of a 64-bit data field. The Identification code 64/72 is used, indicating 8 check bits are required. Check bits and Syndrome bits are generated external to the IDT39C60 EDC using Exclusive-OR gates. For error correction, the syndrome bits must be fed-back to the CBo-6 inputs. Thus, external tri-state buffers are used to select between the check bits read in from memory and the syndrome bits being fed back.

The ERROR signal is low for one or more errors detected. From any of the 4 devices, MULTERROR is low for some double bit errors and for all three bit errors. Both are high otherwise. The DOUBLE ERROR signal is high only when a double bit error is detected.

Figure 6 indicates the 72-bit data format of 8 bytes of data and 8 check bits. Check bits are input to the various units through a tri-state buffer such as the IDT74FCT244. Correction of single bit errors of the 64-bit configuration requires a feedback of syndrome bits as generated external to the IDT39C60 EDC. The MUX shown on the functional block diagram is used to select the CBo-6 pins as the syndrome bits rather than internally generated syndrome bits.

Table 3 describes the operating modes available for the 64/72 configuration.

Syndrome bits are generated by an Exclusive-OR of the generated check bits with the read check bits. For example,  $S_n$  is the XOR of check bits  $C_n$  from those read with those generated. Table 11 indicates the decoding of the 8 syndrome bits to determine the bit-in-error for a single bit error or whether

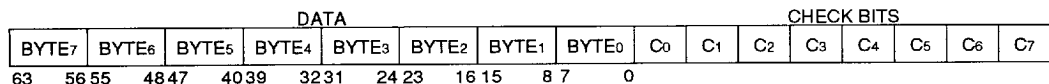
a double or triple bit error was detected. The all zero case indicates no errors detected.

In the Correct Mode, the syndrome bits are used to complement (correct) single bit errors in the data bits. For double or multiple error detection, the data available as input to the Data Out Latch is not defined.

Performance data is provided in Table 12 for a single IDT39C60 EDC with the four units of Figure 7. Delay through the Exclusive-OR gates and the 3-state buffer must be included.

Table 13 indicates the Data Bits participating in the check bit generation. For example, check bit  $C_0$  is the Exclusive-OR function of the 32 data input bits marked with an X. Check bits are generated and output in the Generate and Initialization mode. In the PASSTHRU mode, the contents of the check bit latch are passed through the external Exclusive-OR gates and appear inverted at the outputs  $C_0$  to  $C_7$ .

Table 14 defines the bit definition for the Diagnostic Latch. As defined in Table 3, several modes will use the Diagnostic Check Bits to determine syndrome bits or to pass as check bits to the SC0-6 outputs. The Internal Mode substitutes the indicated bit position for the external control signals.



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Uses Modified Hamming Code 64/72  
32 Data Bits with 8 Check Bits

Figure 6. 64-Bit Data Format

|     |               |    |    |    | Hex | 0  | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | A  | B | C | D  | E | F  |   |   |   |   |
|-----|---------------|----|----|----|-----|----|----|----|----|----|----|----|----|----|----|----|---|---|----|---|----|---|---|---|---|
|     | Syndrome Bits |    |    |    | S7  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 1  | 1 | 1 | 1  | 1 | 1  | 1 |   |   |   |
|     |               |    |    |    | S6  | 0  | 0  | 0  | 0  | 1  | 1  | 1  | 1  | 0  | 0  | 0  | 0 | 1 | 1  | 1 | 1  | 1 | 1 | 1 |   |
|     |               |    |    |    | S5  | 0  | 0  | 1  | 1  | 0  | 0  | 1  | 1  | 0  | 0  | 1  | 1 | 1 | 1  | 0 | 0  | 1 | 1 | 1 | 1 |
|     |               |    |    |    | S4  | 0  | 1  | 0  | 1  | 0  | 1  | 0  | 1  | 0  | 0  | 1  | 1 | 0 | 1  | 0 | 1  | 0 | 1 | 0 | 1 |
| Hex | S3            | S2 | S1 | S0 |     |    |    |    |    |    |    |    |    |    |    |    |   |   |    |   |    |   |   |   |   |
| 0   | 0             | 0  | 0  | 0  | *   | C4 | C5 | T  | C6 | T  | T  | 62 | C7 | T  | T  | 46 | T | M | M  | T | T  |   |   |   |   |
| 1   | 0             | 0  | 0  | 1  | C0  | T  | T  | 14 | T  | M  | M  | T  | T  | M  | M  | T  | M | T | T  | T | 30 |   |   |   |   |
| 2   | 0             | 0  | 1  | 0  | C1  | T  | T  | M  | T  | 34 | 56 | T  | T  | 50 | 40 | T  | M | T | T  | T | M  |   |   |   |   |
| 3   | 0             | 0  | 1  | 1  | T   | 18 | 8  | T  | M  | T  | T  | M  | M  | T  | T  | M  | T | 2 | 24 | T | T  |   |   |   |   |
| 4   | 0             | 1  | 0  | 0  | C2  | T  | T  | 15 | T  | 35 | 57 | T  | T  | 51 | 41 | T  | M | T | T  | T | 31 |   |   |   |   |
| 5   | 0             | 1  | 0  | 1  | T   | 19 | 9  | T  | M  | T  | T  | 63 | M  | T  | T  | 47 | T | 3 | 25 | T | T  |   |   |   |   |
| 6   | 0             | 1  | 1  | 0  | T   | 20 | 10 | T  | M  | T  | T  | M  | M  | T  | T  | M  | T | 4 | 26 | T | T  |   |   |   |   |
| 7   | 0             | 1  | 1  | 1  | M   | T  | T  | M  | T  | 36 | 58 | T  | T  | 52 | 42 | T  | M | T | T  | T | M  |   |   |   |   |
| 8   | 1             | 0  | 0  | 0  | C3  | T  | T  | M  | T  | 37 | 59 | T  | T  | 53 | 43 | T  | M | T | T  | T | M  |   |   |   |   |
| 9   | 1             | 0  | 0  | 1  | T   | 21 | 11 | T  | M  | T  | T  | M  | M  | T  | T  | M  | T | 5 | 27 | T | T  |   |   |   |   |
| A   | 1             | 0  | 1  | 0  | T   | 22 | 12 | T  | 33 | T  | T  | M  | 49 | T  | T  | M  | T | 6 | 28 | T | T  |   |   |   |   |
| B   | 1             | 0  | 1  | 1  | 17  | T  | T  | M  | T  | 38 | 60 | T  | T  | 54 | 44 | T  | 1 | T | T  | T | M  |   |   |   |   |
| C   | 1             | 1  | 0  | 0  | T   | 23 | 13 | T  | M  | T  | T  | M  | M  | T  | T  | M  | T | 7 | 29 | T | T  |   |   |   |   |
| D   | 1             | 1  | 0  | 1  | M   | T  | T  | M  | T  | 39 | 61 | T  | T  | 55 | 45 | T  | M | T | T  | T | M  |   |   |   |   |
| E   | 1             | 1  | 1  | 0  | 16  | T  | T  | M  | T  | M  | M  | T  | T  | M  | M  | T  | 0 | T | T  | T | M  |   |   |   |   |
| F   | 1             | 1  | 1  | 1  | T   | M  | M  | T  | 32 | T  | T  | M  | 48 | T  | T  | M  | T | M | M  | T | T  |   |   |   |   |

**NOTES:**

\* = No errors detected

Number = The number of the single bit-in-error

T = Two errors detected

M = Three or more errors detected

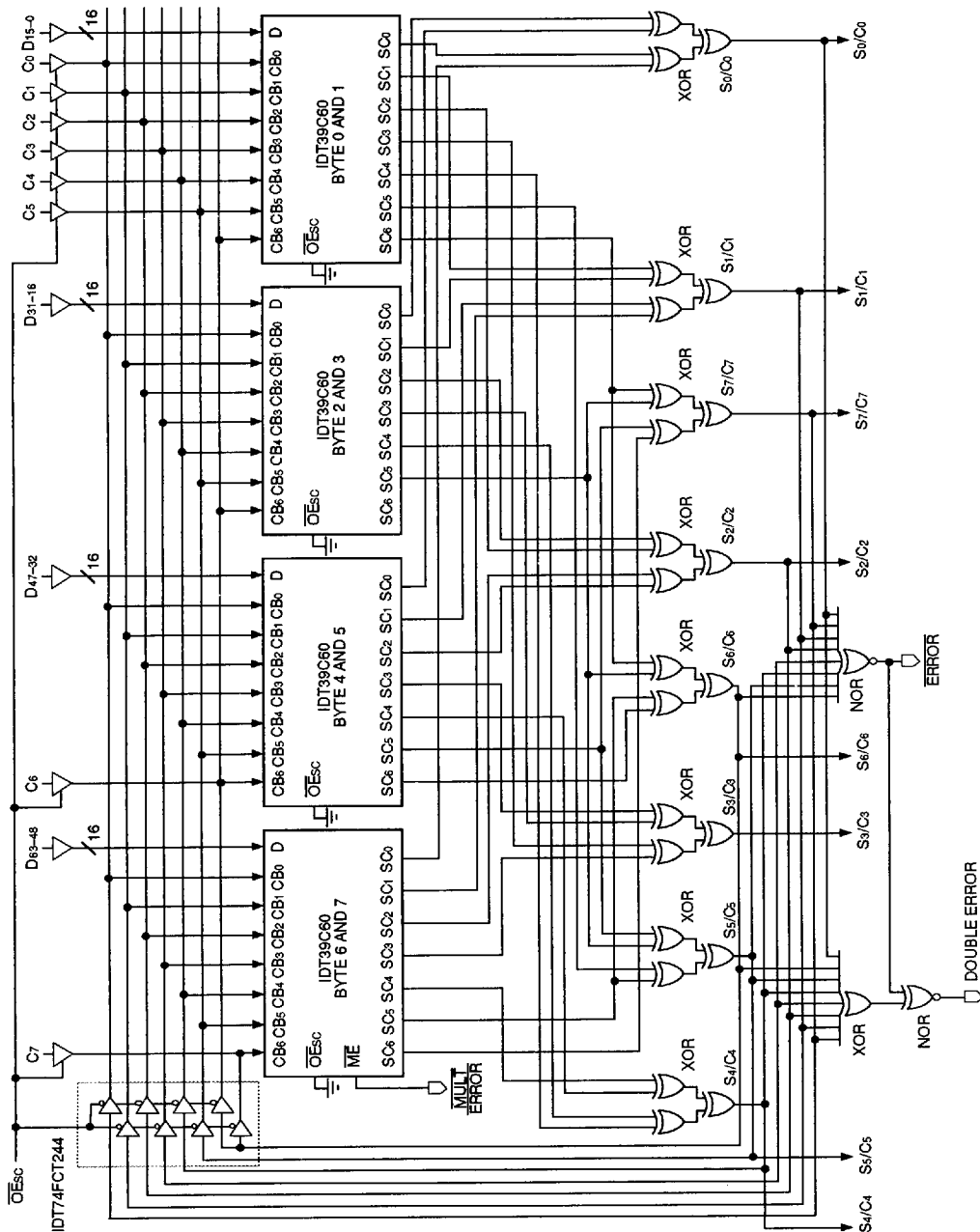
2595 tbl 13

Table 11. Syndrome Decode to Bit-In-Error (64-Bit Configuration)

| 64-Bit Propagation Delay |                               | Component Delay From IDT39C60                                                 |
|--------------------------|-------------------------------|-------------------------------------------------------------------------------|
| From                     | To                            |                                                                               |
| DATA                     | Check Bits Out                | (DATA to SC) + (XOR Delay)                                                    |
| DATA                     | Corrected DATA <sub>OUT</sub> | (DATA to SC) + (XOR Delay) + (Buffer Delay) + (CB to DATA, CODE ID 1xx)       |
| DATA                     | Syndromes                     | (DATA to SC) + (XOR Delay)                                                    |
| DATA                     | ERROR for 64 Bits             | (DATA to SC) + (XOR Delay) + (NOR Delay)                                      |
| DATA                     | MULT ERROR for 64 Bits        | (DATA to SC) + (XOR Delay) + (Buffer Delay) + (CB to MULT ERROR, CODE ID 1xx) |
| DATA                     | DOUBLE ERROR for 64 Bits      | (DATA to SC) + (XOR Delay) + (XOR/NOR Delay)                                  |

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Table 12. Key AC Calculations for the 64-Bit Configuration



NOTES:

1. In PASSTHRU mode the contents of the Check Latch appears on the XOR outputs inverted.
2. In Diagnostic Generate mode the contents of the Diagnostic Latch appear on the XOR outputs inverted.

Figure 7. 64-Bit Configuration

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| Generated<br>Check Bits | Parity     | Participating Data Bits <sup>(1)</sup> |   |   |   |   |   |   |   |   |   |    |    |    |    |    |    |
|-------------------------|------------|----------------------------------------|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|
|                         |            | 0                                      | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 |
| C <sub>0</sub>          | Even (XOR) |                                        | X | X | X |   | X |   |   | X | X |    | X  |    |    | X  |    |
| C <sub>1</sub>          | Even (XOR) | X                                      | X | X |   | X |   | X |   | X |   | X  |    | X  |    |    |    |
| C <sub>2</sub>          | Odd (XNOR) | X                                      |   |   | X | X |   |   | X |   | X | X  |    |    | X  |    | X  |
| C <sub>3</sub>          | Odd (XNOR) | X                                      | X |   |   |   | X | X | X |   |   |    | X  | X  | X  |    |    |
| C <sub>4</sub>          | Even (XOR) |                                        |   | X | X | X | X | X | X |   |   |    |    |    |    | X  | X  |
| C <sub>5</sub>          | Even (XOR) |                                        |   |   |   |   |   |   |   | X | X | X  | X  | X  | X  | X  | X  |
| C <sub>6</sub>          | Even (XOR) | X                                      | X | X | X | X | X | X | X |   |   |    |    |    |    |    |    |
| C <sub>7</sub>          | Even (XOR) | X                                      | X | X | X | X | X | X | X |   |   |    |    |    |    |    |    |

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| Generated Check Bits | Parity     | Participating Data Bits <sup>(1)</sup> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|----------------------|------------|----------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|                      |            | 16                                     | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 |
| C0                   | Even (XOR) |                                        | X  | X  | X  |    | X  |    |    | X  | X  |    | X  |    |    | X  |    |
| C1                   | Even (XOR) | X                                      | X  | X  |    | X  |    | X  |    | X  |    | X  |    | X  |    |    |    |
| C2                   | Odd (XNOR) | X                                      |    |    | X  | X  |    |    | X  |    | X  | X  |    |    | X  |    | X  |
| C3                   | Odd (XNOR) | X                                      | X  |    |    |    | X  | X  | X  |    |    |    | X  | X  | X  |    |    |
| C4                   | Even (XOR) |                                        |    | X  | X  | X  | X  | X  | X  |    |    |    |    |    |    | X  | X  |
| C5                   | Even (XOR) |                                        |    |    |    |    |    |    |    | X  | X  | X  | X  | X  | X  | X  | X  |
| C6                   | Even (XOR) |                                        |    |    |    |    |    |    |    | X  | X  | X  | X  | X  | X  | X  | X  |
| C7                   | Even (XOR) |                                        |    |    |    |    |    |    |    | X  | X  | X  | X  | X  | X  | X  | X  |

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| Generated Check Bits | Parity     | Participating Data Bits <sup>(1)</sup> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|----------------------|------------|----------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|                      |            | 32                                     | 33 | 34 | 35 | 36 | 37 | 38 | 39 | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 |
| C0                   | Even (XOR) | X                                      |    |    |    | X  |    | X  | X  |    |    | X  |    | X  | X  |    | X  |
| C1                   | Even (XOR) | X                                      | X  | X  |    | X  |    | X  |    | X  |    | X  |    | X  |    |    |    |
| C2                   | Odd (XNOR) | X                                      |    |    | X  | X  |    |    | X  |    | X  | X  |    |    | X  |    | X  |
| C3                   | Odd (XNOR) | X                                      | X  |    |    |    | X  | X  | X  |    |    |    | X  | X  | X  |    |    |
| C4                   | Even (XOR) |                                        |    | X  | X  | X  | X  | X  | X  |    |    |    |    |    |    | X  | X  |
| C5                   | Even (XOR) |                                        |    |    |    |    |    |    |    | X  | X  | X  | X  | X  | X  | X  | X  |
| C6                   | Even (XOR) | X                                      | X  | X  | X  | X  | X  | X  | X  |    |    |    |    |    |    |    |    |
| C7                   | Even (XOR) |                                        |    |    |    |    |    |    |    | X  | X  | X  | X  | X  | X  | X  | X  |

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| Generated<br>Check Bits | Parity     | Participating Data Bits <sup>(1)</sup> |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|-------------------------|------------|----------------------------------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|                         |            | 48                                     | 49 | 50 | 51 | 52 | 53 | 54 | 55 | 56 | 57 | 58 | 59 | 60 | 61 | 62 | 63 |
| C0                      | Even (XOR) | X                                      |    |    |    | X  |    | X  | X  |    |    | X  |    | X  | X  |    | X  |
| C1                      | Even (XOR) | X                                      | X  | X  |    | X  |    | X  |    | X  |    | X  |    | X  |    |    |    |
| C2                      | Odd (XNOR) | X                                      |    |    | X  | X  |    |    | X  |    | X  | X  |    |    | X  |    | X  |
| C3                      | Odd (XNOR) | X                                      | X  |    |    |    | X  | X  | X  |    |    |    | X  | X  | X  |    |    |
| C4                      | Even (XOR) |                                        |    | X  | X  | X  | X  | X  | X  |    |    |    |    |    |    | X  | X  |
| C5                      | Even (XOR) |                                        |    |    |    |    |    |    |    | X  | X  | X  | X  | X  | X  | X  | X  |
| C6                      | Even (XOR) |                                        |    |    |    |    |    |    |    | X  | X  | X  | X  | X  | X  | X  | X  |
| C7                      | Even (XOR) | X                                      | X  | X  | X  | X  | X  | X  | X  |    |    |    |    |    |    |    |    |

**NOTE:**

1. The check bit is generated as either an XOR or XNOR of the 32 data bits noted by an "X" in the table.

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Table 13. 64-Bit Modified Hamming Code — Check Bit Encode Chart

■ 4825771 0016244 405 ■



| Data Bit | Internal Function      | Data Bit | Internal Function      |
|----------|------------------------|----------|------------------------|
| 0        | Diagnostic Check Bit0  | 31       | Don't Care             |
| 1        | Diagnostic Check Bit1  | 32-37    | Don't Care             |
| 2        | Diagnostic Check Bit2  | 38       | Diagnostic Check Bits  |
| 3        | Diagnostic Check Bit3  | 39       | Don't Care             |
| 4        | Diagnostic Check Bit4  | 40       | Slice 4/5 — CODE ID0   |
| 5        | Diagnostic Check Bits  | 41       | Slice 4/5 — CODE ID1   |
| 6, 7     | Don't Care             | 42       | Slice 4/5 — CODE ID2   |
| 8        | Slice 0/1 — CODE ID0   | 43       | Slice 4/5 — DIAG MODE0 |
| 9        | Slice 0/1 — CODE ID1   | 44       | Slice 4/5 — DIAG MODE1 |
| 10       | Slice 0/1 — CODE ID2   | 45       | Slice 4/5 — CORRECT    |
| 11       | Slice 0/1 — DIAG MODE0 | 46       | Slice 4/5 — PASSTHRU   |
| 12       | Slice 0/1 — DIAG MODE1 | 47       | Don't Care             |
| 13       | Slice 0/1 — CORRECT    | 48-54    | Don't Care             |
| 14       | Slice 0/1 — PASSTHRU   | 55       | Diagnostic Check Bit7  |
| 15       | Don't Care             | 56       | Slice 6/7 — CODE ID0   |
| 16-23    | Don't Care             | 57       | Slice 6/7 — CODE ID1   |
| 24       | Slice 2/3 — CODE ID0   | 58       | Slice 6/7 — CODE ID2   |
| 25       | Slice 2/3 — CODE ID1   | 59       | Slice 6/7 — DIAG MODE0 |
| 26       | Slice 2/3 — CODE ID2   | 60       | Slice 6/7 — DIAG MODE1 |
| 27       | Slice 2/3 — DIAG MODE0 | 61       | Slice 6/7 — CORRECT    |
| 28       | Slice 2/3 — DIAG MODE1 | 62       | Slice 6/7 — PASSTHRU   |
| 29       | Slice 2/3 — CORRECT    | 63       | Don't Care             |
| 30       | Slice 2/3 — PASSTHRU   |          |                        |

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Table 14. Diagnostic Latch Loading — 64-Bit Format

Some multiple errors will cause a data bit to be inverted. For example, in the 16-bit mode where bits 8 and 13 are in error, the syndrome 111100 (S0, S1, S2, S3, S4, S5) is produced. The bit-in-error decoder receives the syndrome 11100 (S0, S1, S2, S3, S4) which it decodes as a single error in data bit 0 and inverts that bit. Figure 8 indicates a method for inhibiting correction when a multiple error occurs.

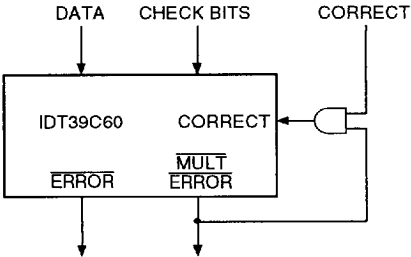


Figure 8. Inhibition of Data Modification

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## FUNCTIONAL EQUATIONS

The following equations and tables describes how the output values of the IDT39C60 EDC are determined as a function of the value of the inputs and the internal states. Carefully read the following definitions of symbols before examining the tables.

### DEFINITIONS

$D_i \leftarrow \text{DATA}_i$  if LEIN is HIGH or the output of bit  $i$  of the Data Input Latch if LEIN is LOW

$C_i \leftarrow \text{CBI}_i$  if LEIN is HIGH or the output of bit  $i$  of the Check Bit Latch if LEIN is LOW

$DL_i \leftarrow \text{Output of bit } i \text{ of the Diagnostic Latch}$

$SI \leftarrow \text{Internally generated syndromes (same as outputs of } SC_i \text{ if outputs enabled)}$

$PA \leftarrow D_0 \oplus D_1 \oplus D_2 \oplus D_4 \oplus D_6 \oplus D_8 \oplus D_{10} \oplus D_{12}$

$PB \leftarrow D_0 \oplus D_1 \oplus D_2 \oplus D_3 \oplus D_4 \oplus D_5 \oplus D_6 \oplus D_7$

$PC \leftarrow D_8 \oplus D_9 \oplus D_{10} \oplus D_{11} \oplus D_{12} \oplus D_{13} \oplus D_{14} \oplus D_{15}$

$PD \leftarrow D_0 \oplus D_3 \oplus D_4 \oplus D_7 \oplus D_9 \oplus D_{10} \oplus D_{13} \oplus D_{15}$

$PE \leftarrow D_0 \oplus D_1 \oplus D_5 \oplus D_6 \oplus D_7 \oplus D_{11} \oplus D_{12} \oplus D_{13}$

$PF \leftarrow D_2 \oplus D_3 \oplus D_4 \oplus D_5 \oplus D_6 \oplus D_{14} \oplus D_{15} \oplus D_7$

$PG_1 \leftarrow D_0 \oplus D_4 \oplus D_6 \oplus D_7$

$PG_2 \leftarrow D_1 \oplus D_2 \oplus D_3 \oplus D_5$

$PG_3 \leftarrow D_8 \oplus D_9 \oplus D_{11} \oplus D_{14}$

$PG_4 \leftarrow D_{10} \oplus D_{12} \oplus D_{13} \oplus D_{15}$

### Error Signals

$\text{ERROR} \leftarrow (S_6 \cdot (ID_1 + ID_2)) \cdot S_5 \cdot S_4 \cdot S_3 \cdot S_2 \cdot S_1 \cdot S_0 + \text{GENERATE} + \text{INITIALIZE} + \text{PASSTHRU}$

**MULT ERROR:**

(16 and 32-Bit Modes)  $\leftarrow ((S_6 \cdot ID_1) \oplus S_5 \oplus S_4 \oplus S_3 \oplus S_2 \oplus S_1 \oplus S_0) (\text{ERROR}) + \text{TOME} + \text{GENERATE} + \text{PASSTHRU} + \text{INITIALIZE}$

**MULT ERROR:** (64-Bit Modes)  $\leftarrow \text{TOME} + \text{GENERATE} + \text{PASSTHRU} + \text{INITIALIZE}$

|     |                |                | Hex            | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|-----|----------------|----------------|----------------|---|---|---|---|---|---|---|---|
|     |                |                | S <sub>6</sub> | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
|     |                |                | S <sub>5</sub> | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
|     |                |                | S <sub>4</sub> | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
|     |                |                | S <sub>3</sub> | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
|     |                |                | S <sub>2</sub> | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
|     |                |                | S <sub>1</sub> | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
|     |                |                | S <sub>0</sub> | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| Hex | S <sub>2</sub> | S <sub>1</sub> | S <sub>0</sub> | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 0 8 | 0              | 0              | 0              |   |   |   |   | 1 | 1 | 1 | 1 |
| 1 9 | 0              | 0              | 1              |   | 1 |   | 1 | 1 | 1 | 1 | 1 |
| 2 A | 0              | 1              | 0              |   |   | 1 |   | 1 | 1 |   | 1 |
| 3 B | 0              | 1              | 1              | 1 |   |   |   | 1 | 1 |   | 1 |
| 4 C | 1              | 0              | 0              |   | 1 |   |   | 1 | 1 |   | 1 |
| 5 D | 1              | 0              | 1              | 1 | 1 |   |   | 1 | 1 |   | 1 |
| 6 E | 1              | 1              | 0              | 1 |   | 1 | 1 | 1 | 1 | 1 |   |
| 7 F | 1              | 1              | 1              | 1 |   | 1 | 1 | 1 | 1 | 1 | 1 |

### NOTES:

- $S_6, S_5, \dots, S_0$  are internal syndromes except in Modes 010, 100, 101, 110, 111 (CODE ID<sub>2</sub>, ID<sub>1</sub>, ID<sub>0</sub>). In these modes, the syndromes are input over the check bit lines.  $S_6 \leftarrow C_6, S_5 \leftarrow C_5, \dots, S_1 \leftarrow C_1, S_0 \leftarrow C_0$ .
- The  $S_6$  internal syndrome is always forced to 0 in CODE ID 000.

Table 15. TOME (Three or More Errors)

| Generate Mode (Check Bits) | CODE ID <sub>0-2</sub>            |                                   |                                                     |                                   |                                   |                                   |                                   |
|----------------------------|-----------------------------------|-----------------------------------|-----------------------------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|
|                            | 000                               | 010                               | 011                                                 | 100                               | 101                               | 110                               | 111                               |
| SC <sub>0</sub> ←          | PG <sub>2</sub> ⊕ PG <sub>3</sub> | PG <sub>1</sub> ⊕ PG <sub>3</sub> | PG <sub>2</sub> ⊕ PG <sub>4</sub> ⊕ CB <sub>0</sub> | PG <sub>2</sub> ⊕ PG <sub>3</sub> | PG <sub>2</sub> ⊕ PG <sub>3</sub> | PG <sub>1</sub> ⊕ PG <sub>4</sub> | PG <sub>1</sub> ⊕ PG <sub>4</sub> |
| SC <sub>1</sub> ←          | PA                                | PA                                | PA ⊕ CB <sub>1</sub>                                | PA                                | PA                                | PA                                | PA                                |
| SC <sub>2</sub> ←          | PD                                | PD                                | PD ⊕ CB <sub>2</sub>                                | PD                                | PD                                | PD                                | PD                                |
| SC <sub>3</sub> ←          | PE                                | PE                                | PE ⊕ CB <sub>3</sub>                                | PE                                | PE                                | PE                                | PE                                |
| SC <sub>4</sub> ←          | PF                                | PF                                | PF ⊕ CB <sub>4</sub>                                | PF                                | PF                                | PF                                | PF                                |
| SC <sub>5</sub> ←          | PC                                | PC                                | PC ⊕ CB <sub>5</sub>                                | PC                                | PC                                | PC                                | PC                                |
| SC <sub>6</sub> ←          | 1                                 | PB                                | PC ⊕ CB <sub>6</sub>                                | PB                                | PB                                | PB                                | PB                                |

Table 16. Generate Mode (Check Bits)

| Detect and Correct Modes (Syndromes) | CODE ID <sub>0-2</sub>                             |                                                    |                                                     |                                                    |                                   |                                   |                                   |
|--------------------------------------|----------------------------------------------------|----------------------------------------------------|-----------------------------------------------------|----------------------------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|
|                                      | 000                                                | 010                                                | 011 <sup>(1)</sup>                                  | 100                                                | 101                               | 110                               | 111                               |
| SC <sub>0</sub> ←                    | PG <sub>2</sub> ⊕ PG <sub>3</sub> ⊕ C <sub>0</sub> | PG <sub>1</sub> ⊕ PG <sub>3</sub> ⊕ C <sub>0</sub> | PG <sub>2</sub> ⊕ PG <sub>4</sub> ⊕ CB <sub>0</sub> | PG <sub>2</sub> ⊕ PG <sub>3</sub> ⊕ C <sub>0</sub> | PG <sub>2</sub> ⊕ PG <sub>3</sub> | PG <sub>1</sub> ⊕ PG <sub>4</sub> | PG <sub>1</sub> ⊕ PG <sub>4</sub> |
| SC <sub>1</sub> ←                    | PA ⊕ C <sub>1</sub>                                | PA ⊕ C <sub>1</sub>                                | PA ⊕ CB <sub>1</sub>                                | PA ⊕ C <sub>1</sub>                                | PA                                | PA                                | PA                                |
| SC <sub>2</sub> ←                    | PD ⊕ C <sub>2</sub>                                | PD ⊕ C <sub>2</sub>                                | PD ⊕ CB <sub>2</sub>                                | PD ⊕ C <sub>2</sub>                                | PD                                | PD                                | PD                                |
| SC <sub>3</sub> ←                    | PE ⊕ C <sub>3</sub>                                | PE ⊕ C <sub>3</sub>                                | PE ⊕ CB <sub>3</sub>                                | PE ⊕ C <sub>3</sub>                                | PE                                | PE                                | PE                                |
| SC <sub>4</sub> ←                    | PF ⊕ C <sub>4</sub>                                | PF ⊕ C <sub>4</sub>                                | PF ⊕ CB <sub>4</sub>                                | PF ⊕ C <sub>4</sub>                                | PF                                | PF                                | PF                                |
| SC <sub>5</sub> ←                    | PC ⊕ C <sub>5</sub>                                | PC ⊕ C <sub>5</sub>                                | PC ⊕ CB <sub>5</sub>                                | PC ⊕ C <sub>5</sub>                                | PC                                | PC                                | PC                                |
| SC <sub>6</sub> ←                    | 1                                                  | PB ⊕ C <sub>6</sub>                                | PC ⊕ CB <sub>6</sub>                                | PB                                                 | PB                                | PB ⊕ C <sub>6</sub>               | PB ⊕ C <sub>6</sub>               |

**NOTE:**

1. In CODE ID<sub>2=0</sub> 011 the Check Bit Latch is forced transparent. The Data Latch operates normally.

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**Table 17. Detect and Correct Modes (Syndromes)**

| Diagnostic Detect and Correct Mode | CODE ID <sub>0-2</sub>                              |                                                     |                                                     |                                                     |                                   |                                   |                                   |
|------------------------------------|-----------------------------------------------------|-----------------------------------------------------|-----------------------------------------------------|-----------------------------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|
|                                    | 000                                                 | 010                                                 | 011 <sup>(1)</sup>                                  | 100                                                 | 101                               | 110                               | 111                               |
| SC <sub>0</sub> ←                  | PG <sub>2</sub> ⊕ PG <sub>3</sub> ⊕ DL <sub>0</sub> | PG <sub>1</sub> ⊕ PG <sub>3</sub> ⊕ DL <sub>0</sub> | PG <sub>2</sub> ⊕ PG <sub>4</sub> ⊕ CB <sub>0</sub> | PG <sub>2</sub> ⊕ PG <sub>3</sub> ⊕ DL <sub>0</sub> | PG <sub>2</sub> ⊕ PG <sub>3</sub> | PG <sub>1</sub> ⊕ PG <sub>4</sub> | PG <sub>1</sub> ⊕ PG <sub>4</sub> |
| SC <sub>1</sub> ←                  | PA ⊕ DL <sub>1</sub>                                | PA ⊕ DL <sub>1</sub>                                | PA ⊕ CB <sub>1</sub>                                | PA ⊕ DL <sub>1</sub>                                | PA                                | PA                                | PA                                |
| SC <sub>2</sub> ←                  | PD ⊕ DL <sub>2</sub>                                | PD ⊕ DL <sub>2</sub>                                | PD ⊕ CB <sub>2</sub>                                | PD ⊕ DL <sub>2</sub>                                | PD                                | PD                                | PD                                |
| SC <sub>3</sub> ←                  | PE ⊕ DL <sub>3</sub>                                | PE ⊕ DL <sub>3</sub>                                | PE ⊕ CB <sub>3</sub>                                | PE ⊕ DL <sub>3</sub>                                | PE                                | PE                                | PE                                |
| SC <sub>4</sub> ←                  | PF ⊕ DL <sub>4</sub>                                | PF ⊕ DL <sub>4</sub>                                | PF ⊕ CB <sub>4</sub>                                | PF ⊕ DL <sub>4</sub>                                | PF                                | PF                                | PF                                |
| SC <sub>5</sub> ←                  | PDL ⊕ DL <sub>5</sub>                               | PC ⊕ DL <sub>5</sub>                                | PC ⊕ CB <sub>5</sub>                                | PC ⊕ DL <sub>5</sub>                                | PC                                | PC                                | PC                                |
| SC <sub>6</sub> ←                  | 1                                                   | PB ⊕ DL <sub>6</sub>                                | PC ⊕ CB <sub>6</sub>                                | PB                                                  | PB                                | PB ⊕ DL <sub>6</sub>              | PB ⊕ DL <sub>7</sub>              |

**NOTE:**

1. In CODE ID<sub>2=0</sub> 011 the Check Bit Latch is forced transparent. The Data Latch operates normally.

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**Table 18. Diagnostic Detect and Correct Mode**

| Diagnostic Generate Mode | CODE ID <sub>0-2</sub> |                 |                    |                 |     |                 |                 |
|--------------------------|------------------------|-----------------|--------------------|-----------------|-----|-----------------|-----------------|
|                          | 000                    | 010             | 011 <sup>(1)</sup> | 100             | 101 | 110             | 111             |
| SC <sub>0</sub> ←        | DL <sub>0</sub>        | DL <sub>0</sub> | CB <sub>0</sub>    | DL <sub>0</sub> | 1   | 1               | 1               |
| SC <sub>1</sub> ←        | DL <sub>1</sub>        | DL <sub>1</sub> | CB <sub>1</sub>    | DL <sub>1</sub> | 1   | 1               | 1               |
| SC <sub>2</sub> ←        | DL <sub>2</sub>        | DL <sub>2</sub> | CB <sub>2</sub>    | DL <sub>2</sub> | 1   | 1               | 1               |
| SC <sub>3</sub> ←        | DL <sub>3</sub>        | DL <sub>3</sub> | CB <sub>3</sub>    | DL <sub>3</sub> | 1   | 1               | 1               |
| SC <sub>4</sub> ←        | DL <sub>4</sub>        | DL <sub>4</sub> | CB <sub>4</sub>    | DL <sub>4</sub> | 1   | 1               | 1               |
| SC <sub>5</sub> ←        | DL <sub>5</sub>        | DL <sub>5</sub> | CB <sub>5</sub>    | DL <sub>5</sub> | 1   | 1               | 1               |
| SC <sub>6</sub> ←        | 1                      | DL <sub>6</sub> | CB <sub>6</sub>    | 1               | 1   | DL <sub>6</sub> | DL <sub>7</sub> |

**NOTE:**

1. In CODE ID<sub>2=0</sub> 011 the Check Bit Latch is forced transparent. The Data Latch operates normally.

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**Table 19. Diagnostic Generate Mode**

| PASSTHRU Mode     | CODE ID <sub>0-2</sub> |                |                    |                |     |                |                |
|-------------------|------------------------|----------------|--------------------|----------------|-----|----------------|----------------|
|                   | 000                    | 010            | 011 <sup>(1)</sup> | 100            | 101 | 110            | 111            |
| SC <sub>0</sub> ← | C <sub>0</sub>         | C <sub>0</sub> | CB <sub>0</sub>    | C <sub>0</sub> | 1   | 1              | 1              |
| SC <sub>1</sub> ← | C <sub>1</sub>         | C <sub>1</sub> | CB <sub>1</sub>    | C <sub>1</sub> | 1   | 1              | 1              |
| SC <sub>2</sub> ← | C <sub>2</sub>         | C <sub>2</sub> | CB <sub>2</sub>    | C <sub>2</sub> | 1   | 1              | 1              |
| SC <sub>3</sub> ← | C <sub>3</sub>         | C <sub>3</sub> | CB <sub>3</sub>    | C <sub>3</sub> | 1   | 1              | 1              |
| SC <sub>4</sub> ← | C <sub>4</sub>         | C <sub>4</sub> | CB <sub>4</sub>    | C <sub>4</sub> | 1   | 1              | 1              |
| SC <sub>5</sub> ← | C <sub>5</sub>         | C <sub>5</sub> | CB <sub>5</sub>    | C <sub>5</sub> | 1   | 1              | 1              |
| SC <sub>6</sub> ← | 1                      | C <sub>6</sub> | CB <sub>6</sub>    | 1              | 1   | C <sub>6</sub> | C <sub>6</sub> |

**NOTE:**

1. In CODE ID<sub>2=0</sub> 011 the Check Bit Latch is forced transparent. The Data Latch operates normally.

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**Table 20. PASSTHRU Mode**

| S <sub>2</sub> | S <sub>1</sub> | S <sub>5</sub> S <sub>4</sub> S <sub>3</sub> |   |   |   |    |    |    |   |
|----------------|----------------|----------------------------------------------|---|---|---|----|----|----|---|
|                |                | 0                                            | 0 | 0 | 0 | 1  | 1  | 1  | 1 |
| 0              | 0              | —                                            | — | — | 5 | —  | 11 | 14 | — |
| 0              | 1              | —                                            | 1 | 2 | 6 | 8  | 12 | —  | — |
| 1              | 0              | —                                            | — | 3 | 7 | 9  | 13 | 15 | — |
| 1              | 1              | —                                            | 0 | 4 | — | 10 | —  | —  | — |

NOTE:

1. Unlisted S combinations are no correction.

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Table 21. CODE ID<sub>2-0</sub> = 000

| C <sub>2</sub> | C <sub>1</sub> | C <sub>6</sub> C <sub>5</sub> C <sub>4</sub> C <sub>3</sub> |    |    |   |   |   |   |   |
|----------------|----------------|-------------------------------------------------------------|----|----|---|---|---|---|---|
|                |                | 0                                                           | 0  | 0  | 0 | 1 | 1 | 1 | 1 |
| 0              | 0              | —                                                           | 11 | 14 | — | — | — | — | 5 |
| 0              | 1              | 8                                                           | 12 | —  | — | — | 1 | 2 | 6 |
| 1              | 0              | 9                                                           | 13 | 15 | — | — | — | 3 | 7 |
| 1              | 1              | 10                                                          | —  | —  | — | — | 0 | 4 | — |

NOTE:

1. Unlisted C<sub>n</sub> combinations are no correction.

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Table 22. CODE ID<sub>2-0</sub> = 010

| S <sub>2</sub> | S <sub>1</sub> | S <sub>6</sub> S <sub>5</sub> S <sub>4</sub> S <sub>3</sub> |   |   |   |    |    |    |   |
|----------------|----------------|-------------------------------------------------------------|---|---|---|----|----|----|---|
|                |                | 0                                                           | 0 | 0 | 0 | 1  | 1  | 1  | 1 |
| 0              | 0              | —                                                           | — | — | 5 | —  | 11 | 14 | — |
| 0              | 1              | —                                                           | 1 | 2 | 6 | 8  | 12 | —  | — |
| 1              | 0              | —                                                           | — | 3 | 7 | 9  | 13 | 15 | — |
| 1              | 1              | —                                                           | 0 | 4 | — | 10 | —  | —  | — |

NOTE:

1. Unlisted S combinations are no correction.

2595 tbl 29

Table 23. CODE ID<sub>2-0</sub> = 011

| C <sub>2</sub> | C <sub>1</sub> | C <sub>0</sub> C <sub>6</sub> C <sub>5</sub> C <sub>4</sub> C <sub>3</sub> |    |    |   |   |   |   |   |
|----------------|----------------|----------------------------------------------------------------------------|----|----|---|---|---|---|---|
|                |                | 0                                                                          | 0  | 0  | 0 | 1 | 1 | 1 | 1 |
| 0              | 0              | —                                                                          | 11 | 14 | — | — | — | — | 5 |
| 0              | 1              | 8                                                                          | 12 | —  | — | — | 1 | 2 | 6 |
| 1              | 0              | 9                                                                          | 13 | 15 | — | — | — | 3 | 7 |
| 1              | 1              | 10                                                                         | —  | —  | — | — | 0 | 4 | — |

NOTE:

1. Unlisted C<sub>n</sub> combinations are no correction.

2595 tbl 30

Table 24. CODE ID<sub>2-0</sub> = 100

| C <sub>2</sub> | C <sub>1</sub> | C <sub>0</sub> C <sub>6</sub> C <sub>5</sub> C <sub>4</sub> C <sub>3</sub> |   |   |   |    |    |    |   |
|----------------|----------------|----------------------------------------------------------------------------|---|---|---|----|----|----|---|
|                |                | 0                                                                          | 0 | 0 | 0 | 1  | 1  | 1  | 1 |
| 0              | 0              | —                                                                          | — | — | 5 | —  | 11 | 14 | — |
| 0              | 1              | —                                                                          | 1 | 2 | 6 | 8  | 12 | —  | — |
| 1              | 0              | —                                                                          | — | 3 | 7 | 9  | 13 | 15 | — |
| 1              | 1              | —                                                                          | 0 | 4 | — | 10 | —  | —  | — |

NOTE:

1. Unlisted C<sub>n</sub> combinations are no correction.

2595 tbl 31

Table 25. CODE ID<sub>2-0</sub> = 101

| C <sub>2</sub> | C <sub>1</sub> | C <sub>0</sub> C <sub>6</sub> C <sub>5</sub> C <sub>4</sub> C <sub>3</sub> |   |   |   |    |    |    |   |
|----------------|----------------|----------------------------------------------------------------------------|---|---|---|----|----|----|---|
|                |                | 0                                                                          | 0 | 0 | 0 | 1  | 1  | 1  | 1 |
| 0              | 0              | —                                                                          | — | — | 5 | —  | 11 | 14 | — |
| 0              | 1              | —                                                                          | 1 | 2 | 6 | 8  | 12 | —  | — |
| 1              | 0              | —                                                                          | — | 3 | 7 | 9  | 13 | 15 | — |
| 1              | 1              | —                                                                          | 0 | 4 | — | 10 | —  | —  | — |

NOTE:

1. Unlisted C<sub>n</sub> combinations are no correction.

2595 tbl 32

Table 26. CODE ID<sub>2-0</sub> = 110

| C <sub>2</sub> | C <sub>1</sub> | C <sub>0</sub> C <sub>6</sub> C <sub>5</sub> C <sub>4</sub> C <sub>3</sub> |    |    |   |   |   |   |   |
|----------------|----------------|----------------------------------------------------------------------------|----|----|---|---|---|---|---|
|                |                | 0                                                                          | 0  | 0  | 0 | 1 | 1 | 1 | 1 |
| 0              | 0              | —                                                                          | 11 | 14 | — | — | — | — | 5 |
| 0              | 1              | 8                                                                          | 12 | —  | — | — | 1 | 2 | 6 |
| 1              | 0              | 9                                                                          | 13 | 15 | — | — | — | 3 | 7 |
| 1              | 1              | 10                                                                         | —  | —  | — | — | 0 | 4 | — |

NOTE:

1. Unlisted C<sub>n</sub> combinations are no correction.

2595 tbl 33

Table 27. CODE ID<sub>2-0</sub> = 111

4825771 0016248 050

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

| Symbol            | Rating                                  | Com'l.                        | Mil.                          | Unit |
|-------------------|-----------------------------------------|-------------------------------|-------------------------------|------|
| VTERM             | Terminal Voltage with Respect to Ground | -0.5 to V <sub>CC</sub> + 0.5 | -0.5 to V <sub>CC</sub> + 0.5 | V    |
| V <sub>CC</sub>   | Power Supply Voltage                    | -0.5 to +7.0                  | -0.5 to +7.0                  | V    |
| T <sub>A</sub>    | Operating Temperature                   | 0 to +70                      | -55 to +125                   | °C   |
| T <sub>BIAS</sub> | Temperature Under Bias                  | -55 to +125                   | -65 to +135                   | °C   |
| T <sub>STG</sub>  | Storage Temperature                     | -55 to +125                   | -65 to +150                   | °C   |
| I <sub>OUT</sub>  | DC Output Current                       | 30                            | 30                            | mA   |

**NOTE:** 2595 tbl 34  
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## CAPACITANCE (T<sub>A</sub> = +25°C, f = 1.0MHz)

| Symbol           | Parameter <sup>(1)</sup> | Conditions            | Typ. | Unit |
|------------------|--------------------------|-----------------------|------|------|
| C <sub>IN</sub>  | Input Capacitance        | V <sub>IN</sub> = 0V  | 5    | pF   |
| C <sub>OUT</sub> | Output Capacitance       | V <sub>OUT</sub> = 0V | 7    | pF   |

**NOTE:** 2595 tbl 35  
1. This parameter is sampled and not 100% tested.

## DC ELECTRICAL CHARACTERISTICS

Commercial: T<sub>A</sub> = 0°C to +70°C, V<sub>CC</sub> = 5.0V ± 5%; Military: T<sub>A</sub> = -55°C to +125°C, V<sub>CC</sub> = 5.0V ± 10%  
V<sub>LC</sub> = 0.2V; V<sub>HC</sub> = V<sub>CC</sub> - 0.2V

| Symbol          | Parameter                                 | Test Conditions <sup>(1)</sup>                               | Min.                                    | Typ. <sup>(2)</sup> | Max.            | Unit |
|-----------------|-------------------------------------------|--------------------------------------------------------------|-----------------------------------------|---------------------|-----------------|------|
| V <sub>IH</sub> | Input HIGH Level                          | Guaranteed Logic HIGH Level <sup>(4)</sup>                   | 2.0                                     | —                   | —               | V    |
| V <sub>IL</sub> | Input LOW Level                           | Guaranteed Logic LOW Level <sup>(4)</sup>                    | —                                       | —                   | 0.8             | V    |
| I <sub>IH</sub> | Input HIGH Current                        | V <sub>CC</sub> = Max., V <sub>IN</sub> = V <sub>CC</sub>    | —                                       | 0.1                 | 5               | μA   |
| I <sub>IL</sub> | Input LOW Current                         | V <sub>CC</sub> = Max., V <sub>IN</sub> = GND                | —                                       | -0.1                | -5              | μA   |
| V <sub>OH</sub> | Output HIGH Voltage                       | V <sub>CC</sub> = Min.                                       | I <sub>OH</sub> = -300μA                | V <sub>HC</sub>     | V <sub>CC</sub> | V    |
|                 |                                           |                                                              | I <sub>OH</sub> = -6mA MIL.             | 2.4                 | 4.3             |      |
|                 |                                           |                                                              | I <sub>OH</sub> = -6mA COM'L.           | 2.4                 | 4.3             |      |
| V <sub>OL</sub> | Output LOW Voltage                        | V <sub>CC</sub> = Min.                                       | I <sub>OL</sub> = 300μA                 | —                   | GND             | V    |
|                 |                                           |                                                              | I <sub>OL</sub> = 8mA MIL.              | —                   | 0.3             |      |
|                 |                                           |                                                              | I <sub>OL</sub> = 8mA COM'L.            | —                   | 0.3             |      |
| I <sub>OZ</sub> | Off State (High Impedance) Output Current | V <sub>CC</sub> = Max.                                       | V <sub>O</sub> = 0V                     | —                   | -0.1            | μA   |
|                 |                                           |                                                              | V <sub>O</sub> = V <sub>CC</sub> (Max.) | —                   | 0.1             |      |
| I <sub>OS</sub> | Output Short Circuit Current              | V <sub>CC</sub> = Max., V <sub>OUT</sub> = 0V <sup>(3)</sup> | -20                                     | —                   | —               | mA   |

**NOTES:** 2595 tbl 36  
1. For conditions shown as Max. or Min. use appropriate value specified under DC Electrical Characteristics.  
2. Typical values are at V<sub>CC</sub> = 5.0V, +25°C ambient and maximum loading.  
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.  
4. These input levels should only be static tested in a noise-free environment. Guaranteed by design.

## DC ELECTRICAL CHARACTERISTICS (Cont'd.)

Commercial: TA = 0°C to +70°C, VCC = 5.0V ± 5%; Military: TA = -55°C to +125°C, VCC = 5.0V ± 10%  
VLC = 0.2V; VHC = VCC - 0.2V

| Symbol | Parameter                                                                  | Test Conditions <sup>(1)</sup>                                                                                                                                                       | Min.   | Typ. <sup>(2)</sup> | Max. | Unit      |
|--------|----------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|---------------------|------|-----------|
| Iccq   | Quiescent Power Supply Current (CMOS) Inputs                               | VCC = Max.<br>VIN = VCC or GND<br>fOP = 0                                                                                                                                            | —      | 3.0                 | 5.0  | mA        |
| Icct   | Quiescent Input Power Supply Current (per Input @ TTL High) <sup>(3)</sup> | VCC = Max., VIN = 3.4V, fOP = 0                                                                                                                                                      | —      | 0.3                 | 2.0  | mA/ Input |
| Iccp   | Dynamic Power Supply Current                                               | VCC = Max.<br>VIN = VCC or GND<br>Outputs Open, OE = L                                                                                                                               | MIL.   | —                   | 5.0  | 8.5       |
|        |                                                                            |                                                                                                                                                                                      | COM'L. | —                   | 5.0  | 7.0       |
| Icc    | Total Power Supply Current <sup>(4)</sup>                                  | VCC = Max., fOP = 10MHz<br>Outputs Open, OE = L<br>50% Duty Cycle<br>VIN = VCC or GND<br>VCC = Max., fOP = 10MHz<br>Outputs Open, OE = L<br>50% Duty Cycle<br>VIN = 3.4V, VIN = 0.4V | MIL.   | —                   | 53   | 90        |
|        |                                                                            |                                                                                                                                                                                      | COM'L. | —                   | 53   | 75        |
|        |                                                                            |                                                                                                                                                                                      | MIL.   | —                   | 60   | 100       |
|        |                                                                            |                                                                                                                                                                                      | COM'L. | —                   | 60   | 85        |

### NOTES:

2595 tbl 37

- For conditions shown as Max. or Min. use appropriate value specified under DC Electrical Characteristics.
- Typical values are at VCC = 5.0V, +25°C ambient and maximum loading.
- Icct is derived by measuring the total current with all the inputs tied together at 3.4V, subtracting out Iccq, then dividing by the total number of inputs.
- Total Supply Current is the sum of the Quiescent Current and the Dynamic Current (at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:  

$$I_{CC} = I_{CCQ} + I_{CCT} (NT \times DH) + I_{CCP} (fOP)$$

DH = Data duty cycle TTL high period (VIN = 3.4V)  
NT = Number of dynamic inputs driven at TTL levels  
fOP = Operating frequency

IDT 39C60B AC ELECTRICAL CHARACTERISTICS

**Guaranteed Commercial Range Performance:** Temperature range: 0°C to +70°C; VCC = 5.0V ± 5%  
The signals switch between 0V and 3V with signal measured at 1.5V level.

**MAXIMUM PROPAGATION DELAYS** CL = 50pF

| From Input                               | To Output |                   |       |            |      |
|------------------------------------------|-----------|-------------------|-------|------------|------|
|                                          | SC0-6     | DATA0-15          | ERROR | MULT ERROR | Unit |
| DATA0-15                                 | 18        | 25 <sup>(1)</sup> | 18    | 20         | ns   |
| CB0-6 (CODE ID = 000, 011)               | 12        | 22                | 17    | 20         | ns   |
| CB0-6 (CODE ID = 010, 100,101, 110, 111) | 12        | 16                | 17    | 20         | ns   |
| GENERATE                                 | 15        | —                 | 14    | 19         | ns   |
| CORRECT                                  | —         | 22                | —     | —          | ns   |
| (Not Internal Control Mode)              |           |                   |       |            |      |
| DIAG MODE and PASSTHRU                   | 20        | 22                | 16    | 19         | ns   |
| (Not Internal Control Mode)              |           |                   |       |            |      |
| CODE ID                                  | 20        | 22                | 22    | 24         | ns   |
| LEIN                                     | 20        | 28                | 20    | 22         | ns   |
| From latched to transparent              |           |                   |       |            |      |
| LEOUT                                    | —         | 11                | —     | —          | ns   |
| From latched to transparent              |           |                   |       |            |      |
| LEDIAG                                   | 20        | 28                | 20    | 22         | ns   |
| From latched to transparent              |           |                   |       |            |      |
| Internal Control Mode: LEDIAG            | 24        | 33                | 24    | 27         | ns   |
| From latched to transparent              |           |                   |       |            |      |
| Internal Control Mode: DATA0-15          | 24        | 33                | 24    | 27         | ns   |
| Via Diagnostic Latch                     |           |                   |       |            |      |

**NOTE:** 1. DATAin to corrected DATAout measurement requires timing as shown below. 2595 tbl 38

MINIMUM SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

| From Input                                | To Input<br>(Latching Data) |        | Set-up Time | Hold Time | Unit |
|-------------------------------------------|-----------------------------|--------|-------------|-----------|------|
| DATA0-15                                  | ✂                           | LEIN   | 5           | 3         | ns   |
| CB0-6 (not applic. to CODE ID = 11)       |                             |        | 5           | 3         | ns   |
| DATA0-15                                  | ✂                           | LEOUT  | 24          | 2         | ns   |
| CB0-7 (CODE ID = 000, 011)                |                             |        | 21          | 0         | ns   |
| CB0-7 (CODE ID = 010, 100, 101, 110, 111) |                             |        | 21          | 0         | ns   |
| CORRECT                                   |                             |        | 22          | 0         | ns   |
| DIAG MODE                                 |                             |        | 22          | 0         | ns   |
| PASSTHRU                                  |                             |        | 22          | 0         | ns   |
| CODE ID1, 0                               |                             |        | 25          | 0         | ns   |
| LEIN                                      |                             |        | 28          | 0         | ns   |
| DATA0-15                                  |                             | LEDIAG | 5           | 3         | ns   |

MAXIMUM OUTPUT ENABLE/DISABLE TIMES

Output tests specified with CL = 5pF and measured to 0.5V change of output voltage level. Test performed with CL = 50pF and correlated to CL = 5pF.

| From Input  | Enable | Disable | To Output | Enable Max. | Disable Max. | Unit |
|-------------|--------|---------|-----------|-------------|--------------|------|
| OE Byte0, 1 | ✂      | ✂       | DAT0-15   | 12          | 10           | ns   |
| OEsc        | ✂      | ✂       | SC0-7     | 12          | 10           | ns   |

MINIMUM PULSE WIDTHS

|                     |   |                        |      |   |    |
|---------------------|---|------------------------|------|---|----|
| LEIN, LEOUT, LEDIAG | ✂ | (Positive-going pulse) | Min. | 8 | ns |
|---------------------|---|------------------------|------|---|----|

## IDT 39C60B AC ELECTRICAL CHARACTERISTICS

**Guaranteed Military Range Performance:** Temperature range:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ;  $V_{CC} = 5.0\text{V} \pm 10\%$   
The inputs switch between 0V to 3V with signal measured at the 1.5V level.

**MAXIMUM PROPAGATION DELAYS**  $C_L = 50\text{pF}$

| From Input                                                   | To Output |                   |       |            |      |
|--------------------------------------------------------------|-----------|-------------------|-------|------------|------|
|                                                              | SC0-6     | DATA0-15          | ERROR | MULT ERROR | Unit |
| DATA0-15                                                     | 22        | 30 <sup>(1)</sup> | 22    | 25         | ns   |
| CB0-6 (CODE ID = 000, 011)                                   | 14        | 26                | 20    | 24         | ns   |
| CB0-6 (CODE ID = 010, 100, 101, 110, 111)                    | 14        | 19                | 20    | 24         | ns   |
| GENERATE                                                     | —         | —                 | 14    | 19         | ns   |
|                                                              | 15        | —                 | —     | —          | —    |
| CORRECT<br>(Not Internal Control Mode)                       | —         | 20                | —     | —          | ns   |
| DIAG MODE and PASSTHRU<br>(Not Internal Control Mode)        | 24        | 26                | 19    | 21         | ns   |
| CODE ID                                                      | 24        | 29                | 26    | 29         | ns   |
| LEIN<br>From latched to transparent                          | 24        | 34                | 24    | 26         | ns   |
| LEOUT<br>From latched to transparent                         | —         | 13                | —     | —          | ns   |
| Internal Control Mode: LEDIAG<br>From latched to transparent | 24        | 34                | 24    | 26         | ns   |
| LEDIAG<br>From latched to transparent                        | 29        | 40                | 29    | 32         | ns   |
| Internal Control Mode: DATA0-15<br>Via Diagnostic Latch      | 29        | 40                | 29    | 32         | ns   |

**NOTE:**

1. DATAIN to corrected DATAout measurement requires timing as shown below.

2595 tbl 42

### MINIMUM SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

| From Input                                | To Input<br>(Latching Data) | Set-up Time | Hold Time | Unit |
|-------------------------------------------|-----------------------------|-------------|-----------|------|
| DATA0-15                                  | LEIN                        | 6           | 4         | ns   |
| CB0-6 (not applic. to CODE ID = 11)       |                             | 6           | 4         | ns   |
| DATA0-15                                  | LEOUT                       | 29          | 2         | ns   |
| CB0-7 (CODE ID = 000, 011)                |                             | 25          | 0         | ns   |
| CB0-7 (CODE ID = 010, 100, 101, 110, 111) |                             | 25          | 0         | ns   |
| CORRECT                                   |                             | 26          | —         | ns   |
| DIAG MODE                                 |                             | 26          | 0         | ns   |
| PASSTHRU                                  |                             | 26          | 0         | ns   |
| CODE ID1,0                                |                             | 30          | 0         | ns   |
| LEIN                                      |                             | 34          | —         | ns   |
| DATA0-15                                  | LEDIAG                      | 6           | 4         | ns   |

2595 tbl 43

### MAXIMUM OUTPUT ENABLE/DISABLE TIMES

Output tests specified with  $C_L = 5\text{pF}$  and measured to 0.5V change of output voltage level. Test performed with  $C_L = 50\text{pF}$  and correlated to  $C_L = 5\text{pF}$ .

| From Input | Enable | Disable | To Output | Enable Max. | Disable Max. | Unit |
|------------|--------|---------|-----------|-------------|--------------|------|
| OE Byte0,1 |        |         | DAT0-15   | 15          | 12           | ns   |
| OEsc       |        |         | SC0-7     | 15          | 12           | ns   |

### MINIMUM PULSE WIDTHS

|                     |                        |      |      |
|---------------------|------------------------|------|------|
| LEIN, LEOUT, LEDIAG | (Positive-going pulse) | Min. | Unit |
|                     |                        | 10   | ns   |

2595 tbl 45



## IDT 39C60A AC ELECTRICAL CHARACTERISTICS

**Guaranteed Commercial Range Performance:** Temperature range: 0°C to +70°C; V<sub>CC</sub> = 5.0V ± 5%  
The signals switch between 0V and 3V with signal measured at 1.5V level.

**MAXIMUM PROPAGATION DELAYS** CL = 50pF

| From Input                                                   |                                                                                   | To Output |                   |         |           |      |
|--------------------------------------------------------------|-----------------------------------------------------------------------------------|-----------|-------------------|---------|-----------|------|
|                                                              |                                                                                   | SC0-6     | DATA0-15          | ERROR   | MULTERROR | Unit |
| DATA0-15                                                     |                                                                                   | 20        | 30 <sup>(1)</sup> | 20      | 23        | ns   |
| CB0-6 (CODE ID = 000, 011)                                   |                                                                                   | 14        | 25                | 20      | 23        | ns   |
| CB0-6 (CODE ID = 010, 100, 101, 110, 111)                    |                                                                                   | 14        | 18                | 20      | 23        | ns   |
| GENERATE                                                     |  | —<br>15   | 33<br>—           | 18<br>— | 23<br>—   | ns   |
| CORRECT<br>(Not Internal Control Mode)                       |                                                                                   | —         | 20                | —       | —         | ns   |
| DIAG MODE and PASSTHRU<br>(Not Internal Control Mode)        |                                                                                   | 22        | 25                | 18      | 21        | ns   |
| CODE ID                                                      |                                                                                   | 23        | 28                | 25      | 28        | ns   |
| LEIN<br>From latched to transparent                          |  | 22        | 32                | 22      | 25        | ns   |
| LEOUT<br>From latched to transparent                         |  | —         | 13                | —       | —         | ns   |
| LEDIAG<br>From latched to transparent                        |  | 22        | 32                | 22      | 25        | ns   |
| Internal Control Mode: LEDIAG<br>From latched to transparent |  | 28        | 38                | 28      | 31        | ns   |
| Internal Control Mode: DATA0-15<br>Via Diagnostic Latch      |                                                                                   | 28        | 38                | 28      | 31        | ns   |

**NOTE:**

1. DATAIN to corrected DATAOUT measurement requires timing as shown below.

2595 tbi 46

### MINIMUM SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

| From Input                                | To Input<br>(Latching Data)                                                         |        | Set-up Time | Hold Time | Unit |
|-------------------------------------------|-------------------------------------------------------------------------------------|--------|-------------|-----------|------|
| DATA0-15                                  |    | LEIN   | 5           | 3         | ns   |
| CB0-6 (not applic. to CODE ID = 11)       |    |        | 5           | 3         | ns   |
| DATA0-15                                  |  | LEOUT  | 24          | 2         | ns   |
| CB0-7 (CODE ID = 000, 011)                |  |        | 21          | 0         | ns   |
| CB0-7 (CODE ID = 010, 100, 101, 110, 111) |  |        | 21          | 0         | ns   |
| CORRECT                                   |  |        | 22          | 0         | ns   |
| DIAG MODE                                 |  |        | 22          | 0         | ns   |
| PASSTHRU                                  |  |        | 22          | 0         | ns   |
| CODE ID1, 0                               |  |        | 25          | 0         | ns   |
| LEIN                                      |  |        | 28          | 0         | ns   |
| DATA0-15                                  |                                                                                     | LEDIAG | 5           | 3         | ns   |

2595 tbi 47

### MAXIMUM OUTPUT ENABLE/DISABLE TIMES

Output tests specified with CL = 5pF and measured to 0.5V change of output voltage level. Test performed with CL = 50pF and correlated to CL = 5pF.

| From Input | Enable                                                                              | Disable                                                                             | To Output | Enable Max. | Disable Max. | Unit |
|------------|-------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|-----------|-------------|--------------|------|
| OEByte0, 1 |  |  | DAT0-15   | 24          | 21           | ns   |
| OESc       |  |  | SC0-7     | 24          | 21           | ns   |

### MINIMUM PULSE WIDTHS

|                     |                                                                                     |                        | Min. |    |
|---------------------|-------------------------------------------------------------------------------------|------------------------|------|----|
| LEIN, LEOUT, LEDIAG |  | (Positive-going pulse) | 12   | ns |

2595 tbi 48

2595 tbi 49

## IDT 39C60A AC ELECTRICAL CHARACTERISTICS

**Guaranteed Military Range Performance:** Temperature range:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ;  $V_{\text{CC}} = 5.0\text{V} \pm 10\%$   
The inputs switch between 0V to 3V with signal measured at the 1.5V level.

### MAXIMUM PROPAGATION DELAYS $C_L = 50\text{pF}$

| From Input                                                   |                                                                                   | To Output |                   |       |            | Unit |
|--------------------------------------------------------------|-----------------------------------------------------------------------------------|-----------|-------------------|-------|------------|------|
|                                                              |                                                                                   | SC0-6     | DATA0-15          | ERROR | MULT ERROR |      |
| DATA0-15                                                     |                                                                                   | 22        | 35 <sup>(1)</sup> | 24    | 27         | ns   |
| CB0-6 (CODE ID = 000, 011)                                   |                                                                                   | 17        | 25                | 24    | 27         | ns   |
| CB0-6 (CODE ID = 010, 100, 101, 110, 111)                    |                                                                                   | 17        | 20                | 24    | 27         | ns   |
| GENERATE                                                     |  | —         | 28                | 21    | 25         | ns   |
|                                                              |  | 20        | —                 | —     | —          | ns   |
| CORRECT<br>(Not Internal Control Mode)                       |                                                                                   | —         | 25                | —     | —          | ns   |
| DIAG MODE and PASSTHRU<br>(Not Internal Control Mode)        |                                                                                   | 25        | 28                | 21    | 24         | ns   |
| CODE ID                                                      |                                                                                   | 26        | 31                | 28    | 31         | ns   |
| LEIN<br>From latched to transparent                          |  | 24        | 37                | 26    | 29         | ns   |
| LEOUT<br>From latched to transparent                         |  | —         | 16                | —     | —          | ns   |
| LEDIAG<br>From latched to transparent                        |  | 24        | 37                | 26    | 29         | ns   |
| Internal Control Mode: LEDIAG<br>From latched to transparent |  | 30        | 43                | 32    | 35         | ns   |
| Internal Control Mode: DATA0-15<br>Via Diagnostic Latch      |                                                                                   | 30        | 43                | 32    | 35         | ns   |

#### NOTE:

1. DATAIN to corrected DATAOUT measurement requires timing as shown below.

2595 tbl 50

### MINIMUM SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

| From Input                                | To Input<br>(Latching Data)                                                         |        | Set-up Time | Hold Time | Unit |
|-------------------------------------------|-------------------------------------------------------------------------------------|--------|-------------|-----------|------|
| DATA0-15                                  |    | LEIN   | 5           | 3         | ns   |
| CB0-6 (not applic. to CODE ID = 11)       |   |        | 5           | 3         | ns   |
| DATA0-15                                  |  | LEOUT  | 27          | 2         | ns   |
| CB0-7 (CODE ID = 000, 011)                |  |        | 24          | 0         | ns   |
| CB0-7 (CODE ID = 010, 100, 101, 110, 111) |  |        | 24          | 0         | ns   |
| CORRECT                                   |  |        | 25          | 0         | ns   |
| DIAG MODE                                 |  |        | 25          | 0         | ns   |
| PASSTHRU                                  |  |        | 25          | 0         | ns   |
| CODE ID1,0                                |  |        | 28          | 0         | ns   |
| LEIN                                      |  |        | 30          | 0         | ns   |
| DATA0-15                                  |                                                                                     | LEDIAG | 5           | 3         | ns   |

2595 tbl 51

### MAXIMUM OUTPUT ENABLE/DISABLE TIMES

Output tests specified with  $C_L = 5\text{pF}$  and measured to 0.5V change of output voltage level. Test performed with  $C_L = 50\text{pF}$  and correlated to  $C_L = 5\text{pF}$ .

| From Input  | Enable                                                                              | Disable                                                                             | To Output | Enable Max. | Disable Max. | Unit |
|-------------|-------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|-----------|-------------|--------------|------|
| OE Byte0, 1 |  |  | DAT0-15   | 24          | 21           | ns   |
| OESc        |  |  | SC0-7     | 24          | 21           | ns   |

### MINIMUM PULSE WIDTHS

|                                                                                                                                |  |  |  | Min. | Unit |
|--------------------------------------------------------------------------------------------------------------------------------|--|--|--|------|------|
| LEIN, LEOUT, LEDIAG  (Positive-going pulse) |  |  |  | 12   | ns   |

2595 tbl 53

## IDT 39C60-1 AC ELECTRICAL CHARACTERISTICS

**Guaranteed Commercial Range Performance:** Temperature range: 0°C to +70°C; V<sub>CC</sub> = 5.0V ± 5%

The signals switch between 0V and 3V with signal measured at 1.5V level.

**MAXIMUM PROPAGATION DELAYS** C<sub>L</sub> = 50pF

| From Input                                                   |  | To Output |                   |       |            |      |
|--------------------------------------------------------------|--|-----------|-------------------|-------|------------|------|
|                                                              |  | SC0-6     | DATA0-15          | ERROR | MULT ERROR | Unit |
| DATA0-15                                                     |  | 28        | 52 <sup>(1)</sup> | 25    | 50         | ns   |
| CB0-6 (CODE ID = 000, 011)                                   |  | 23        | 50                | 23    | 47         | ns   |
| CB0-6 (CODE ID = 010, 100, 101, 110, 111)                    |  | 28        | 34                | 29    | 34         | ns   |
| GENERATE                                                     |  | —         | 63                | 36    | 55         | ns   |
|                                                              |  | 35        | —                 | —     | —          | ns   |
| CORRECT<br>(Not Internal Control Mode)                       |  | —         | 45                | —     | —          | ns   |
| DIAG MODE (Not Internal Control Mode)                        |  | 50        | 78                | 59    | 75         | ns   |
| PASSTHRU (Not Internal Control Mode)                         |  | 36        | 44                | 29    | 46         | ns   |
| CODE ID                                                      |  | 61        | 90                | 60    | 80         | ns   |
| LEIN<br>From latched to transparent                          |  | 39        | 72                | 39    | 59         | ns   |
| LEOUT<br>From latched to transparent                         |  | —         | 31                | —     | —          | ns   |
| LEDIAG<br>From latched to transparent                        |  | 45        | 78                | 45    | 65         | ns   |
| Internal Control Mode: LEDIAG<br>From latched to transparent |  | 67        | 96                | 66    | 86         | ns   |
| Internal Control Mode: DATA0-15<br>Via Diagnostic Latch      |  | 67        | 96                | 66    | 86         | ns   |

**NOTE:**

1. DATA<sub>IN</sub> to corrected DATA<sub>OUT</sub> measurement requires timing as shown below.

2595 tbl 54

### MINIMUM SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

| From Input                                |  | To Input<br>(Latching Data) |        | Set-up Time | Hold Time | Unit |
|-------------------------------------------|--|-----------------------------|--------|-------------|-----------|------|
|                                           |  |                             |        |             |           |      |
| DATA0-15                                  |  |                             | LEIN   | 6           | 7         | ns   |
| CB0-6 (not applic. to CODE ID = 11)       |  |                             |        | 5           | 6         | ns   |
| DATA0-15                                  |  |                             | LEOUT  | 34          | 5         | ns   |
| CB0-7 (CODE ID = 000, 011)                |  |                             |        | 35          | 0         | ns   |
| CB0-7 (CODE ID = 010, 100, 101, 110, 111) |  |                             |        | 27          | 0         | ns   |
| CORRECT                                   |  |                             |        | 26          | 1         | ns   |
| DIAG MODE                                 |  |                             |        | 69          | 0         | ns   |
| PASSTHRU                                  |  |                             |        | 26          | 0         | ns   |
| CODE ID <sub>1,0</sub>                    |  |                             |        | 81          | 0         | ns   |
| LEIN                                      |  |                             |        | 51          | 5         | ns   |
| DATA0-15                                  |  |                             | LEDIAG | 6           | 8         | ns   |

2595 tbl 55

### MAXIMUM OUTPUT ENABLE/DISABLE TIMES

Output tests specified with C<sub>L</sub> = 5pF and measured to 0.5V change of output voltage level. Test performed with C<sub>L</sub> = 50pF and correlated to C<sub>L</sub> = 5pF.

| From Input             |  | Enable | Disable | To Output |  | Enable<br>Max. | Disable<br>Max. | Unit |
|------------------------|--|--------|---------|-----------|--|----------------|-----------------|------|
|                        |  |        |         |           |  |                |                 |      |
| OE Byte <sub>0,1</sub> |  |        |         | DATA0-15  |  | 30             | 30              | ns   |
| OESc                   |  |        |         | SC0-7     |  | 30             | 30              | ns   |

### MINIMUM PULSE WIDTHS

|                     |  |                        |      |    |    |
|---------------------|--|------------------------|------|----|----|
| LEIN, LEOUT, LEDIAG |  | (Positive-going pulse) | Min. | 15 | ns |
|---------------------|--|------------------------|------|----|----|

2595 tbl 57

## IDT 39C60-1 AC ELECTRICAL CHARACTERISTICS

**Guaranteed Military Range Performance:** Temperature range:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ;  $V_{CC} = 5.0\text{V} \pm 10\%$   
The inputs switch between 0V to 3V with signal measured at the 1.5V level.

**MAXIMUM PROPAGATION DELAYS**  $C_L = 50\text{pF}$

| From Input                                                   |  | To Output |                   |       |            |
|--------------------------------------------------------------|--|-----------|-------------------|-------|------------|
|                                                              |  | SC0-6     | DATA0-15          | ERROR | MULT ERROR |
| DATA0-15                                                     |  | 31        | 59 <sup>(1)</sup> | 28    | 56         |
| CB0-6 (CODE ID = 000, 011)                                   |  | 25        | 55                | 25    | 50         |
| CB0-6 (CODE ID = 010, 100, 101, 110, 111)                    |  | 30        | 38                | 31    | 37         |
| GENERATE                                                     |  | —         | 63                | 36    | 55         |
|                                                              |  | 38        | —                 | —     | —          |
| CORRECT<br>(Not Internal Control Mode)                       |  | —         | 49                | —     | —          |
| DIAG MODE (Not Internal Control Mode)                        |  | 58        | 89                | 65    | 90         |
| PASSTHRU (Not Internal Control Mode)                         |  | 39        | 51                | 34    | 54         |
| CODE ID                                                      |  | 69        | 100               | 68    | 90         |
| LEIN<br>From latched to transparent                          |  | 39        | 82                | 43    | 66         |
| LEOUT<br>From latched to transparent                         |  | —         | 33                | —     | —          |
| LEDIAG<br>From latched to transparent                        |  | 50        | 88                | 49    | 72         |
| Internal Control Mode: LEDIAG<br>From latched to transparent |  | 75        | 106               | 74    | 96         |
| Internal Control Mode: DATA0-15<br>Via Diagnostic Latch      |  | 75        | 106               | 74    | 96         |

**NOTE:**

1. DATAin to corrected DATAout measurement requires timing as shown below.

2595 tbl 58

### MINIMUM SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

| From Input                                | To Input<br>(Latching Data) |        | Set-up Time | Hold Time | Unit |
|-------------------------------------------|-----------------------------|--------|-------------|-----------|------|
| DATA0-15                                  |                             | LEIN   | 7           | 7         | ns   |
| CB0-6 (not applic. to CODE ID = 11)       |                             |        | 5           | 7         | ns   |
| DATA0-15                                  |                             | LEOUT  | 39          | 5         | ns   |
| CB0-7 (CODE ID = 000, 011)                |                             |        | 38          | 0         | ns   |
| CB0-7 (CODE ID = 010, 100, 101, 110, 111) |                             |        | 30          | 0         | ns   |
| CORRECT                                   |                             |        | 28          | 1         | ns   |
| DIAG MODE                                 |                             |        | 84          | 0         | ns   |
| PASSTHRU                                  |                             |        | 30          | 0         | ns   |
| CODE ID1,0                                |                             |        | 89          | 0         | ns   |
| LEIN                                      |                             |        | 59          | 5         | ns   |
| DATA0-15                                  |                             | LEDIAG | 7           | 9         | ns   |

2595 tbl 59

### MAXIMUM OUTPUT ENABLE/DISABLE TIMES

Output tests specified with  $C_L = 5\text{pF}$  and measured to 0.5V change of output voltage level. Test performed with  $C_L = 50\text{pF}$  and correlated to  $C_L = 5\text{pF}$ .

| From Input | Enable | Disable | To Output | Enable Max. | Disable Max. | Unit |
|------------|--------|---------|-----------|-------------|--------------|------|
| OE Byte0,1 |        |         | DAT0-15   | 35          | 35           | ns   |
| OESc       |        |         | SC0-7     | 35          | 35           | ns   |

2595 tbl 60

### MINIMUM PULSE WIDTHS

|                     |  |                        | Min. | Unit |
|---------------------|--|------------------------|------|------|
| LEIN, LEOUT, LEDIAG |  | (Positive-going pulse) | 15   | ns   |

2595 tbl 61

IDT 39C60 AC ELECTRICAL CHARACTERISTICS

**Guaranteed Commercial Range Performance:** Temperature range: 0°C to +70°C; Vcc = 5.0V ± 5%  
The signals switch between 0V and 3V with signal measured at the 1.5V level.

**MAXIMUM PROPAGATION DELAYS** CL = 50pF

| From Input                                                   |  | To Output |                   |         |            |      |
|--------------------------------------------------------------|--|-----------|-------------------|---------|------------|------|
|                                                              |  | SC0-6     | DATA0-15          | ERROR   | MULT ERROR | Unit |
| DATA0-15                                                     |  | 32        | 65 <sup>(1)</sup> | 32      | 50         | ns   |
| CB0-6 (CODE ID = 000, 011)                                   |  | 28        | 56                | 29      | 47         | ns   |
| CB0-6 (CODE ID = 010, 100, 101, 110, 111)                    |  | 28        | 45                | 29      | 34         | ns   |
| GENERATE                                                     |  | —<br>35   | 63<br>—           | 36<br>— | 55<br>—    | ns   |
| CORRECT<br>(Not Internal Control Mode)                       |  | —         | 45                | —       | —          | ns   |
| DIAG MODE(Not Internal Control Mode)                         |  | 50        | 78                | 59      | 75         | ns   |
| PASSTHRU(Not Internal Control Mode)                          |  | 36        | 44                | 29      | 46         | ns   |
| CODE ID                                                      |  | 61        | 90                | 60      | 80         | ns   |
| LEIN<br>From latched to transparent                          |  | 39        | 72                | 39      | 59         | ns   |
| LEOUT<br>From latched to transparent                         |  | —         | 31                | —       | —          | ns   |
| LEDIAG<br>From latched to transparent                        |  | 45        | 78                | 45      | 65         | ns   |
| Internal Control Mode: LEDIAG<br>From latched to transparent |  | 67        | 96                | 66      | 86         | ns   |
| Internal Control Mode: DATA0-15<br>Via Diagnostic Latch      |  | 67        | 96                | 66      | 86         | ns   |

NOTE:  
1. DATAin to corrected DATAout measurement requires timing as shown below.

2595 tbl 62

MINIMUM SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

| From Input                                | To Input<br>(Latching Data) |        | Set-up Time | Hold Time | Unit |
|-------------------------------------------|-----------------------------|--------|-------------|-----------|------|
| DATA0-15                                  |                             | LEIN   | 6           | 7         | ns   |
| CB0-6 (not applic. to CODE ID = 11)       |                             |        | 5           | 6         | ns   |
| DATA0-15                                  |                             | LEout  | 44          | 5         | ns   |
| CB0-7 (CODE ID = 000, 011)                |                             |        | 35          | 0         | ns   |
| CB0-7 (CODE ID = 010, 100, 101, 110, 111) |                             |        | 27          | 0         | ns   |
| CORRECT                                   |                             |        | 26          | 1         | ns   |
| DIAG MODE                                 |                             |        | 69          | 0         | ns   |
| PASSTHRU                                  |                             |        | 26          | 0         | ns   |
| CODE ID1,0                                |                             |        | 81          | 0         | ns   |
| LEIN                                      |                             |        | 51          | 5         | ns   |
| DATA0-15                                  |                             | LEDIAG | 6           | 8         | ns   |

2595 tbl 63

MAXIMUM OUTPUT ENABLE/DISABLE TIMES

Output tests specified with CL = 5pF and measured to 0.5V change of output voltage level. Test performed with CL = 50pF and correlated to CL = 5pF.

| From Input | Enable | Disable | To Output | Enable Max. | Disable Max. | Unit |
|------------|--------|---------|-----------|-------------|--------------|------|
| OE Byte0,1 |        |         | DAT0-15   | 30          | 30           | ns   |
| OEsc       |        |         | SC0-7     | 30          | 30           | ns   |

2595 tbl 64

MINIMUM PULSE WIDTHS

|                     |  |                        |      |    |    |
|---------------------|--|------------------------|------|----|----|
| LEIN, LEOUT, LEDIAG |  | (Positive-going pulse) | Min. | 15 | ns |
|---------------------|--|------------------------|------|----|----|

2595 tbl 65

## IDT 39C60 AC ELECTRICAL CHARACTERISTICS

**Guaranteed Military Range Performance:** Temperature range: -55°C to +125°C; V<sub>CC</sub> = 5.0V ± 10%

The inputs switch between 0V to 3V with signal measured at the 1.5V level.

### MAXIMUM PROPAGATION DELAYS CL = 50pF

| From Input                                                   |                                                                                   | To Output |                   |       |            |
|--------------------------------------------------------------|-----------------------------------------------------------------------------------|-----------|-------------------|-------|------------|
|                                                              |                                                                                   | SC0-6     | DATA0-15          | ERROR | MULT ERROR |
| DATA0-15                                                     |                                                                                   | 35        | 73 <sup>(1)</sup> | 36    | 56         |
| CB0-6 (CODE ID = 000, 011)                                   |                                                                                   | 30        | 61                | 31    | 50         |
| CB0-6 (CODE ID = 010, 100, 101, 110, 111)                    |                                                                                   | 30        | 50                | 31    | 37         |
| GENERATE                                                     |  | —         | 63                | 36    | 55         |
|                                                              |  | 38        | —                 | —     | —          |
| CORRECT<br>(Not Internal Control Mode)                       |                                                                                   | —         | 49                | —     | —          |
| DIAG MODE(Not Internal Control Mode)                         |                                                                                   | 58        | 89                | 65    | 90         |
| PASSTHRU(Not Internal Control Mode)                          |                                                                                   | 39        | 51                | 34    | 54         |
| CODE ID                                                      |                                                                                   | 69        | 100               | 68    | 90         |
| LEIN<br>From latched to transparent                          |  | 44        | 82                | 43    | 66         |
| LEOUT<br>From latched to transparent                         |  | —         | 33                | —     | —          |
| LEDIAG<br>From latched to transparent                        |  | 50        | 88                | 49    | 72         |
| Internal Control Mode: LEDIAG<br>From latched to transparent |  | 75        | 106               | 74    | 96         |
| Internal Control Mode: DATA0-15<br>Via Diagnostic Latch      |                                                                                   | 75        | 106               | 74    | 96         |

#### NOTE:

1. DATA<sub>IN</sub> to corrected DATA<sub>OUT</sub> measurement requires timing as shown below.

2595 tbl 66

### MINIMUM SET-UP AND HOLD TIMES RELATIVE TO LATCH ENABLES

| From Input                                | To Input<br>(Latching Data)                                                         | Set-up Time | Hold Time | Unit |
|-------------------------------------------|-------------------------------------------------------------------------------------|-------------|-----------|------|
| DATA0-15                                  |    | 7           | 7         | ns   |
| CB0-6 (not applic. to CODE ID = 11)       |                                                                                     |             |           |      |
| DATA0-15                                  |   | 50          | 5         | ns   |
| CB0-7 (CODE ID = 000, 011)                |                                                                                     |             |           |      |
| CB0-7 (CODE ID = 010, 100, 101, 110, 111) |                                                                                     |             |           |      |
| CORRECT                                   |                                                                                     |             |           |      |
| DIAG MODE                                 |                                                                                     |             |           |      |
| PASSTHRU                                  |                                                                                     |             |           |      |
| CODE ID <sub>1,0</sub>                    |  | 89          | 0         | ns   |
| LEIN                                      |                                                                                     |             |           |      |
| DATA0-15                                  |  | 59          | 5         | ns   |
|                                           |                                                                                     |             |           |      |
|                                           |  | 7           | 9         | ns   |
|                                           |                                                                                     |             |           |      |

2595 tbl 67

### MAXIMUM OUTPUT ENABLE/DISABLE TIMES

Output tests specified with CL = 5pF and measured to 0.5V change of output voltage level. Test performed with CL = 50pF and correlated to CL = 5pF.

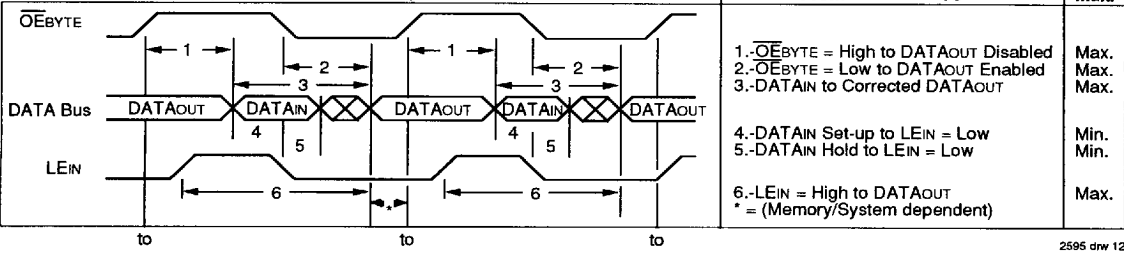
| From Input  | Enable                                                                              | Disable                                                                             | To Output | Enable Max. | Disable Max. | Unit |
|-------------|-------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|-----------|-------------|--------------|------|
| OE Byte0, 1 |  |  | DATA0-15  | 35          | 35           | ns   |
| OEsc        |  |  | SC0-7     | 35          | 35           | ns   |

### MINIMUM PULSE WIDTHS

| LEIN, LEOUT, LEDIAG                                                                                        | Min. | Unit |
|------------------------------------------------------------------------------------------------------------|------|------|
|  (Positive-going pulse) | 15   | ns   |

2595 tbl 69

IDT39C60 — DATAIN TO CORRECTED  
DATAOUT TIMING (Two cycles shown)

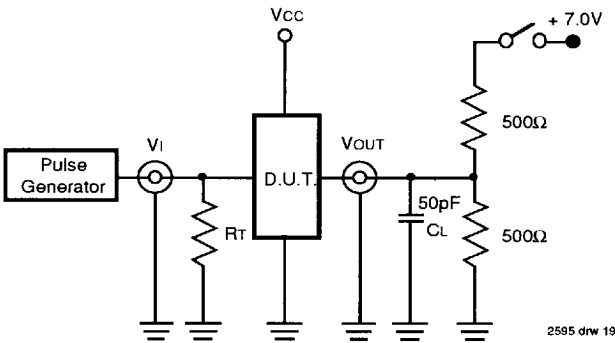


AC TEST CONDITIONS

|                               |              |                   |        |
|-------------------------------|--------------|-------------------|--------|
| Input Pulse Levels            | GND to 3.0V  | Test              | Switch |
| Input Rise/Fall Times         | 1V/ns        | Disable Low       |        |
| Input Timing Reference Levels | 1.5V         | Enable Low        | Closed |
| Output Reference Levels       | 1.5V         | All Other Outputs | Open   |
| Output Load                   | See Figure 9 |                   |        |

2595 tbl 70      2595 tbl 71

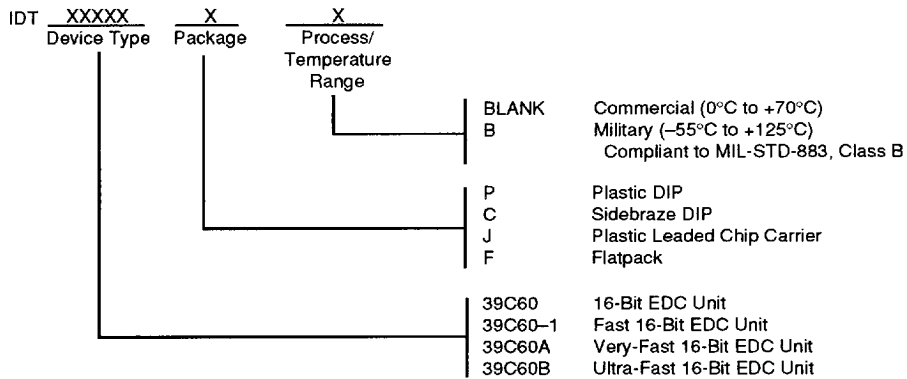
TEST CIRCUIT LOAD



**DEFINITIONS:**  
CL = Load capacitance: includes jig and probe capacitance  
RL = Termination resistance: should be equal to ZOUT of the Pulse Generator

Figure 9.

## ORDERING INFORMATION



2595 drw 20