16-WORD-BY-4-BIT DUAL-PORT RAM

IDT39C705A/B
IDT39C707/A

Integrated Device Technology Inc

MICROSLICE™ PRODUCT

FEATURES:

- Fast
  - Available in either industry-standard speed or 20% speed upgraded versions
- Low-power CEMOS™
  - Military: 50mA (max.)
  - Commercial: 40mA (max.)
- 16-word x 4-bit dual-port CMOS RAM
- Non-inverting data output with respect to data input
- Easily cascadable with separate Write Enables
- Separate 4-bit latches with enables for each output port (IDT39C707/A has separate output control)
- IDT39C705A/B pin-compatible to all versions of the 29705
- IDT39C707/A pin-compatible to all versions of the 29707
- Available in CERDIP, Plastic DIP, LCC and SOIC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT39C705s are high-performance 16-word-by-4-bit dual-port RAMs. Addressing any of the 16 words is performed via the 4-bit A address field with the data appearing on the A output port. The same respective operation holds true for the B address input and output port and can happen simultaneously with the A operation. New incoming data is written into the 4-bit RAM word selected by the B address. The D inputs are used to load new data into the device.

Featured are two separate output ports which allow any two 4-bit words to be read from these outputs simultaneously. Also featured is a 4-bit latch for each of the two output ports with a common Latch Enable (LE) input being used to control all eight latches. Two Write Enable ($\overline{WE}$) inputs are designed such that Write Enable 1 ($\overline{WE}_1$) and Latch Enable (LE) input can be connected to the RAM to operate in an edge-triggered mode. The Write Enable inputs control the writing of new data into the RAM. Data is written into the B address field when the Write Enables are LOW. If either of the Write Enables are HIGH, no data is written into the RAM.

Three-state outputs allow several devices to be easily cascaded for increased memory size. When $\overline{OE}_A$ input is HIGH, the A output port is in the high impedance mode. The same respective operation occurs for the $\overline{OE}_B$ input.

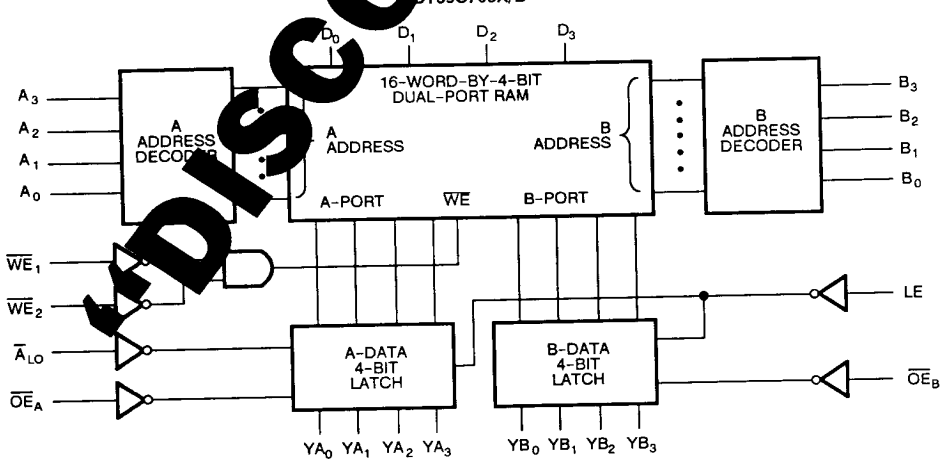
The IDT39C707s function identically to the IDT39C705s, except each output has a separate Latch Enable (LE) input. Also, an extra Write Enable ($\overline{WE}$) may be connected directly to the IEN of the IDT39C203/A for improved cycle times when compared to the IDT39C705s. The $\overline{WE}$/BLE input can then be connected directly to the system clock.

These performance-enhanced, pin-compatible replacements for all respective versions of the 29705s and 29707s are fabricated using IDT's high-speed, high-reliability CEMOS technology.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM

IDT39C705A/B



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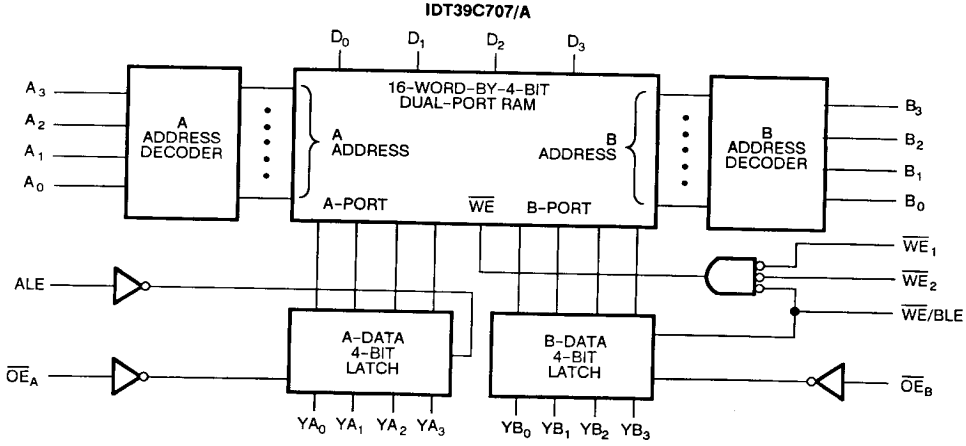
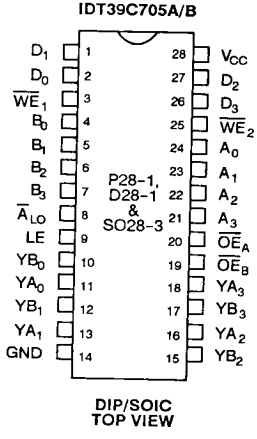
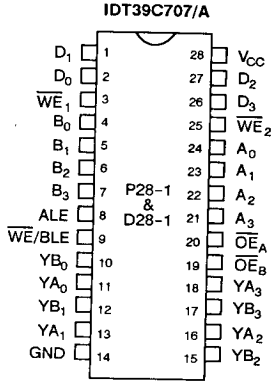
FUNCTIONAL BLOCK DIAGRAM



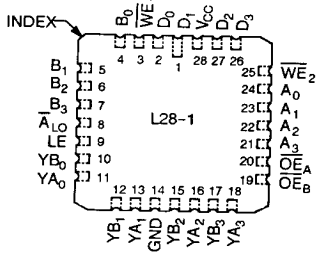
PIN CONFIGURATIONS



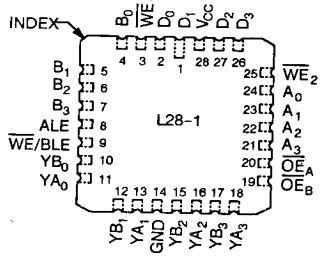
DIP/SOIC TOP VIEW



DIP TOP VIEW



LCC TOP VIEW



LCC TOP VIEW

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PIN DESCRIPTIONS

PIN NAME	I/O	DESCRIPTION
A_0-A_3	I	Four address inputs at the A address decoder which select one of the 16 memory words for output through the A port.
B_0-B_3	I	Four address inputs at the B address decoder which select one of the 16 memory words for output through the B port. The B address field also selects the word into which new data is written.
D_0-D_3	I	Four inputs for writing new data into the RAM.
YA_0-YA_3	O	Four three-state A Data Latch outputs which display A port data and also allow several devices to be easily cascaded.
YB_0-YB_3	O	Four three-state B Data Latch outputs which display B port data and also allow several devices to be easily cascaded.
LE	I	The LE input controls the RAM A Data Latch and B Data Latch. When the LE input is HIGH, the latches are open (transparent) and the output data from the RAM is selected by the A and B address fields. When LE is LOW, the latches are closed and they retain the last data read from the RAM independent of changes in the A and B address fields (IDT39C705A/B only).
$\overline{A}_{LO}$	I	This input is used to force the A Data Latch. When $\overline{A}_{LO}$ input is HIGH, the A Latches operate in their normal fashion. Once the A Latches are forced LOW they remain LOW independent of the $\overline{A}_{LO}$ input if the latches are closed (IDT39C705A/B only).
ALE	I	This input controls the A Data Latch. When ALE is HIGH, the latch is open (transparent) and the data from the RAM, as selected by the A address field, is present at the A output. When ALE is LOW, the latch is closed and retains the last data read from the RAM independent of changes in the A address field (IDT39C707/A only).
$\overline{WE}_1$, $\overline{WE}_2$	I	When both Write Enables are LOW, new data can be written into the word selected by the B address fields. If either Write Enable input is HIGH, no new data can be written into the memory.
$\overline{WE}$/BLE	I	This input controls the writing of new data into the RAM and display of data at the B Data Latch output. When $\overline{WE}$/BLE is LOW together with $\overline{WE}_1$ and $\overline{WE}_2$, new data is written into the word selected by the B address fields. When $\overline{WE}$/BLE or any other Write Enable input is HIGH, no data is written into the RAM. When $\overline{WE}$/BLE is HIGH, the B Latch is open (transparent) and, when this input is LOW, the B Data Latch is closed (IDT39C707/A only) .
$\overline{OE}_A$	I	When the A port output enable is LOW, data at the A Data Latch inputs in presented at the YA_I outputs. When $\overline{OE}_A$ is HIGH, the YA_I outputs are in the high-impedance (off) state.
$\overline{OE}_B$	I	When the B port output enable is LOW, data at the B Data Latch inputs is presented at the YB_I outputs. When $\overline{OE}_B$ is HIGH, the YB_I outputs are in the high-impedance (off) state.

IDT39C705A/B FUNCTION TABLES

WRITE CONTROL

$\overline{WE}_1$	$\overline{WE}_2$	FUNCTION	RAM OUTPUTS AT DATA-LATCH INPUTS	
			A-PORT	B-PORT
L	L	Write D into B	A Data (A ≠ B)	Input Data
L	L	Write D into B	Input Data (A = B)	Input Data
X	H	No Write	A-Data	B-Data
H	X	No Write	A-Data	B-Data

H = HIGH
L = LOW
X = Don't Care

YA READ CONTROL

INPUTS			YA OUTPUT	FUNCTION
$\overline{OE}_A$	$\overline{A}_{LO}$	LE		
H	X	X	Z	High Impedance
L	L	X	L	Force YA LOW
L	H	H	A Port RAM Data	Latches Transparent (Open)
L	H	L	NC	Latches Retain Data (Closed)

H = HIGH
L = LOW
X = Don't Care
Z = High Impedance
NC = No Change

YB READ CONTROL

INPUTS		YB OUTPUT	FUNCTION
$\overline{OE}_B$	LE		
H	X	Z	High Impedance
L	H	B Port RAM Data	Latches Transparent (Open)
L	L	NC	Latches Retain Data (Closed)

H = HIGH
L = LOW
X = Don't Care
Z = High Impedance
NC = No Change

IDT39C707/A FUNCTION TABLES

WRITE CONTROL

$\overline{WE}_1$	$\overline{WE}_2$	$\overline{WE}$/BLE	FUNCTION	RAM OUTPUTS AT LATCH INPUTS	
				A PORT	B PORT
L	L	L	Write D into B	A Data (A ≠ B)	Input Data
X	X	H	No Write	A-Data	B-Data
X	H	X	No Write	A-Data	B-Data
H	X	X	No Write	A-Data	B-Data

H = HIGH
L = LOW
X = Don't Care

YA READ CONTROL

INPUTS		YA OUTPUT	FUNCTION
$\overline{OE}_A$	ALE		
H	X	Z	High Impedance
L	H	A Port RAM Data	Latches Transparent (Open)
L	L	NC	Latches Retain Data (Closed)

H = HIGH Z = High Impedance
L = LOW NC = No Change
X = Don't Care

YB READ CONTROL

INPUTS		YB OUTPUT	FUNCTION
$\overline{OE}_B$	$\overline{WE}$/BLE		
H	X	Z	High Impedance
L	H	B Port RAM Data	Latches Transparent (Open)
L	L	NC	Latches Retain Data (Closed)

H = HIGH Z = High Impedance
L = LOW NC = No Change
X = Don't Care

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ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	30	30	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 5%

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER (1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	7	pF

NOTE:
1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS

Following Conditions Apply Unless Otherwise Specified:

T_A = 0°C to +70°C — V_{CC} = 5.0V ± 5% (Commercial)
T_A = -55°C to +125°C — V_{CC} = 5.0V ± 10% (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS [1]			MIN.	TYP.[2]	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level [4]			2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level [4]			–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}			–	0.1	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND			–	-0.1	-5	µA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA		–	V_{CC}	–	V
			I_{OH} = -12mA MIL.		–	4.3	–	
			I_{OH} = -15mA COM'L.		2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA		–	GND	V_{LC}	V
			I_{OL} = 20mA MIL.		–	0.3	0.5	
			I_{OL} = 24mA COM'L.		–	0.3	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max. $\overline{OE}$ = V_{IH}	V_O = 0		–	-0.1	-10	µA
			V_O = Max.		–	0.1	10	
I_{OS}	Output Short Circuit Current	V_{CC} = Min., V_{OUT} = 0V [3]			-15	–	–	mA
I_{CCQH}	Quiescent Power Supply Current $\overline{WE}$ = H	V_{CC} = Max. $V_{HC} \le V_{IH}$, $V_{IL} \le V_{LC}$ f_{WE} = 0, $\overline{WE}$ = H			–	3	5	mA
I_{CCQL}	Quiescent Power Supply Current $\overline{WE}$ = L	V_{CC} = Max. $V_{HC} \le V_{IH}$, $V_{IL} \le V_{LC}$ f_{WE} = 0, $\overline{WE}$ = L			–	3	5	mA
I_{CCT}	Quiescent Input Power Supply Current (per Input @ TTL High) [5]	V_{CC} = Max., V_{IN} = 3.4V, f_{WE} = 0			–	0.3	0.5	mA/ Input
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. $V_{HC} \le V_{IH}$, $V_{IL} \le V_{LC}$ Outputs Open, $\overline{OE}$ = L		MIL.	–	1.7	3.5	mA/ MHz
				COM'L.	–	1.7	2.5	
I_{CC}	Total Power Supply Current [6]	V_{CC} = Max., f_{WE} = 10MHz Outputs Open, $\overline{OE}$ = L $\overline{WE}$ = 50% Duty cycle $V_{HC} \le V_{IH}$, $V_{IL} \le V_{LC}$		MIL.	–	20	40	mA
				COM'L.	–	20	30	
		V_{CC} = Max., f_{WE} = 10MHz Outputs Open, $\overline{OE}$ = L $\overline{WE}$ = 50% Duty cycle V_{IH} = 3.4V, V_{IL} = 0.4V		MIL.	–	25	50	
				COM'L.	–	25	40	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, + 25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. These input levels provide zero noise immunity and should only be static tested in a noise-free environment.
5. I_{CCT} is derived by measuring total current with all the inputs tied together at 3.4V, subtracting out I_{CCQH}, then dividing by the total number of inputs.
6. Total Supply Current is the sum of the quiescent current and the Dynamic current (at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:

$$I_{CC} = I_{CCQH} (WE_H) + I_{CCQL} (1 - WE_H) + I_{CCT} (N_T \times D_H) + I_{CCD} (f_{WE})$$

WE_H = Write duty cycle high period.
D_H = Data duty cycle TTL high period (V_{IN} = 3.4V).
N_T = Number of dynamic inputs driven at TTL levels.
f_{WE} = Write frequency.

CMOS TESTING CONSIDERATIONS

There are certain testing considerations which must be taken into account when testing high-speed CMOS devices in an automatic environment. These are:

1) Proper decoupling at the test head is necessary. Placement of the capacitor set and the value of capacitors used is critical in reducing the potential erroneous failures resulting from large V_{CC} current changes. Capacitor lead length must be short and as close to the DUT power pins as possible.
2) All input pins should be connected to a voltage potential during testing. If left floating, the device may begin to oscillate causing improper device operation and possible latchup.
3) Definition of input levels is very important. Since many inputs may change coincidentally, significant noise at the device pins may cause the V_{IL} and V_{IH} levels not to be met until the noise has settled. To allow for this testing/board induced noise, IDT recommends using $V_{IL} \leq 0V$ and $V_{IH} \geq 3V$ for AC tests.
4) Device grounding is extremely important for proper device testing. The use of multi-layer performance boards with radial decoupling between power and ground planes is required. The ground plane must be sustained from the performance board to the DUT interface board. All unused interconnect pins must be properly connected to the ground pin. Heavy gauge stranded wire should be used for power wiring and twisted pairs are recommended to minimize inductance.

AC ELECTRICAL CHARACTERISTICS

PARAMETERS	FROM	TO	TEST CONDITIONS	IDT39C705A IDT39C707		IDT39C705B IDT39C707A		UNIT
				COM'L.	MIL.	COM'L.	MIL.	
Access Time	A or B Address Stable	YA Stable or YB Stable	LE = HIGH	25	30	20	24	ns
Turn-on Time	$\overline{OE}_A$ or $\overline{OE}_B$ LOW	YA or YB Stable		20	20	16	16	ns
Turn-off Time	$\overline{OE}_A$ or $\overline{OE}_B$ HIGH	YA or YB Off	C_L = 5pF	20	20	16	16	ns
Reset Time	$\overline{A}_{LO}$ LOW	YA LOW		20	20	16	16	ns
Latch Enable Time	LE HIGH	YA and YB Stable		20	22	16	16	ns
Transparency	$\overline{WE}_1$ and $\overline{WE}_2$ LOW	YA or YB	LE = HIGH	30	35	22	24	ns
	D	YA or YB	LE = HIGH	30	35	22	24	ns

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MINIMUM SETUP AND HOLD TIME

PARAMETERS	FROM	TO	TEST CONDITIONS	IDT39C705A IDT39C707		IDT39C705B IDT39C707A		UNIT
				COM'L.	MIL.	COM'L.	MIL.	
Data Set-up Time	D Stable	Either $\overline{WE}$ HIGH		12	15	9	12	ns
Data Hold Time	Either $\overline{WE}$	D Changing		0	0	0	0	ns
Address Set-up Time	B Stable	Both $\overline{WE}$ LOW		6	8	4	6	ns
Address Hold Time	Either $\overline{WE}$ HIGH	B Changing		0	0	0	0	ns
Latch Close Before Write Begins	LE LOW	$\overline{WE}_1$ LOW	$\overline{WE}_2$ LOW	0	0	0	0	ns
	LE LOW	$\overline{WE}_2$ LOW	$\overline{WE}_1$ LOW	0	0	0	0	ns
Address Set-up Before Latch Closes	A or B Stable	LE LOW		12	15	9	12	ns

MINIMUM PULSE WIDTHS

PARAMETERS	INPUT	PULSE	TEST CONDITIONS	IDT39C705A IDT39C707		IDT39C705B IDT39C707A		UNIT
				COM'L.	MIL.	COM'L.	MIL.	
Write Pulse Width	$\overline{WE}_1$	HIGH-LOW-HIGH	$\overline{WE}_2$ LOW	15	15	12	12	ns
	$\overline{WE}_2$	HIGH-LOW-HIGH	$\overline{WE}_1$ LOW	15	15	12	12	ns
A Latch Reset Pulse	$\overline{A}_{LO}$	HIGH-LOW-HIGH		15	15	12	12	ns
Latch Data Capture	LE	LOW-HIGH-LOW		15	18	12	12	ns

NOTE:
The IDT39C705B/707A meet or exceed all the specifications of the IDT39C705A/707.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

TEST	SWITCH
Open Drain Disable Low Enable Low	Closed
All other Outputs	Open

DEFINITIONS

C_L = Load capacitance: includes jig and probe capacitance

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator

TEST LOAD CIRCUITS

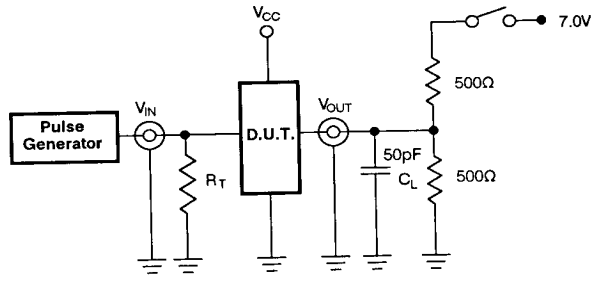

Figure 1. Switching Test Circuit

INPUT/OUTPUT INTERFACE CIRCUIT

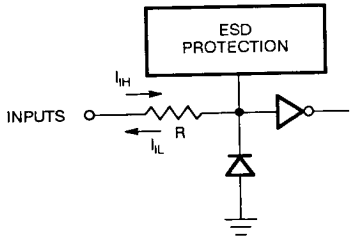

Figure 2. Input Structure

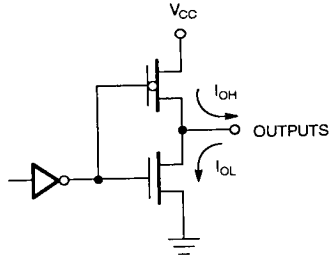

Figure 3. Output Structure

ORDERING INFORMATION