## FEATURES:

- Similar function to AMD's Am2925 bipolar controller with improved speeds and output drive over full temperature and voltage supply extremes
- Four microcode-controlled clock outputs allow clock cycle length control for 15 to 30% increase in system throughput. Microcode selects one of eight clock patterns from 3 to 10 oscillator cycles in length
- System controls for $\overline{RUN}/\overline{HALT}$ and Single Step
  — Switch-debounced inputs provide flexible halt controls
- Low input/output capacitance
  — 6pF inputs (typ.)
  — 8pF outputs (typ.)
- CMOS power levels (1mW typ. static)
- Available in 300 mil 24-pin plastic and ceramic THINDIP, 28-pin LCC and PLCC packages and CERPACK
- Both CMOS and TTL output compatible
- Military product compliant to MIL-STD-883, Class B

## DESCRIPTION:

The IDT49C25/A are single-chip general purpose clock generator/drivers built using IDT's advanced CEMOS™, a dual metal CMOS technology. It has microprogrammable clock cycle length to provide significant speed-up over fixed clock cycle approaches and meets a variety of system speed requirements.

The IDT49C25/A generate four different simultaneous clock out-put waveforms tailored to meet the needs of the IDT3900 CMOS family and other MOS and bipolar microprocessor-based systems. One of eight cycle lengths may be generated under microprogram control using the cycle length inputs, $L_1$, $L_2$ and $L_3$.

A buffered oscillator output, $F_0$, is provided for external system timing in addition to the four microcode controlled clock outputs, $C_1$, $C_2$, $C_3$ and $C_4$.

System control functions include $\overline{RUN}$, $\overline{HALT}$, Single-Step, Initialize and Ready/Wait controls. In addition, the $\overline{FIRST}/\overline{LAST}$ input determines where a halt occurs and the $C_x$ input determines the end point timing of wait cycles. $\overline{WAITACK}$ indicates that the IDT49C25/A are in a wait state.

## FUNCTIONAL BLOCK DIAGRAM
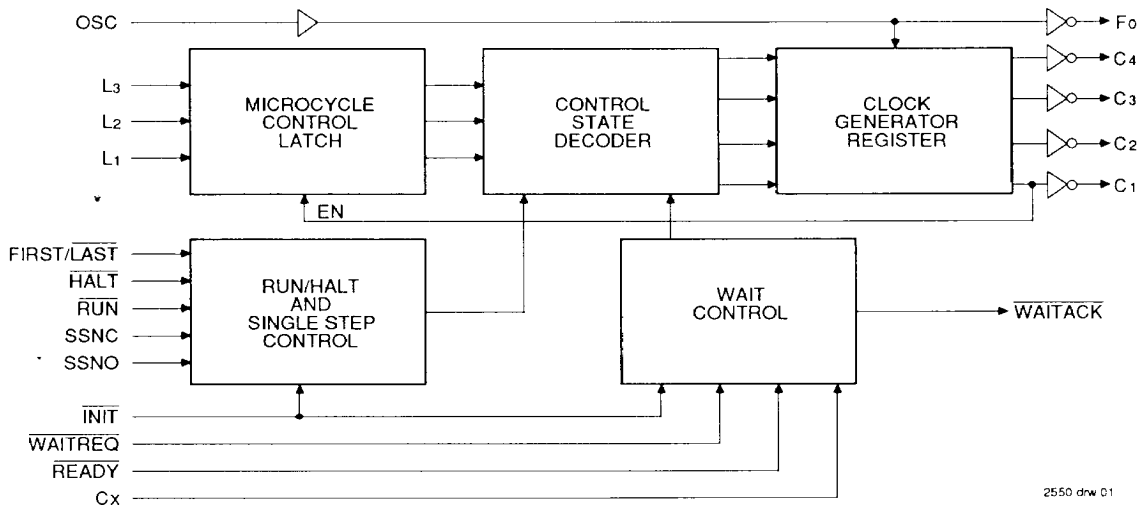


2550 drw 01

CEMOS and MICROSLICE are trademarks of Integrated Device Technology, Inc.

**MILITARY AND COMMERCIAL TEMPERATURE RANGES**

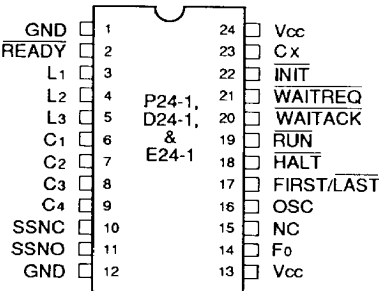DSC-4628/-

1

## PIN CONFIGURATIONS

```
        GND  ┌─1     24─┐  Vcc
      READY  ┌─2     23─┐  Cx
         L1  ┌─3     22─┐  INIT
         L2  ┌─4     21─┐  WAITREQ
         L3  ┌─5  P24-1,  20─┐  WAITACK
         C1  ┌─6  D24-1,  19─┐  RUN
         C2  ┌─7   &    18─┐  HALT
         C3  ┌─8  E24-1  17─┐  FIRST/LAST
         C4  ┌─9     16─┐  OSC
       SSNC  ┌─10    15─┐  NC
       SSNO  ┌─11    14─┐  F0
        GND  ┌─12    13─┐  Vcc
```

**DIP/CERPACK**
**TOP VIEW**

```
                    INDEX
        L2  [ 5              25 ]  NC
        L3  [ 6              24 ]  WAITREQ
        C1  [ 7     J28-1    23 ]  WAITACK
        C2  [ 8     L28-1    22 ]  RUN
        C3  [ 9              21 ]  HALT
        C4  [ 10             20 ]  FIRST/LAST
        NC  [ 11             19 ]  OSC
```

2550 drw 02
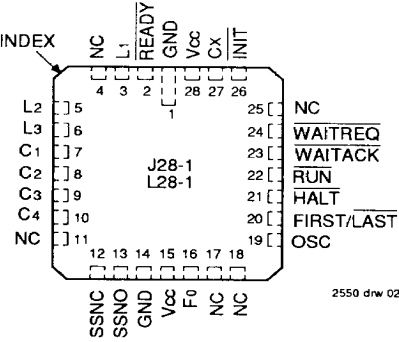
**LCC/PLCC**
**TOP VIEW**

## PIN DESCRIPTIONS

| Pin Names | I/O | Description |
|-----------|-----|-------------|
| C1, C2, C3, C4 | O | System clock outputs. These outputs are all active during every system clock cycle. Their timing is determined by clock cycle length controls: L1, L2 and L3. |
| L1, L2, L3 | I | Clock cycle length control inputs. These inputs receive the microcode bits that select the microcycle lengths. They form a control word which selects one of the eight microcycle waveform patterns $F_3$ through $F_{10}$. |
| F0 | O | The buffered oscillator output. F0 internally generates all of the timing edges for outputs C1, C2, C3, C4 and WAITACK. F0 rises just prior to all of the C1, C2, C3, C4 transitions. |
| HALT and RUN | I | Debounced inputs to provide HALT control. These inputs determine whether the output clocks run or not. A LOW input on HALT (RUN = HIGH) will stop all clock outputs. |
| FIRST/LAST | I | HALT time control input. A HIGH input in conjunction with a HALT command will cause a halt to occur when C4 = LOW and C1 = C2 = C3 = HIGH (see clock waveforms). A LOW input causes a HALT to occur when C1 = C2 = C3 = LOW and C4 = HIGH. |
| SSNO and SSNC | I | Single Step control inputs. These debounced inputs allow system clock cycle single stepping while HALT is activated LOW. |
| WAITREQ | I | The Wait Request active LOW input. When LOW, this input will cause the outputs to halt during the next oscillator cycle after the Cx input goes LOW. |
| Cx | I | Wait cycle control input. The clock outputs respond to a wait request one oscillator clock cycle after Cx goes LOW. Cx is normally tied to any one of C1, C2, C3 or C4. |
| WAITACK | O | The Wait Acknowledge active LOW output. When LOW, this output indicates that all clock outputs are in the "WAIT" state. |
| READY | I | The READY active LOW input is used to continue normal clock output patterns after a wait state. |
| INIT | I | The Initialize active LOW input. This input is intended for use during power-up initialization of the system. When LOW, all clock outputs run free regardless of the state of the Halt, Single Step, Wait Request and Ready inputs. |
| OSC | I | External oscillator input (TTL level input). |

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# LOGIC DIAGRAM
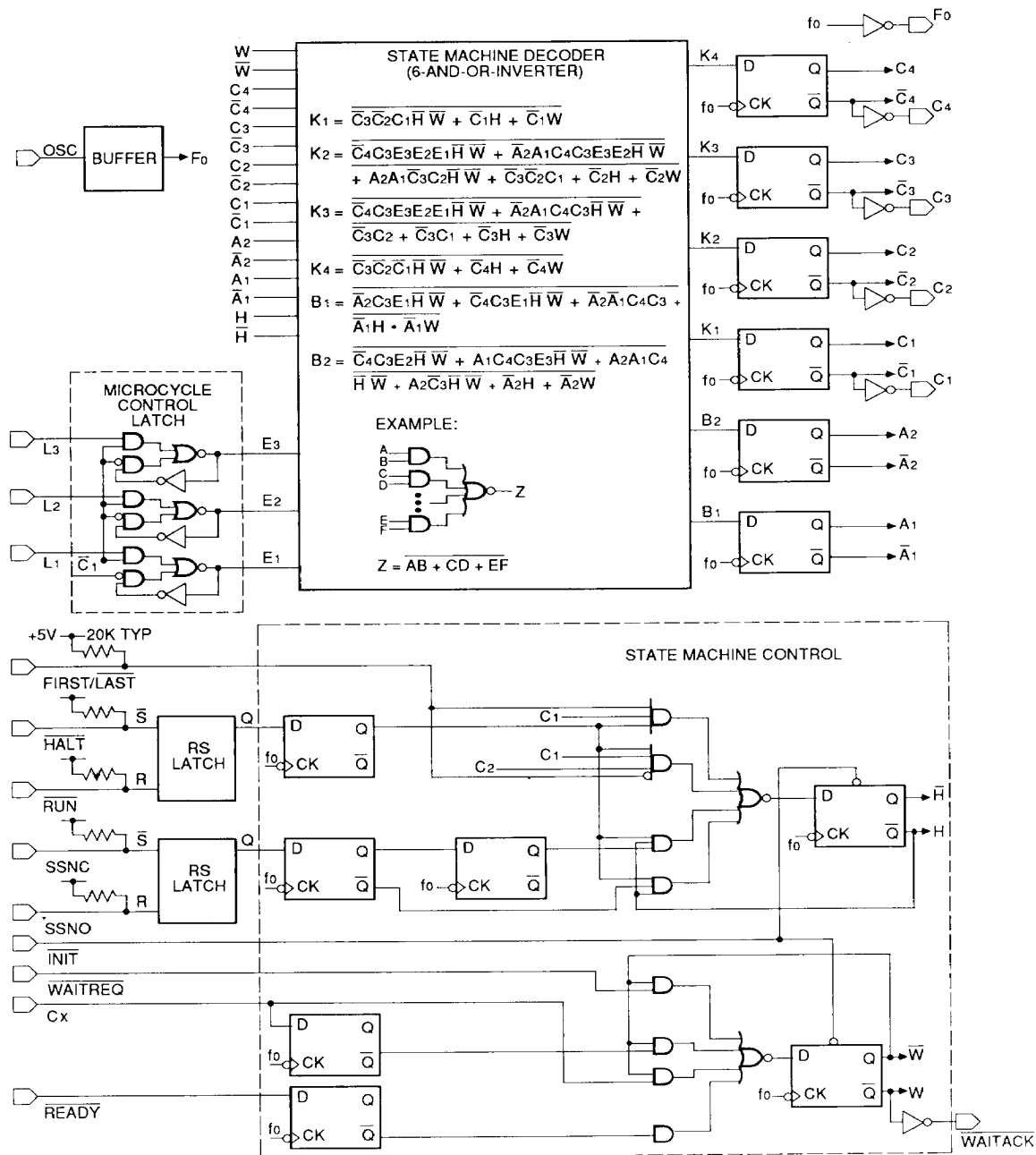
## ABSOLUTE MAXIMUM RATINGS[1]

| Symbol | Rating | Commercial | Military | Unit |
|---|---|---|---|---|
| VTERM[2] | Terminal Voltage with Respect to GND | −0.5 to +7.0 | −0.5 to +7.0 | V |
| VTERM[3] | Terminal Voltage with Respect to GND | −0.5 to Vcc | −0.5 to Vcc | V |
| TA | Operating Temperature | 0 to +70 | −55 to +125 | °C |
| TBIAS | Temperature Under Bias | −55 to +125 | −65 to +135 | °C |
| TSTG | Storage Temperature | −55 to +125 | −65 to +150 | °C |
| PT | Power Dissipation | 0.5 | 0.5 | W |
| IOUT | DC Output Current | 120 | 120 | mA |

NOTES:                                                     2550 tbl 02
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Inputs and Vcc terminals only.
3. Outputs and I/O terminals only.

## CAPACITANCE (TA = +25°C, f = 1.0MHz)

| Symbol | Parameter[1] | Conditions | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| CIN | Input Capacitance | VIN = 0V | 6 | 10 | pF |
| COUT | Output Capacitance | VOUT = 0V | 8 | 12 | pF |

NOTE:                                                      2550 tbl 03
1. This parameter is guaranteed by characterization data and not tested.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: $V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$
Commercial: $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$; Military: $T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$

| Symbol | Parameter | Test Conditions[1] | | Min. | Typ.[2] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| VIH | Input HIGH Level | Guaranteed Logic HIGH Level | | 2.0 | — | — | V |
| VIL | Input LOW Level | Guaranteed Logic LOW Level | | — | — | 0.8 | V |
| IIH | Input HIGH Current | Vcc = Max., VIN = Vcc | | — | — | 25 | µA |
| IIL | Input LOW Current | Vcc = Max. | SSNO, SSNC, RUN, HALT | — | — | -1.0 | mA |
| | | VIN = GND | FIRST/LAST | — | — | -1.5 | |
| | | | Other Inputs | — | — | -5 | µA |
| VIK | Clamp Diode Voltage | Vcc = Min., IN = -18mA | | — | -0.7 | -1.2 | mA |
| ISC | Short Circuit Current | Vcc = Max.[3], Vo = GND | | -60 | -120 | — | mA |
| VOH | Output HIGH Voltage | Vcc = 3V, VIN = VLC or VHC, IOH = -32µA | | VHC | Vcc | — | V |
| | | Vcc = Min. | IOH= -300µA | VHC | Vcc | — | |
| | | VIN = VIH or VIL | IOH = -3.0mA MIL. | 2.4 | 4.0 | — | |
| | | | IOH= -5.0mA COM'L | 2.4 | 4.0 | — | |
| VOL | Output LOW Voltage | Vcc = 3V, VIN = VLC or VHC, IOL = 300µA | | — | GND | VLC | V |
| | | Vcc = Min. | IOL = 300µA | — | GND | VLC[4] | |
| | | VIN = VIH or VIL | IOL = 16mA MIL. | — | — | 0.5 | |
| | | | IOL = 24mA COM'L | — | — | 0.5 | |

NOTES:                                                     2550 tbl 04
1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at VCC = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

6

## POWER SUPPLY CHARACTERISTICS

$V_{LC} = 0.2V$; $V_{HC} = V_{CC} - 0.2V$

| Symbol | Parameter | Test Conditions[1] | | Min. | Typ.[2] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| ICC | Quiescent Power Supply Current | $V_{CC}$ = Max., $V_{IN} \geq V_{HC}$, $V_{IN} \leq V_{LC}$ | | — | 0.2 | 1.5 | mA |
| ΔICC | Quiescent Power Supply Current TTL Inputs HIGH | $V_{CC}$ = Max., $V_{IN}$ = 3.4V[3] | | — | 0.5 | 2.0 | mA |
| ICCD | Dynamic Power Supply Current[4] | $V_{CC}$ = Max. Outputs Open | $V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ | — | 0.24 | 0.4 | mA/ MHz |
| IC | Total Power Supply Current[5] | $V_{CC}$ = Max., Outputs Open, $f_{CP}$ = OSC = 5MHz (50% duty cycle) READY, SSNO, WAITREQ, HALT, INIT = $V_{CC}$ L1, L2, L3, SSNC, FIRST/LAST, RUN, Cx = GND | | — | 6.5 | 9.7 | mA |
| | | $V_{CC}$ = Max. Outputs Open $f_{CP}$ = OSC = 5MHz (50% duty cycle) SSNO, HALT = $V_{CC}$ READY, WAITREQ, INIT = 3.4V (98% duty cycle) L1, L2, L3, SSNC, FIRST/LAST, RUN, Cx = GND | | — | 8.5 | 16.6 | |

2550 tbl 05

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC}$ = 5.0V, +25°C ambient.
3. Per TTL driven input ($V_{IN}$ = 3.4V); all other inputs at $V_{CC}$ or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_O N_O)$
   $I_{CC}$ = Quiescent Current
   $\Delta I_{CC}$ = Power Supply Current for a TTL High Input ($V_{IN}$ = 3.4V)
   $D_H$ = Duty Cycle for TTL Inputs High
   $N_T$ = Number of TTL Inputs at DH
   $I_{CCD}$ = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   $f_{CP}$ = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   $f_O$ = Output Frequency
   $N_O$ = Number of Outputs at fo
   All currents are in milliamps and all frequencies are in megahertz.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

| | Symbol | Parameter | Condition | IDT49C25 Com'l. Min. | Com'l. Max. | Mil. Min. | Mil. Max. | IDT49C25A Com'l. Min. | Com'l. Max. | Mil. Min. | Mil. Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | $f_{MAX1}$ | Fo Frequency (Cx Connected)[1,6] | $C_L = 50pF$ $R_L = 500\Omega$ | 31 | — | 31 | — | 40 | — | 40 | — | MHz |
| 2 | $f_{MAX2}$ | Fo Frequency (Cx = HIGH)[6] | | — | — | — | — | — | — | — | — | MHz |
| 3 | $t_{OFFSET}$ | Fo (⌐) to C1, C2, C3, C4 or WAITACK (⌐) | | — | 8.5 | — | 8.5 | — | 6.0 | — | 6.0 | ns |
| 4 | $t_{OFFSET}$ | Fo (⌐) to C1, C2, C3, C4 or WAITACK (⌐) | | — | 17 | — | 18 | — | 11.5 | — | 12 | ns |
| 5 | $t_{SKEW}$ | C1 (⌐) to C2 (⌐) | | — | 2 | — | 2 | — | 1.5 | — | 1.5 | ns |
| 6 | $t_{SKEW}$ | C1 (⌐) to C3 (⌐) | | — | 2 | — | 2 | — | 1.5 | — | 1.5 | ns |
| 7 | $t_{SKEW}$ | C1 (⌐) to C4 (⌐) Opposite Transition | | — | 11 | — | 11 | — | 8.0 | — | 8.0 | ns |
| 8 | $t_{SU}$ | L1, L2, L3, to C1 (⌐) | | 6 | — | 6 | — | 5 | — | 5 | — | ns |
| 9 | $t_H$ | L1, L2, L3, to C1 (⌐) | | 8 | — | 8 | — | 6 | — | 6 | — | ns |
| 10 | $t_{SU}$ | Cx to Fo (⌐)[2] | | 18 | — | 18 | — | 12 | — | 12 | — | ns |
| 11 | $t_H$ | Cx to Fo (⌐)[2] | | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| 12 | $t_{SU}$ | WAITREQ to Fo (⌐)[3] | | 18 | — | 18 | — | 12 | — | 12 | — | ns |
| 13 | $t_H$ | WAITREQ to Fo (⌐)[3] | | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| 14 | $t_{SU}$ | READY to Fo (⌐)[3] | | 18 | — | 18 | — | 12 | — | 12 | — | ns |
| 15 | $t_H$ | READY to Fo (⌐)[3] | | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| 16 | $t_{SU}$ | RUN, HALT (⌐) to Fo (⌐)[3,4] | | 18 | — | 18 | — | 12 | — | 12 | — | ns |
| 17 | $t_{SU}$ | SSNC, SSNO to Fo (⌐)[3,4] | | 18 | — | 18 | — | 12 | — | 12 | — | ns |
| 18 | $t_{SU}$ | FIRST/LAST to Fo (⌐)[5] | | 18 | — | 18 | — | 12 | — | 12 | — | ns |
| 19 | $t_{SU}$ | INIT (⌐) to Fo (⌐)[3] | | 18 | — | 18 | — | 12 | — | 12 | — | ns |
| 20 | $t_W$ | INIT LOW Pulse Width | | 20 | — | 25 | — | 18 | — | 23 | — | ns |
| 21 | $t_{PLH}$ | INIT to WAITACK | | — | 25 | — | 27 | — | 16 | — | 18 | ns |
| 22 | $t_{PLH}$ | OSC to Fo | | — | 13 | — | 16 | — | 8.5 | — | 10.5 | ns |
| 23 | $t_{PHL}$ | | | — | 13 | — | 16 | — | 8.5 | — | 10.5 | ns |

2550 tbl 06

NOTES:
1. The frequency guarantees apply with Cx connected to C1, C2, C3, C4 or HIGH. The Cx input load must be considered part of the 50pf/500Ω clock output loading.
2. These set-up and hold times apply to the Fo LOW-to-HIGH transition of the period in which Cx goes LOW.
3. These inputs are synchronized internally. Failure to meet ts may cause a 1/Fo delay but will not cause incorrect operation.
4. These inputs are "debounced" by an internal R-S flip-flop and are intended to be connected to manual break-before-make switches.
5. FIRST/LAST normally wired HIGH or LOW.
6. This parameter is guaranteed but not tested.
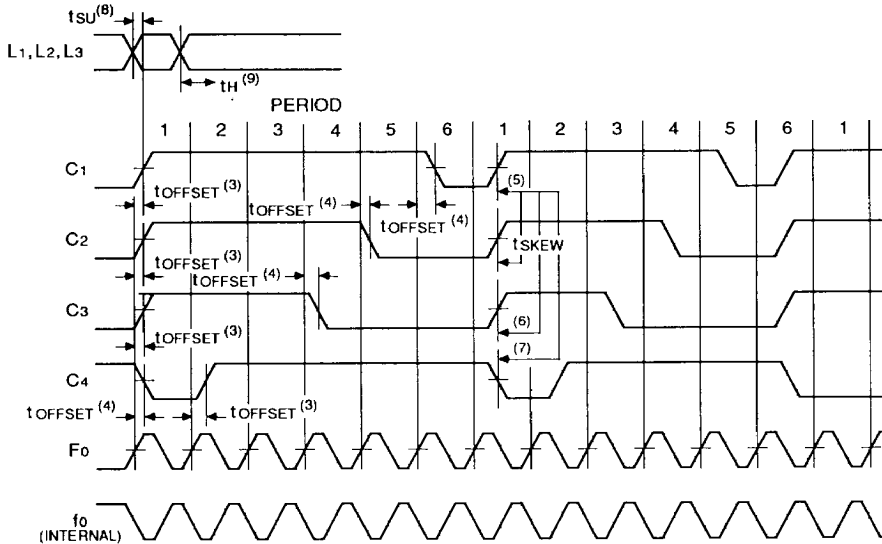
6

## SWITCHING WAVEFORMS



Figure 2.  Normal Cycle Without Wait States (Pattern F6 Shown)
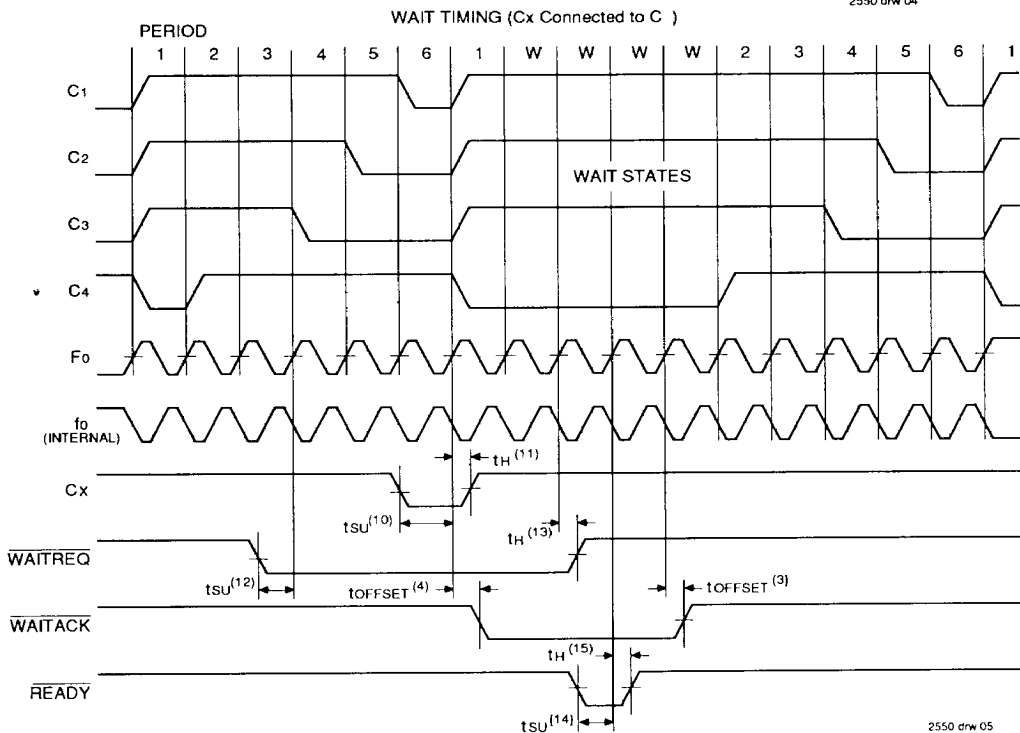
2550 drw 04



Figure 3.  Wait Timing (CX Connected to C1)

2550 drw 05

## DETAILED DESCRIPTION

The IDT49C25/A are dynamically programmable general-purpose clock controllers. They can be logically separated into two parts — a state machine decoder and a state machine control section.

The state machine takes microcode information from the Microcycle Length (L) inputs $L_1$, $L_2$ and $L_3$ and counts the fundamental frequency of the oscillator (OSC) to create the clock outputs $F_0$, $C_1$, $C_2$, $C_3$ and $C_4$.

The clock outputs have a characteristic wave shape
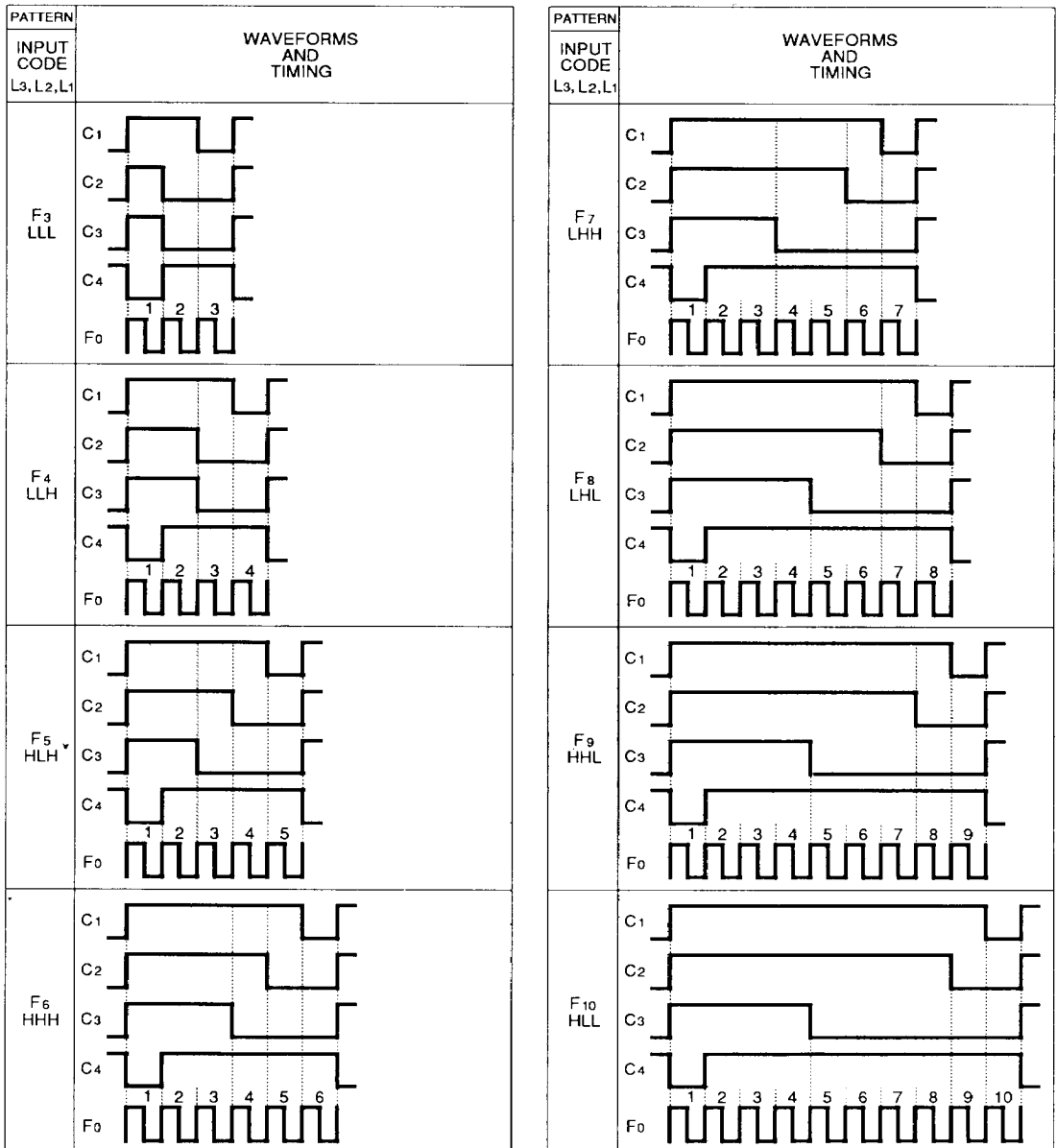


Figure 4. IDT49C25/A Clock Waveforms

6

relationship for each microcycle length. For example, $C_1$ is always LOW only on the last $F_0$ clock period of a microcycle and $C_4$ is always LOW on the first. $C_3$ has an approximate duty cycle of 50% and $C_2$ is HIGH for all but the last two periods (see Figure 4).

The current state of the machine is contained in a register, part of which is the Clock Generator Register. $C_1$, $C_2$, $C_3$ and $C_4$ are the outputs of this register. These outputs and the outputs of the Microcycle Control Latch are fed into combinatorial logic to generate the next state. On each falling edge of the internal clock, the next state is entered into the current state register. The Microcycle Control Latch is latched when $C_1$ is HIGH. This means that it will be loaded during the last state of each microcycle ($C_1 = C_2 = C_3 = $ LOW, $C_4 = $ HIGH). This internal latch selects one of eight possible microcycle lengths, $F_3$ to $F_{10}$.

The state machine control logic, which determines the mode of operation of the state machine, is intended to be connected to a front panel. There are four basic modes of operation of the IDT49C25/A comprised of RUN, HALT, WAIT and SINGLE STEP.

## SYSTEM TIMING

In the typical computer, the time required to execute different instructions varies. However, the time allotted to each instruction is the time that it takes to execute the longest instruction. The IDT49C25/A allows the user to dynamically vary the time allotted for each instruction, thereby allowing the user to realize a higher throughput.

## IDT49C25/A CONTROL INPUTS

The control inputs fall into two categories, microcycle length control and clock control. Microcycle length control is provided via the "L" inputs which are intended to be connected to the microprogram memory. The "L" inputs are used to select one of eight cycle lengths ranging from three oscillator cycles for pattern $F_3$ to ten oscillator cycles for pattern $F_{10}$. This information is always loaded at the end of the microcycle into the Microcycle Control Latch which performs the function of a pipeline register for the microcycle length microcode bits.
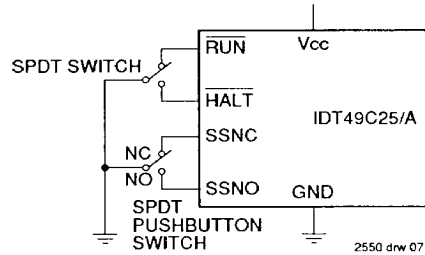


Figure 5. Switch Connection for RUN/HALT and Single Step

Therefore, the cycle length goes in the same microword as the instruction that it is associated with.

The clock control inputs are used to synchronize the microprogram machine with the external world and I/O devices. Inputs like RUN, HALT, SSNO and SSNC, which start and stop execution, are meant to be connected to switches on the front panel of the microprogrammed machine (see Figure 5). These inputs have internal pull-up resistors and are connected to an R-S flip-flop in order to provide switch debouncing. The FIRST/LAST input is used to determine at what point of the microcycle the IDT49C25/A will halt when HALT or a SINGLE STEP is initiated. In most applications, the user wires this input HIGH or LOW, depending on the design.

When HALT is held low (RUN = HIGH), the state machine will start the halt mode on the last ($C_1 = $ LOW) or the first ($C_4 = $ LOW) state of the microcycle as determined by the FIRST/LAST input. When RUN goes low (HALT = HIGH), the state machine will resume the run mode.

The WAITREQ, Cx, READY and WAITACK signals are used to synchronize other parts of a computer system (memory, I/O devices) to the CPU by dynamically stretching the microcycle. For example, the CPU may access a slow peripheral that requires the data remain on the date bus for several microseconds. In this case, the peripheral pulls the WAITREQ line LOW. The Cx input lets the design specify when the WAITREQ line is sampled in the microcycle. This has a direct impact on how much time the peripheral has to
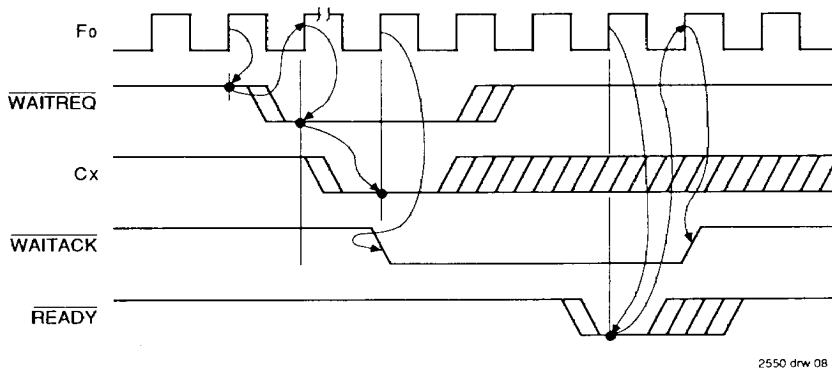


Figure 6. WAIT/READY Timing

respond in order to request a wait cycle (see Figure 6). The READY line is used by the peripheral to signal when it is ready to resume execution of the rest of the microcycle. The WAITACK line goes LOW on the next oscillator cycle after the Cx input goes LOW and remains LOW until the second oscillator cycle after READY goes LOW.

The SSNO and SSNC inputs are used to initiate the SINGLE STEP mode. These debounced inputs allow a single microcycle to occur while in the halt mode. SSNO (normally open) and SSNC (normally closed) are intended to be connected to a momentary SPDT switch. After SSNO has been high for one clock edge, the state machine will change to the next run mode. The microcycle will end on the first or last state of the microcycle, depending on the state of the FIRST/LAST.

## AC TIMING SIGNAL REFERENCES

Set-up and hold times in registers and latches are measured relative to the clock signals that drive them. In the IDT49C25/A, the external oscillator provides a free running clock signal that drives all the registers on the devices. This clock is provided for the user through the buffered output of $F_0$. Therefore, $F_0$ is used as the reference of set-up, hold and clock-to-output times. However, for the Microcycle Control Latch, the set-up and hold times are referenced to the $C_1$ output which is the buffered version of the latch enable. This reference is appropriate for the Microcycle Control Latch because, in a typical application, this latch is considered part of the pipeline register which is also driven by one of the "C" outputs.
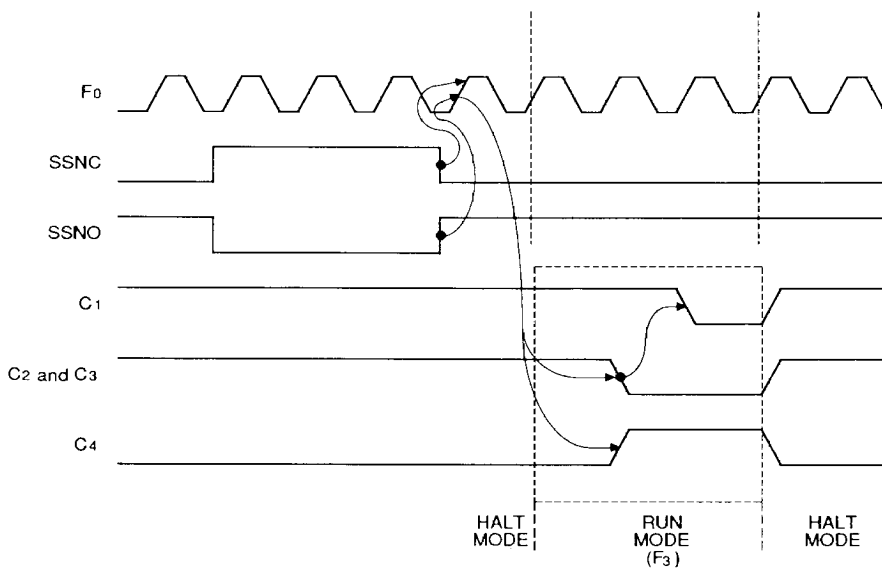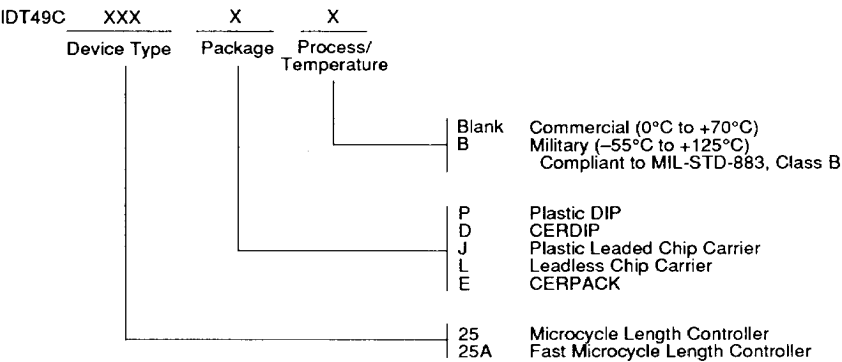


Figure 7. Single Step Timing Sequence

## ORDERING INFORMATION

```
IDT49C    XXX        X        X
        Device Type  Package  Process/
                              Temperature
```

| | |
|---|---|
| Blank | Commercial (0°C to +70°C) |
| B | Military (−55°C to +125°C) |
| | Compliant to MIL-STD-883, Class B |
| | |
| P | Plastic DIP |
| D | CERDIP |
| J | Plastic Leaded Chip Carrier |
| L | Leadless Chip Carrier |
| E | CERPACK |
| | |
| 25 | Microcycle Length Controller |
| 25A | Fast Microcycle Length Controller |

2550 drw 10