Integrated Device Technology, Inc.

# 16-BIT CMOS MICROPROCESSOR SLICE

**IDT49C402**
**IDT49C402A**
**IDT49C402B**

## FEATURES:

- Functionally equivalent to four 2901s and one 2902
- IDT49C402B is 60% faster than four 2901Cs and one 2902A
- Expanded two-address architecture with independent, simultaneous access to two 64 x 16 register files
- Expanded destination functions with 8 new operations allowing Direct Data to be loaded directly into the dual-port RAM and Q Register
- Fully cascadable
- 84-pin PGA, 80-pin PQFP and 68-pin 25 MIL Center Flatpack
- Military product compliant to MIL-STD-883, Class B

## DESCRIPTION:

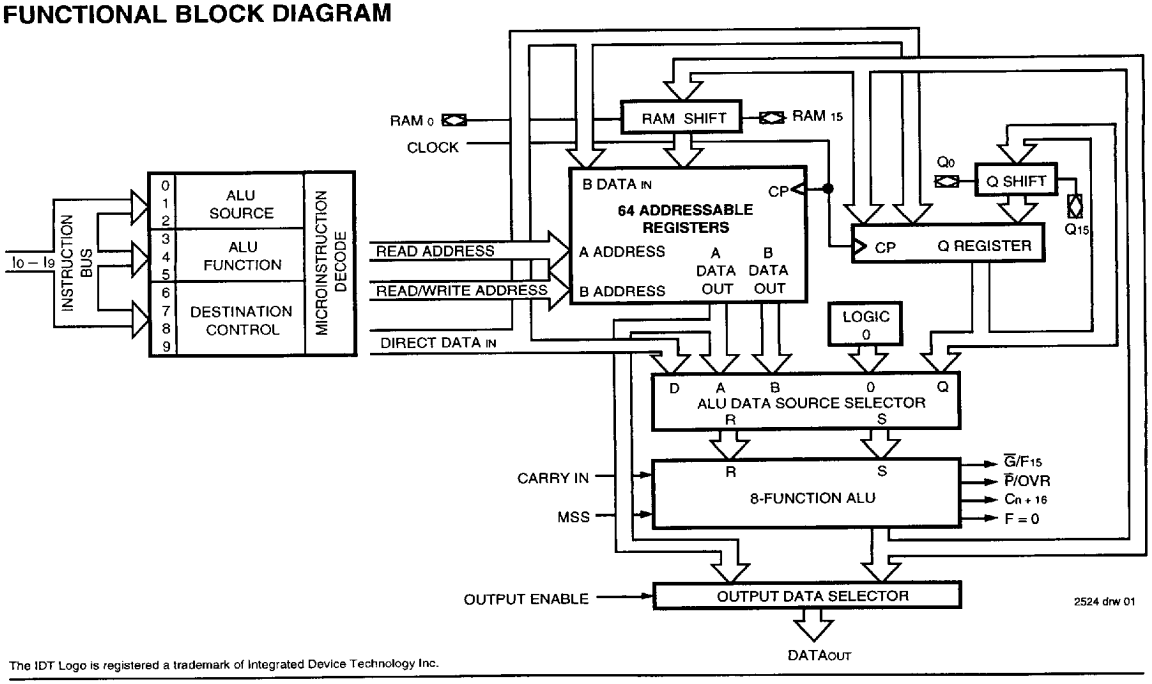
The IDT49C402s are high-speed, fully cascadable 16-bit CMOS microprocessor slice units which combine the standard functions of four 2901s and a 2902 with additional control features aimed at enhancing the performance of bit-slice microprocessor designs.

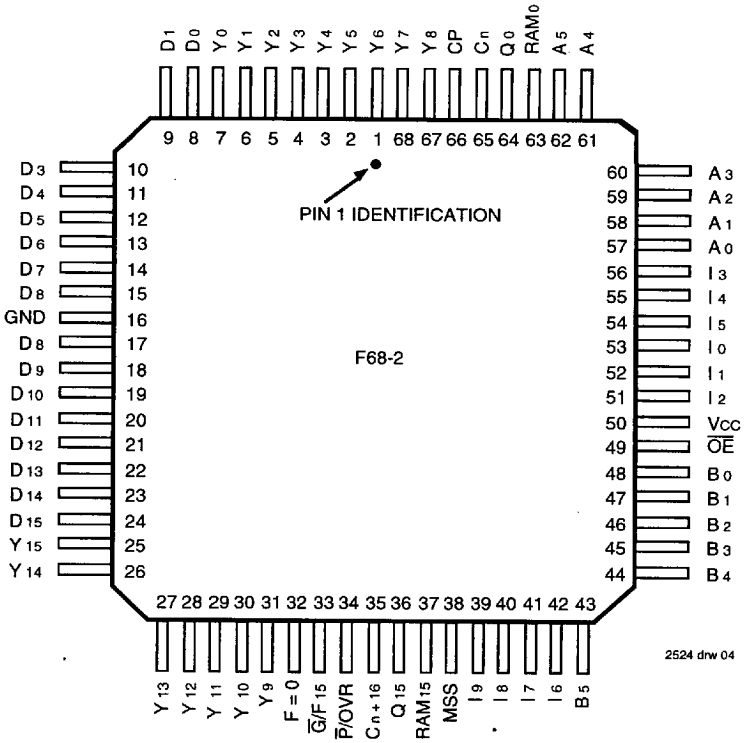
The IDT49C402s include all of the normal functions associated with standard 2901 bit-slice operation: a) a 3-bit instruction field ($I_0$, $I_1$, $I_2$) which controls the source operand selection for the ALU; b) a 3-bit microinstruction field ($I_3$,$I_4$, $I_5$) used to control the eight possible functions of the ALU; c) eight destination control functions which are selected by the microcode inputs ($I_6$, $I_7$, $I_8$); and d) a tenth microinstruction input, $I_9$, offering eight additional destination control functions. This $I_9$ input, in conjunction with $I_6$, $I_7$ and $I_8$, allows for shifting the Q Register up and down, loading the RAM or Q Register directly from the D inputs without going through the ALU, and having the RAM A data output port available at the Y output pins of the device.

Also featured is an on-chip dual-port RAM that contains 64-words-by-16 bits – four times the number of working registers in a 2901.

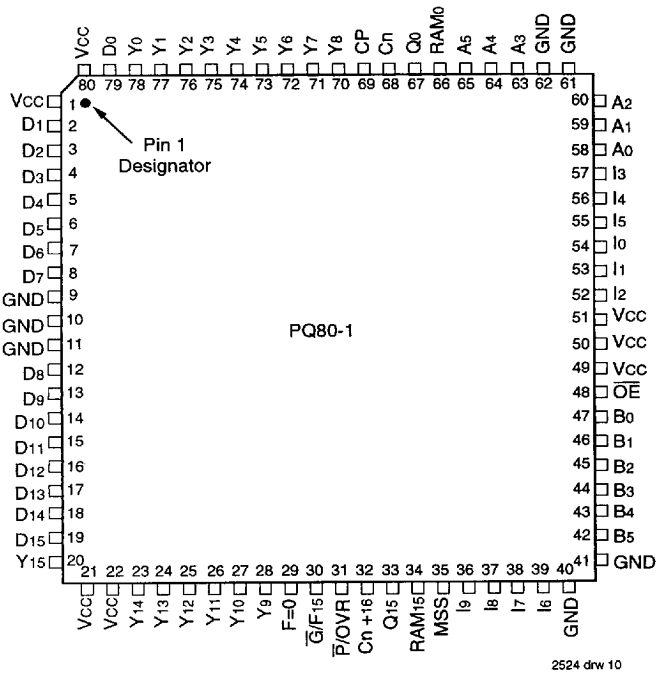
The IDT49C402s are fabricated using CMOS technology designed for high performance and high reliability. These performance-enhanced devices feature both bipolar speed and bipolar output drive capabilities, while maintaining exceptional microinstruction speeds at greatly reduced CMOS power levels.

## FUNCTIONAL BLOCK DIAGRAM






**FINE PITCH FLATPACK**
**TOP VIEW**




**PQFP**
**TOP VIEW**

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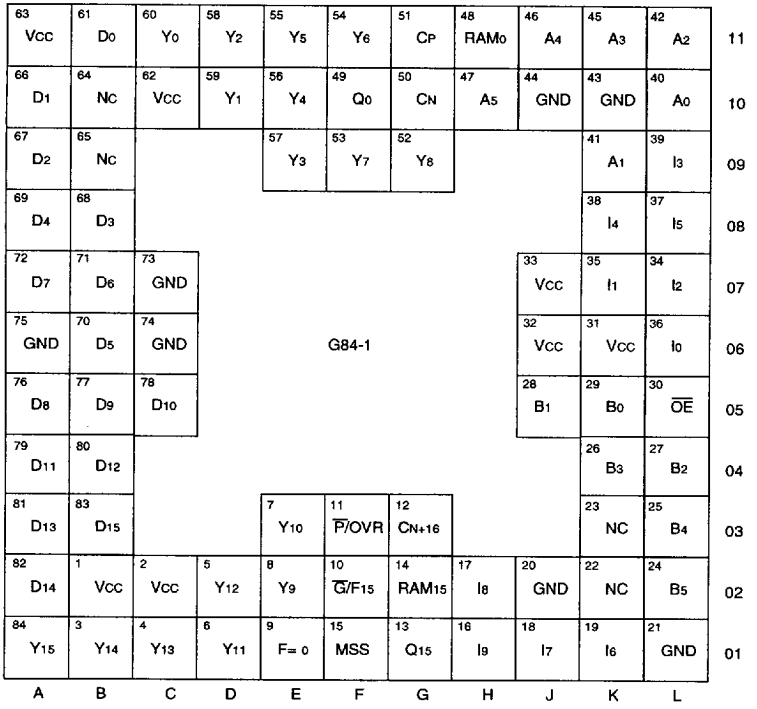


**PGA**
**TOP VIEW**

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## PIN DESCRIPTIONS

| Pin Name | I/O | Description |
|---|---|---|
| $A_0$ - $A_5$ | I | Six address inputs to the register file which selects one register and displays its contents through the A port. |
| $B_0$ - $B_5$ | I | Six address inputs to the register file which selects one of the registers in the file, the contents of which is displayed through the B port. It also selects the location into which new data can be written when the clock goes LOW. |
| $I_0$ - $I_9$ | I | Ten instruction control lines which determine what data source will be applied to the ALU $I_{(0, 1, 2)}$, what function the ALU will perform $I_{(3, 4, 5)}$ and what data is deposited in the Q Register or the register file $I_{(6, 7, 8, 9)}$. Original 2901 destinations are selected if $I_9$ is disconnected in this mode, proper $I_9$ bias is achieved by an external pullup resistor to $V_{CC}$ (47K ohms recommended). |
| $D_0$ - $D_{15}$ | I | Sixteen-bit direct data inputs which are the data source for entering external data into the device ALU, Q Register or RAM. $D_0$ is the LSB. |
| $Y_0$ - $Y_{15}$ | O | Sixteen three-state output lines which, when enabled, display either the sixteen outputs of the ALU or the data on the A port of the register stack. This is determined by the destination code $I_{(6, 7, 8, 9)}$. |
| $\overline{G}/F_{15}$ | O | A multipurpose pin which indicates the carry generate ($\overline{G}$) function at the least significant and intermediate slices or as $F_{15}$, the most significant ALU output (sign bit). $\overline{G}/F_{15}$ selection is controlled by the MSS pin. If MSS = HIGH, $F_{15}$ is enabled. If MSS = LOW, $\overline{G}$ is enabled. |
| F = 0 | O | Open drain output which goes HIGH if the $F_0$ - $F_{15}$ ALU outputs are all LOW. This indicates that the result of an ALU operation is zero (positive logic). |
| $C_n$ | I | Carry-in to the internal ALU. |
| $C_{n+16}$ | O | Carry-out of the ALU. |
| $Q_{15}$ $RAM_{15}$ | I/O | Bidirectional lines controlled by $I_{(6, 7, 8, 9)}$. Both are three-state output drivers connected to the TTL-compatible inputs. When the destination code on $I_{(6, 7, 8, 9)}$ indicates an up shift, the three-state outputs are enabled, the MSB of the Q Register is available on the $Q_{15}$ pin and the MSB of the ALU output is available on the $RAM_{15}$ pin. When the destination code indicates a down shift, the pins are the data inputs to the MSB of the Q Register and the MSB of the RAM. |
| $Q_0$ $RAM_0$ | I/O | Both bidirectional lines function identically to $Q_{15}$ and $RAM_{15}$ lines except they are the LSB of the Q Register and RAM. |
| $\overline{OE}$ | I | Output enable. When pulled HIGH, the Y outputs are OFF (high impedance). When pulled LOW, the Y outputs are enabled. |
| $\overline{P}$/OVR | O | A multipurpose pin which indicates the carry propagate ($\overline{P}$) output for performing a carry lookahead operation or overflow (OVR) the Exclusive-OR of the carry-in and carry-out of the ALU MSB. OVR, at the most significant end of the word, indicates that the result of an arithmetic two's complement operation has overflowed into the sign bit. $\overline{P}$/OVR selection is controlled by the MSS pin. If MSS = HIGH, OVR is enabled. If MSS = LOW, $\overline{P}$ is enabled. |
| CP | I | The clock input LOW-to-HIGH clock transitions will change the Q Register and the register file outputs. Clock LOW time is internally the write enable time for the 64 x 16 RAM. While the clock is LOW, the slave latches on the RAM outputs are closed, storing the data previously on the RAM outputs. Synchronous MASTER-SLAVE operation of the register file is achieved by this. |
| MSS | I | When HIGH, enables OVR and $F_{15}$ on the $\overline{P}$/OVR and $\overline{G}/F_{15}$ pins. When LOW, enables $\overline{G}$ and $\overline{P}$ on these pins. If left open, internal pullup resistor to $V_{CC}$ provides declaration that the device is the most significant slice. |

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## DEVICE ARCHITECTURE

The IDT49C402 CMOS bit-slice microprocessor is configured sixteen bits wide and is cascadable to any number of bits (16, 32, 48, 64). Key elements which make up this 16-bit microprocessor slice are the 1) register file (64 x 16 dual-port RAM) with shifter 2) ALU and 3) Q Register and shifter.

**REGISTER FILE** — A 16-bit data word from one of the 64 RAM registers can read from the A port as selected by the 6-bit A address field. Simultaneously, the same data word, or any other word from the 64 RAM registers, can be read from the B port as selected by the 6-bit B address field. New data is written into the RAM register location selected by the B address field during the clock (CP) LOW time. Two sixteen-bit latches hold the RAM A port and B port during the clock (CP) LOW time, eliminating any data races. During clock HIGH, these latches are transparent, reading the data selected by the A and B addresses. The RAM data input field is driven from a four-input multiplexer that selects the ALU output or the D inputs. The ALU output can be shifted up one position, down one position or not shifted. Shifting data operations involves the $RAM_{15}$ and $RAM_0$ I/O pins. For a shift up operation, the RAM shifter MSB is connected to an enabled $RAM_{15}$ I/O output, while the $RAM_0$ I/O input is selected as the input to the LSB. During a shift down operation, the RAM shifter LSB is connected to an enabled $RAM_0$ I/O output, while the $RAM_{15}$ I/O input is selected as the input to the MSB.

**ALU** — The ALU can perform three binary arithmetic and five logic operations on the two 16-bit input words S and R. The S input field is driven from a 3-input multiplexer and the R input field is driven from a 2-input multiplexer, with both having a zero source operand. Both multiplexers are controlled by the $I_{(0, 1, 2)}$ inputs. This multiplexer configuration enables the user to select the various pairs of the A, B, D, Q and "0" inputs as source operands to the ALU. Microinstruction inputs $I_{(3, 4, 5)}$ are used to select the ALU function. This high-speed ALU cascades to any word length, providing carry-in ($C_n$), carry-out ($C_{n+16}$) and an open-drain (F = 0) output. When all bits of the ALU are zero, the pull-down device of F = 0 is off, allowing a wire-OR of this pin over all cascaded devices. Multipurpose pins $\overline{G}/F_{15}$ and $\overline{P}$/OVR are aimed at accelerating arithmetic operations. For intermediate and least significant slices, the MSS pin is programmed LOW, selecting the carry-generate ($\overline{G}$) and carry propagate ($\overline{P}$) output functions to be used by carry lookahead logic. For the most significant slice, MSS is programmed HIGH, selecting the sign-bit ($F_{15}$) and the two's complement overflow (OVR) output functions. The sign bit ($F_{15}$) allows the ALU sign bit to be monitored without enabling the three-state ALU outputs. The overflow (OVR) output is high when the two's complement arithmetic operation has overflowed into the sign bit, as logically determined from the Exclusive-OR of the carry-in and carry-out of the most significant bit of the ALU. The ALU data outputs are available at the three-state outputs $Y_{(0\text{-}15)}$ or as inputs to the RAM register file and Q register under control of the $I_{(6, 7, 8, 9)}$ instruction inputs.

**Q REGISTER** — The Q Register is a separate 16-bit file intended for multiplication and division routines and can also be used as an accumulator or holding register for other types of applications. It is driven from a 4-input multiplexer. In the no-shift mode, the multiplexer enters the ALU F output or Direct Data into the Q Register. In either the shift up or shift down mode, the multiplexer selects the Q Register data appropriately shifted up or down. The Q shifter has two ports, $Q_0$ and $Q_{15}$, which operate comparably to the RAM shifter. They are controlled by the $I_{(6, 7, 8, 9)}$ inputs.

The clock input of the IDT49C402 controls the RAM, Q Register and A and B data latches. When enabled, the data is clocked into the Q Register on the LOW- to-HIGH transition. When the clock is HIGH, the A and B latches are open and pass data that is present at the RAM outputs. When the clock is LOW, the latches are closed and retain the last data entered. When the clock is LOW and $I_{(6, 7, 8, 9)}$ define the RAM as the destination, new data will be written into the RAM file defined by the B address field.

## ALU SOURCE OPERAND CONTROL

| Mnemonic | Microcode | | | | ALU Source Operands | |
|---|---|---|---|---|---|---|
| | $I_2$ | $I_1$ | $I_0$ | Octal Code | R | S |
| AQ | L | L | L | 0 | A | Q |
| AB | L | L | H | 1 | A | B |
| ZQ | L | H | L | 2 | 0 | Q |
| ZB | L | H | H | 3 | 0 | B |
| ZA | H | L | L | 4 | 0 | A |
| DA | H | L | H | 5 | D | A |
| DQ | H | H | L | 6 | D | Q |
| DZ | H | H | H | 7 | D | 0 |

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## ALU FUNCTION CONTROL

| Mnemonic | Microcode | | | | ALU Function | Symbol |
|---|---|---|---|---|---|---|
| | $I_2$ | $I_1$ | $I_0$ | Octal Code | | |
| ADD | L | L | L | 0 | R Plus S | R + S |
| SUBR | L | L | H | 1 | S Minus R | S – R |
| SUBS | L | H | L | 2 | R Minus S | R – S |
| OR | L | H | H | 3 | R OR S | R ∨ S |
| AND | H | L | L | 4 | R AND S | R ∧ S |
| NOTRS | H | L | H | 5 | $\overline{R}$ AND S | $\overline{R}$ ∧ S |
| EXOR | H | H | L | 6 | R EX-OR S | R ∇ S |
| EXNOR | H | H | H | 7 | R EX-NOR S | $\overline{R \nabla S}$ |

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## ALU ARITHMETIC MODE FUNCTIONS

| Octal | | $C_n$ = L | | $C_n$ = H | |
|---|---|---|---|---|---|
| $I_{5,4,3}$ | $I_{2,1,0}$ | Group | Function | Group | Function |
| 0 | 0 | ADD | A + Q | ADD plus one | A + Q + 1 |
| 0 | 1 | | A + B | | A + B + 1 |
| 0 | 5 | | D + A | | D + A + 1 |
| 0 | 6 | | D + Q | | D + Q + 1 |
| 0 | 2 | PASS | Q | Increment | Q + 1 |
| 0 | 3 | | B | | B + 1 |
| 0 | 4 | | A | | A + 1 |
| 0 | 7 | | D | | D + 1 |
| 1 | 2 | Decrement | Q – 1 | PASS | Q |
| 1 | 3 | | B – 1 | | B |
| 1 | 4 | | A – 1 | | A |
| 2 | 7 | | D – 1 | | D |
| 2 | 2 | 1's Comp. | –Q – 1 | 2's Comp. (Negate) | –Q |
| 2 | 3 | | –B – 1 | | –B |
| 2 | 4 | | –A – 1 | | –A |
| 1 | 7 | | –D – 1 | | –D |
| 1 | 0 | Subtract (1's Comp) | Q – A – 1 | Subtract (2's Comp) | Q – A |
| 1 | 1 | | B – A – 1 | | B – A |
| 1 | 5 | | A – D – 1 | | A – D |
| 1 | 6 | | Q – D – 1 | | Q – D |
| 2 | 0 | | A – Q – 1 | | A – Q |
| 2 | 1 | | A – B – 1 | | A – B |
| 2 | 5 | | D – A – 1 | | D – A |
| 2 | 6 | | D – Q – 1 | | D – Q |

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## ALU LOGIC MODE FUNCTIONS

| Octal | | Group | Function |
|---|---|---|---|
| $I_{5,4,3}$ | $I_{2,1,0}$ | | |
| 4 | 0 | AND | A ∧ Q |
| 4 | 1 | | A ∧ B |
| 4 | 5 | | D ∧ A |
| 4 | 6 | | D ∧ Q |
| 3 | 0 | OR | A ∨ Q |
| 3 | 1 | | A ∨ B |
| 3 | 5 | | D ∨ A |
| 3 | 6 | | D ∨ Q |
| 6 | 0 | EX–OR | A ∇ Q |
| 6 | 1 | | A ∇ B |
| 6 | 5 | | D ∇ A |
| 6 | 6 | | D ∇ Q |
| 7 | 0 | EX–NOR | $\overline{A \nabla Q}$ |
| 7 | 1 | | $\overline{A \nabla B}$ |
| 7 | 5 | | $\overline{D \nabla A}$ |
| 7 | 6 | | $\overline{D \nabla Q}$ |
| 7 | 2 | INVERT | $\overline{Q}$ |
| 7 | 3 | | $\overline{B}$ |
| 7 | 4 | | $\overline{A}$ |
| 7 | 7 | | $\overline{D}$ |
| 6 | 2 | PASS | Q |
| 6 | 3 | | B |
| 6 | 4 | | A |
| 6 | 7 | | D |
| 3 | 2 | PASS | Q |
| 3 | 3 | | B |
| 3 | 4 | | A |
| 3 | 7 | | D |
| 4 | 2 | "ZERO" | 0 |
| 4 | 3 | | 0 |
| 4 | 4 | | 0 |
| 4 | 7 | | 0 |
| 5 | 0 | MASK | $\overline{A}$ ∧ Q |
| 5 | 1 | | $\overline{A}$ ∧ B |
| 5 | 5 | | $\overline{D}$ ∧ A |
| 5 | 6 | | $\overline{D}$ ∧ Q |

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## SOURCE OPERAND AND ALU FUNCTION MATRIX (1)

| Octal | ALU | $I_{2,1,0}$ Octal | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
| Octal | ALU | ALU Source | | | | | | | |
| $I_{5,4,3}$ | Function | A, Q | A, B | 0, Q | 0, B | 0, A | D, A | D, Q | D, 0 |
| 0 | $C_n$ = L<br>R Plus S<br>$C_n$ = H | A + Q<br>A + Q + 1 | A + B<br>A + B + 1 | Q<br>Q + 1 | B<br>B + 1 | A<br>A + 1 | D + A<br>D + A + 1 | D + Q<br>D + Q + 1 | D<br>D + 1 |
| 1 | $C_n$ = L<br>S Minus R<br>$C_n$ = H | Q − A − 1<br>Q − A | B − A − 1<br>B − A | Q − 1<br>Q | B − 1<br>B | A − 1<br>A | A − D − 1<br>A − D | Q − D − 1<br>Q − D | −D − 1<br>−D |
| 2 | $C_n$ = L<br>R Minus S<br>$C_n$ = H | A − Q − 1<br>A − Q | A − B − 1<br>A − B | −Q − 1<br>−Q | −B − 1<br>−B | −A − 1<br>−A | D − A − 1<br>D − A | D − Q − 1<br>D − Q | D − 1<br>D |
| 3 | R OR S | A ∨ Q | A ∨ B | Q | B | A | D ∨ A | D ∨ Q | D |
| 4 | R AND S | A ∧ Q | A ∧ B | 0 | 0 | 0 | D ∧ A | D ∧ Q | 0 |
| 5 | $\overline{R}$ AND S | $\overline{A}$ ∧ Q | $\overline{A}$ ∧ B | Q | B | A | $\overline{D}$ ∧ A | $\overline{D}$ ∧ Q | 0 |
| 6 | R EX-OR S | A ∇ Q | A ∇ B | Q | B | A | D ∇ A | D ∇ Q | D |
| 7 | R EX-NOR S | $\overline{A \nabla Q}$ | $\overline{A \nabla B}$ | $\overline{Q}$ | $\overline{B}$ | $\overline{A}$ | $\overline{D \nabla A}$ | $\overline{D \nabla Q}$ | $\overline{D}$ |

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**NOTE:**
1. + = Plus; − = Minus; ∧ = AND; ∇ = EX-OR; ∨ = OR.

## ALU DESTINATION CONTROL(1)

| | Microcode | | | | | RAM Function | | Q Register Function | | Y | RAM Shifter | | Q Shifter | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Mnemonic | $I_8$ | $I_8$ | $I_7$ | $I_6$ | Hex Code | Shift | Load | Shift | Load | Output | $RAM_0$ | $RAM_{15}$ | $Q_0$ | $Q_{15}$ | |
| OREG | H | L | L | L | 8 | X | NONE | NONE | F → Q | F | X | X | X | X | Existing 2901 |
| NOP | H | L | L | H | 9 | X | NONE | X | NONE | F | X | X | X | X | Functions |
| RAMA | H | L | H | L | A | NONE | F → B | X | NONE | A | X | X | X | X | |
| RAMF | H | L | H | H | B | NONE | F → B | X | NONE | F | X | X | X | X | |
| RAMQD | H | H | L | L | C | DOWN | F/2 → B | DOWN | Q/2 → Q | F | $F_0$ | $IN_{15}$ | $Q_0$ | $IN_{15}$ | |
| RAMD | H | H | L | H | D | DOWN | F/2 → B | X | NONE | F | $F_0$ | $IN_{15}$ | $Q_0$ | X | |
| RAMQU | H | H | H | L | E | UP | 2F → B | UP | 2Q → Q | F | $IN_0$ | $F_{15}$ | $IN_0$ | $Q_{15}$ | |
| RAMU | H | H | H | H | F | UP | 2F → B | X | NONE | F | $IN_0$ | $F_{15}$ | X | $Q_{15}$ | |
| DFF | L | L | L | L | 0 | NONE | D → B | NONE | F → Q | F | X | X | X | X | New Added |
| DFA | L | L | L | H | 1 | NONE | D → B | NONE | F → Q | A | X | X | X | X | IDT49C402 |
| FDF | L | L | H | L | 2 | NONE | F → B | NONE | D → Q | F | X | X | X | X | Functions |
| FDA | L | L | H | H | 3 | NONE | F → B | NONE | D → Q | A | X | X | X | X | |
| XQDF | L | H | L | L | 4 | X | NONE | DOWN | Q/2 → Q | F | X | X | $Q_0$ | $IN_{15}$ | |
| DXF | L | H | L | H | 5 | NONE | D → B | X | NONE | F | X | X | $Q_0$ | X | |
| XQUF | L | H | H | L | 6 | X | NONE | UP | 2Q → Q | F | X | X | $IN_0$ | $Q_{15}$ | |
| XDF | L | H | H | H | 7 | X | NONE | NONE | D → Q | F | X | X | X | $Q_{15}$ | |

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**NOTE:**
1. X = Don't care. Electrically, the shift pin is a TTL input internally connected to a three-state output which is in the impedance state.
   B = Register Addressed by B inputs.
   UP is toward MSB; DOWN is toward LSB.

## ABSOLUTE MAXIMUM RATINGS[1]

| Symbol | Rating | Com'l. | Mil. | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Power Supply Voltage | -0.5 to +7.0 | -0.5 to +7.0 | V |
| $V_{TERM}$ | Terminal Voltage with Respect to Ground | –0.5 to $V_{CC}$ + 0.5 | –0.5 to $V_{CC}$ + 0.5 | V |
| $T_A$ | Operating Temperature | 0 to +70 | –55 to +125 | °C |
| $T_{BIAS}$ | Temperature Under Bias | –55 to +125 | –65 to +135 | °C |
| $T_{STG}$ | Storage Temperature | –55 to +125 | –65 to +150 | °C |
| $P_T$ | Power Dissipation | 1.5 | 1.5 | W |
| $I_{OUT}$ | DC Output Current | 50 | 50 | mA |

**NOTE:** 2524 tbl 08

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## CAPACITANCE ($T_A$ = +25°C, f = 1.0MHz)

| Symbol | Parameter [1] | Conditions | Typ. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | 5 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0V | 7 | pF |

**NOTE:** 2524 tbl 09

1. This parameter is sampled and not 100% tested.

## DC ELECTRICAL CHARACTERISTICS

Commercial: $T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0V ± 5%; Military: $T_A$ = –55°C to +125°C, $V_{CC}$ = 5.0V ± 10%

| Symbol | Parameter | Test Conditions [1] | | Min. | Typ. [2] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Level | Guaranteed Logic High Level | | 2.0 | – | – | V |
| $V_{IL}$ | Input LOW Level | Guaranteed Logic Low Level | | – | – | 0.8 | V |
| $I_{IH}$ | Input HIGH Current | $V_{CC}$ = Max., $V_{IN}$ = $V_{CC}$ | | – | 0.1 | 5 | µA |
| $I_{IL}$ | Input LOW Current | $V_{CC}$ = Max., $V_{IN}$ = GND | | – | –0.1 | –5 | µA |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min. | $I_{OH}$ = –6mA MIL. | 2.4 | 4.3 | – | V |
| | | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = –8mA COM'L. | 2.4 | 4.3 | – | |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min. | $I_{OL}$ = 8mA MIL. | – | 0.3 | 0.5 | V |
| | | $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 10mA COM'L. | – | 0.3 | 0.5 | |
| $I_{OZ}$ | Off State (High Impedance) Output Current | $V_{CC}$ = Max. | $V_O$ = 0V | – | –0.1 | –10 | µA |
| | | | $V_O$ = $V_{CC}$ (Max.) | – | 0.1 | 10 | |
| $I_{OS}$ | Output Short Circuit Current | $V_{CC}$ = Max., $V_{OUT}$ = 0V [3] | | –15 | –30 | –70 | mA |

**NOTES:** 2524 tbl 10

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at $V_{CC}$ = 5.0V, +25°C ambient and maximum loading, not production tested.
3. Not more than one output should be shorted at one time. Duration of the circuit test should not exceed one second.

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## DC ELECTRICAL CHARACTERISTICS

Commercial: $T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0V ± 5%; Military: $T_A$ = –55°C to +125°C, $V_{CC}$ = 5.0V ± 10%

| Symbol | Parameter | Test Conditions[1] | | Min. | Typ.[2] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $I_{CCQH}$ | Quiescent Power Supply Current | $V_{CC}$ = Max. | MIL. | – | – | 10 | mA |
| | CP = H (CMOS Inputs) | $V_{IH}$ = $V_{CC}$, $V_{IL}$ = 0V | COM'L. | – | – | 10 | |
| | | $f_{CP}$ = 0, CP = H | | | | | |
| $I_{CCQL}$ | Quiescent Power Supply Current | $V_{CC}$ = Max. | MIL. | – | – | 10 | mA |
| | CP = L (CMOS Inputs) | $V_{IH}$ = $V_{CC}$, $V_{IL}$ = 0V | COM'L. | – | – | 10 | |
| | | $f_{CP}$ = 0, CP = L | | | | | |
| $I_{CCT}$ | Quiescent Input Power Supply[6] | $V_{CC}$ = Max., $V_{IH}$ = 3.4V, $f_{CP}$ = 0 | MIL. | – | – | 1.5 | mA/ |
| | Current (per Input @ TTL High) | | COM'L. | – | – | 0.85 | Input |
| $I_{CCD}$ | Dynamic Power Supply Current | $V_{CC}$ = Max. | MIL. | – | – | 7.5 | mA/ |
| | | $V_{IH}$ = $V_{CC}$, $V_{IL}$ = 0V | COM'L. | – | – | 4.5 | MHz |
| | | Outputs Open, $\overline{OE}$ = L | | | | | |
| $I_{CC}$ | Total Power Supply Current[7] | $V_{CC}$ = Max.., $f_{CP}$ = 10MHz | MIL. | – | – | 85 | mA |
| | | Outputs Open, $\overline{OE}$ = L | COM'L. | – | – | 55 | |
| | | CP = 50 % Duty cycle | | | | | |
| | | $V_{IH}$ = $V_{CC}$, $V_{IL}$ = 0V | | | | | |
| | | $V_{CC}$ = Max.., $f_{CP}$ = 10MHz | MIL. | – | – | 130 | |
| | | Outputs Open, $\overline{OE}$ = L | COM'L. | – | – | 95 | |
| | | CP = 50 % Duty cycle | | | | | |
| | | $V_{IH}$ = 3.4V, $V_{IL}$ = 0.4V | | | | | |

2524 tbl 11

**NOTES:**

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics.
2. Typical values are at $V_{CC}$ = 5.0V, +25°C ambient and maximum loading, not production tested.
3. Not more than one output should be shorted at one time. Duration of the circuit test should not exceed one second.
4. These input levels provide zero noise immunity and should only be static tested in a noise-free environment.
5. Guaranteed by design, not production tested.
6. $I_{CCT}$ is derived by measuring the total current with all the inputs tied together at 3.4V, subtracting out $I_{CCQH}$, then dividing by the total number of inputs.
7. Total Supply Current is the sum of the Quiescent current and the Dynamic current (at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:
   $I_{CC}$ = $I_{CCQH}$ ($CD_H$) +$I_{CCQL}$ (1 – $CD_H$) + $I_{CCT}$ ($N_T$ x $D_H$) + $I_{CCD}$ ($f_{CP}$ /2 +fiNi)
   $CD_H$ = Clock duty cycle high period
   $D_H$ = Data duty cycle TTL high period ($V_{IN}$ = 3.4V)
   $N_T$ = Number of dynamic inputs driven at TTL levels
   $f_{CP}$ = Clock input frequency
   $I_{CCT}$ = Quiescent Power Supply Current for TTL level inputs
   $I_{CCD}$ =Dynamic Power Supply Current in mA/MHz
   fi =Input frequency
   Ni =Number of inputs switching

## AC ELECTRICAL CHARACTERISTICS IDT49C402

**(Military and Commercial Temperature Ranges)**

The tables below specify the guaranteed performance of the IDT49C402 over the –55°C to +125°C and 0°C to +70°C temperature ranges. Vcc is specified at 5V ± 10% for military temperature range and 5V ± 5% for commercial temperature range. All times are in nanoseconds and are measured at the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads.

## CYCLE TIME AND CLOCK CHARACTERISTICS

| | Mil. (6) | Com'l. | Unit |
|---|---|---|---|
| Read-Modify-Write Cycle (from selection of A, B registers to end of cycle) | 50 | 48 | ns |
| Maximum Clock Frequency to shift Q (50% duty cycle, I = C32 or E32) | 20 | 21 | MHz |
| Minimum Clock LOW Time | 30 | 25 | ns |
| Minimum Clock HIGH Time | 20 | 20 | ns |
| Minimum Clock Period | 50 | 48 | ns |

2524 tbl 13

## MAXIMUM COMBINATIONAL PROPAGATION DELAYS(1) $C_L$ = 50pF

| From Input | To Output: Y | | (MSS = L) $\overline{G}$, $\overline{P}$ | | (MSS = H) $F_{15}$ | | OVR | | $C_{n+16}$ | | F = 0 | | $RAM_0$ $RAM_{15}$ | | $Q_0$ $Q_{15}$ | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Mil. | Com'l. | Mil. | Com'l. | Mil. | Com'l. | Mil. | Com'l. | Mil. | Com'l. | Mil. | Com'l. | Mil. | Com'l. | Mil. | Com'l. | Unit |
| A, B Address | 52 | 47 | 47 | 42 | 52 | 47 | 47 | 42 | 38 | 34 | 52 | 47 | 44 | 40 | – | – | ns |
| D | 35 | 32 | 34 | 31 | 35 | 32 | 34 | 31 | 27 | 25 | 35 | 32 | 28 | 26 | – | – | ns |
| $C_n$ | 29 | 26 | – | – | 29 | 26 | 27 | 25 | 20 | 18 | 29 | 26 | 23 | 21 | – | – | ns |
| $I_{0, 1, 2}$ | 41 | 37 | 30 | 27 | 41 | 37 | 38 | 35 | 29 | 26 | 41 | 37 | 30 | 27 | – | – | ns |
| $I_{3, 4, 5}$ | 40 | 36 | 28 | 26 | 40 | 36 | 37 | 34 | 27 | 25 | 40 | 36 | 28 | 26 | – | – | ns |
| $I_{6, 7, 8, 9}$ | 26 | 24 | – | – | – | – | – | – | – | – | – | – | 20 | 18 | 20 | 18 | ns |
| A Bypass ALU (I = AXX, 1XX, 3XX) | 30 | 27 | – | – | – | – | – | – | – | – | – | – | – | – | – | – | ns |
| Clock ↓ | 42 | 38 | 41 | 37 | 42 | 38 | 41 | 37 | 30 | 27 | 42 | 38 | 41 | 37 | 25 | 23 | ns |

2524 tbl 14

## MINIMUM SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP INPUT)

CP: 

| Input | Set-up Time Before H → L | | Hold Time After H → L | | Set-up Time Before L → H | | Hold Time After L → H | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | Mil. | Com'l. | Mil. | Com'l. | Mil. | Com'l. | Mil. | Com'l. | |
| A, B Source Address | 20 | 18 | 2 (3) | 1 (3) | 50 (4) | 50 (4) | 2 | 1 | ns |
| B Destination Address | 20 | 18 | Do not change (2) | | | | 2 | 1 | ns |
| D | – (1) | – | – | – | 30/40 (5) | 26/36 (5) | 2 | 1 | ns |
| $C_n$ | – | – | – | – | 35 | 32 | 0 | 0 | ns |
| $I_{0, 1, 2}$ | – | – | – | – | 45 | 41 | 0 | 0 | ns |
| $I_{3, 4, 5}$ | – | – | – | – | 45 | 41 | 0 | 0 | ns |
| $I_{6, 7, 8, 9}$ | 12 | 11 | Do not change (2) | | | | 0 | 0 | ns |
| $RAM_{0,15}$, $Q_{0,15}$ | – | – | – | – | 12 | 11 | 0 | 0 | ns |

2524 tbl 15

**NOTES:**

1. A dash indicates a propagation delay or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation.
3. Source addresses must be stable prior to the H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination: i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU and returned to the RAM. It includes all the time from stable A and B addresses to the clock L → H transition, regardless of when the H → L transition occurs.
5. First value is direct path ($DATA_{IN}$ → RAM/Q Register). Second value is indirect path ($DATA_{IN}$ → ALU → RAM/Q Register).
6. Guaranteed by design, not production tested.

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## AC ELECTRICAL CHARACTERISTICS IDT49C402A

**(Military and Commercial Temperature Ranges)**

The tables below specify the guaranteed performance of the IDT49C402A over the –55°C to +125°C and 0°C to +70°C temperature ranges. Vcc is specified at 5V ± 10% for military temperature range and 5V ± 5% for commercial temperature range. All times are in nanoseconds and are measured at the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads.

## CYCLE TIME AND CLOCK CHARACTERISTICS

| | Mil.(6) | Com'l. | Unit |
|---|---|---|---|
| Read-Modify-Write Cycle (from selection of A, B registers to end of cycle)(6) | 23 | 22 | ns |
| Maximum Clock Frequency to shift Q (50% duty cycle, I = C32 or E32)(6) | 35 | 41 | MHz |
| Minimum Clock LOW Time | 13 | 11 | ns |
| Minimum Clock HIGH Time | 13 | 11 | ns |
| Minimum Clock Period(6) | 36 | 31 | ns |

2524 tbl 16

## MAXIMUM COMBINATIONAL PROPAGATION DELAYS(1) $C_L$ = 50pF

| From Input | To Output: Y | | (MSS = L) $\overline{G}$, $\overline{P}$ | | (MSS = H) $F_{15}$ | | (MSS = H) OVR | | $C_{n+16}$ | | F = 0 | | $RAM_0$ $RAM_{15}$ | | $Q_0$ $Q_{15}$ | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Mil. | Com'l. | Mil. | Com'l. | Mil. | Com'l. | Mil. | Com'l. | Mil. | Com'l. | Mil. | Com'l. | Mil. | Com'l. | Mil. | Com'l. | |
| A, B Address | 41 | 37 | 39 | 35 | 41 | 37 | 41 | 37 | 37 | 34 | 41 | 37 | 40 | 36 | – | – | ns |
| D | 32 | 29 | 29 | 26 | 29 | 26 | 31 | 28 | 27 | 25 | 32 | 29 | 28 | 26 | – | – | ns |
| $C_n$ | 28 | 25 | – | – | 26 | 24 | 25 | 23 | 20 | 18 | 29 | 26 | 23 | 21 | – | – | ns |
| $I_{0,1,2}$ | 35 | 32 | 30 | 27 | 35 | 32 | 34 | 31 | 29 | 26 | 35 | 32 | 30 | 27 | – | – | ns |
| $I_{3,4,5}$ | 35 | 32 | 28 | 26 | 34 | 31 | 34 | 31 | 27 | 25 | 35 | 32 | 28 | 26 | – | – | ns |
| $I_{6,7,8,9}$ | 25 | 23 | – | – | – | – | – | – | – | – | – | – | 20 | 18 | 20 | 18 | ns |
| A Bypass ALU (I = AXX, 1XX, 3XX) | 30 | 27 | – | – | – | – | – | – | – | – | – | – | – | – | – | – | ns |
| Clock ↓ | 34 | 31 | 31 | 28 | 33 | 30 | 34 | 31 | 30 | 27 | 34 | 31 | 34 | 31 | 25 | 23 | ns |

2524 tbl 17

## MINIMUM SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP INPUT)

CP: 

| Input | Set-up Time Before H → L | | Hold Time After H → L | | Set-up Time Before L → H | | Hold Time After L → H | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | Mil. | Com'l. | Mil. | Com'l. | Mil. | Com'l. | Mil. | Com'l. | |
| A, B Source Address | 11 | 10 | 2 (3) | 1 (3) | 25 (4) | 21 (4) | 2 | 1 | ns |
| B Destination Address | 11 | 10 | Do not change (2) | | | | 2 | 1 | ns |
| D | – (1) | – | – | – | 12/22 (5) | 10/20 (5) | 2 | 1 | ns |
| $C_n$ | – | – | – | – | 17 | 15 | 0 | 0 | ns |
| $I_{0,1,2}$ | – | – | – | – | 28 | 25 | 0 | 0 | ns |
| $I_{3,4,5}$ | – | – | – | – | 28 | 25 | 0 | 0 | ns |
| $I_{6,7,8,9}$ | 11 | 10 | Do not change (2) | | | | 0 | 0 | ns |
| $RAM_{0,15}$, $Q_{0,15}$ | – | – | – | – | 12 | 11 | 0 | 0 | ns |

2524 tbl 18

**NOTES:**

1. A dash indicates a propagation delay or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation.
3. Source addresses must be stable prior to the H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination: i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU and returned to the RAM. It includes all the time from stable A and B addresses to the clock L → H transition, regardless of when the H → L transition occurs.
5. First value is direct path ($DATA_{IN}$ → RAM/Q Register). Second value is indirect path ($DATA_{IN}$ → ALU → RAM/Q Register).
6. Guaranteed by design, not production tested.

## AC ELECTRICAL CHARACTERISTICS IDT49C402B

**(Military and Commercial Temperature Ranges)**

The tables below specify the guaranteed performance of the IDT49C402B over the –55°C to +125°C and 0°C to +70°C temperature ranges. Vcc is specified at 5V ± 10% for military temperature range and 5V ± 5% for commercial temperature range. All times are in nanoseconds and are measured at the 1.5V signal level. The inputs switch between 0V and 3V with signal transition rates of 1V per nanosecond. All outputs have maximum DC current loads.

## CYCLE TIME AND CLOCK CHARACTERISTICS

| | Mil.[6] | Com'l. | Unit |
|---|---|---|---|
| Read-Modify-Write Cycle (from selection of A, B registers to end of cycle)[6] | 22 | 19 | ns |
| Maximum Clock Frequency to shift Q (50% duty cycle, I = C32 or E32)[6] | 52 | 60 | MHz |
| Minimum Clock LOW Time | 11 | 9 | ns |
| Minimum Clock HIGH Time | 11 | 9 | ns |
| Minimum Clock Period[6] | 24 | 20 | ns |

2524 tbl 19

## MAXIMUM COMBINATIONAL PROPAGATION DELAYS[1] $C_L$ = 50pF

| From Input | To Output: Y | | (MSS = L) $\overline{G}$, $\overline{P}$ | | (MSS = H) F15 | | OVR | | $C_{n+16}$ | | F = 0 | | $RAM_0$ $RAM_{15}$ | | $Q_0$ $Q_{15}$ | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Mil. | Com'l. | Mil. | Com'l. | Mil. | Com'l. | Mil. | Com'l. | Mil. | Com'l. | Mil. | Com'l. | Mil. | Com'l. | Mil. | Com'l. | |
| A, B Address | 33 | 28 | 31 | 26 | 31 | 28 | 31 | 28 | 28 | 26 | 31 | 28 | 32 | 29 | – | – | ns |
| D | 26 | 23 | 23 | 21 | 23 | 21 | 25 | 22 | 22 | 20 | 26 | 23 | 24 | 23 | – | – | ns |
| $C_n$ | 22 | 20 | – | – | 20 | 18 | 19 | 17 | 15 | 14 | 22 | 20 | 18 | 17 | – | – | ns |
| $I_{0,1,2}$ | 28 | 26 | 24 | 22 | 28 | 26 | 27 | 25 | 23 | 21 | 28 | 26 | 26 | 24 | – | – | ns |
| $I_{3,4,5}$ | 28 | 26 | 22 | 21 | 27 | 25 | 27 | 25 | 22 | 20 | 28 | 26 | 25 | 23 | – | – | ns |
| $I_{6,7,8,9}$ | 20 | 18 | – | – | – | – | – | – | – | – | – | – | 16 | 14 | 16 | 14 | ns |
| A Bypass ALU (I = AXX, 1XX, 3XX) | 24 | 22 | – | – | – | – | – | – | – | – | – | – | – | – | – | – | ns |
| Clock ↓ | 27 | 25 | 25 | 22 | 26 | 24 | 27 | 25 | 25 | 22 | 27 | 25 | 27 | 25 | 20 | 18 | ns |

2524 tbl 20

## MINIMUM SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP INPUT)

CP: 

| Input | Set-up Time Before H → L | | Hold Time After H → L | | Set-up Time Before L → H | | Hold Time After L → H | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | Mil. | Com'l. | Mil. | Com'l. | Mil. | Com'l. | Mil. | Com'l. | |
| A, B Source Address | 10 | 9 | 2 [3] | 1 [3] | 20 [4] | 18 [4] | 2 | 1 | ns |
| B Destination Address | 10 | 9 | Do not change[2] | | | | 2 | 1 | ns |
| D | – [1] | – | – | – | 12/22[5] | 10/20[5] | 2 | 1 | ns |
| $C_n$ | – | – | – | – | 16 | 14 | 0 | 0 | ns |
| $I_{0,1,2}$ | – | – | – | – | 26 | 24 | 0 | 0 | ns |
| $I_{3,4,5}$ | – | – | – | – | 26 | 24 | 0 | 0 | ns |
| $I_{6,7,8,9}$ | 10 | 9 | Do not change[2] | | | | 0 | 0 | ns |
| $RAM_{0,15}$, $Q_{0,15}$ | – | – | – | – | 12 | 10 | 0 | 0 | ns |

2524 tbl 21

**NOTES:**

1. A dash indicates a propagation delay or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation.
3. Source addresses must be stable prior to the H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination: i.e., if data is not being written back into the RAM. Normally A and B are not changed during the clock LOW time.
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU and returned to the RAM. It includes all the time from stable A and B addresses to the clock L → H transition, regardless of when the H → L transition occurs.
5. First value is direct path ($DATA_{IN}$ → RAM/Q Register). Second value is indirect path ($DATA_{IN}$ → ALU → RAM/Q Register).
6. Guaranteed by design, not production tested.

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## IDT49C402B
## MAX. OUTPUT ENABLE/DISABLE TIMES

($C_L$ = 5pF, measured to 0.5V change of $V_{OUT}$ in nanoseconds)
Tested at $C_L$ = 50pF, correlated to 5pF

| Input | Output | Enable | | Disable | |
|---|---|---|---|---|---|
| | | Mil. | Com'l. | Mil. | Com'l. |
| $\overline{OE}$ | Y | 18 | 16 | 15 | 13 |

2524 tbl 22

## IDT49C402A
## MAX. OUTPUT ENABLE/DISABLE TIMES

($C_L$ = 5pF, measured to 0.5V change of $V_{OUT}$ in nanoseconds)
Tested at $C_L$ = 50pF, correlated to 5pF

| Input | Output | Enable | | Disable | |
|---|---|---|---|---|---|
| | | Mil. | Com'l. | Mil. | Com'l. |
| $\overline{OE}$ | Y | 22 | 20 | 20 | 18 |

2524 tbl 23

## IDT49C402
## MAX. OUTPUT ENABLE/DISABLE TIMES

($C_L$ = 5pF, measured to 0.5V change of $V_{OUT}$ in nanoseconds)
Tested at $C_L$ = 50pF, correlated to 5pF

| Input | Output | Enable | | Disable | |
|---|---|---|---|---|---|
| | | Mil. | Com'l. | Mil. | Com'l. |
| $\overline{OE}$ | Y | 25 | 23 | 25 | 23 |

2524 tbl 24

## CRITICAL SPEED PATH ANALYSIS

Critical speed paths for the IDT49C402B versus the equivalent bipolar circuit implementation using four 2901Cs and one 2902A are shown below.

The IDT49C402B operates faster than the theoretically achievable values of the discrete bipolar implementation. Actual speed values for the discrete bipolar circuit will increase due to on-chip/off-chip circuit board delays.

## TIMING COMPARISION: IDT49C402B vs 2901C w/2902A

| 16–Bit µP System | Data Path (Com'l.) | | Data Path (Mil.) | | Unit |
|---|---|---|---|---|---|
| | AB ADDR → F = 0 | AB ADDR → $RAM_{0, 15}$ | AB ADDR → F = 0 | AB ADDR → $RAM_{0, 15}$ | |
| Four 2901Cs + 2902A | ≥ 71 | ≥ 71 | ≥ 83.5 | ≥ 83.5 | ns |
| IDT49C402B | 28 | 23 | 31 | 25 | ns |
| Speed Savings | 43 | 48 | 52 | 55 | ns |

2524 tbl 26

## TIMING COMPARISION: IDT49C402A vs 2901C w/2902A

| 16–Bit µP System | Data Path (Com'l.) | | Data Path (Mil.) | | Unit |
|---|---|---|---|---|---|
| | AB ADDR → F = 0 | AB ADDR → $RAM_{0, 15}$ | AB ADDR → F = 0 | AB ADDR → $RAM_{0, 15}$ | |
| Four 2901Cs + 2902A | ≥ 71 | ≥ 71 | ≥ 83.5 | ≥ 83.5 | ns |
| IDT49C402A | 37 | 36 | 41 | 25 | ns |
| Speed Savings | 34 | 35 | 42.5 | 43.5 | ns |

2524 tbl 27

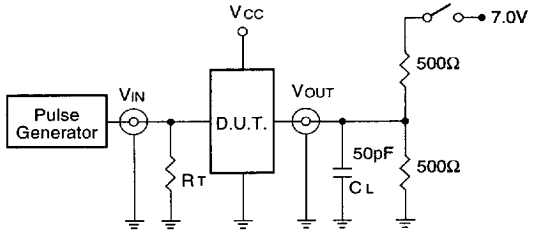
## TIMING COMPARISION: IDT49C402 vs 2901C w/2902A

| 16–Bit µP System | Data Path (Com'l.) | | Data Path (Mil.) | | Unit |
|---|---|---|---|---|---|
| | AB ADDR → F = 0 | AB ADDR → $RAM_{0, 15}$ | AB ADDR → F = 0 | AB ADDR → $RAM_{0, 15}$ | |
| Four 2901Cs + 2902A | ≥ 71 | ≥ 71 | ≥ 83.5 | ≥ 83.5 | ns |
| IDT49C402A | 47 | 40 | 52 | 44 | ns |
| Speed Savings | 24 | 31 | 31.5 | 39.5 | ns |

2524 tbl 28

# TEST CIRCUITS AND WAVEFORMS

## TEST CIRCUITS FOR ALL OUTPUTS




2524 drw 05

## SWITCH POSITION

| Test | Switch |
|---|---|
| Open Drain<br>Disable Low<br>Enable Low | Closed |
| All Other Tests | Open |

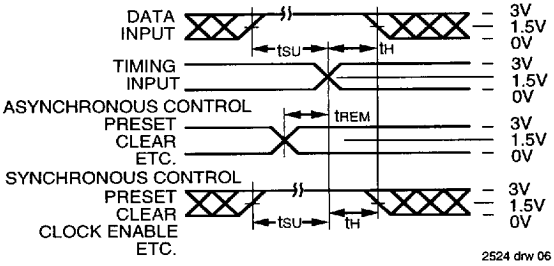
2524 lnk 25

**DEFINITIONS:**

$C_L$ = Load capacitance: includes jig and probe capacitance.

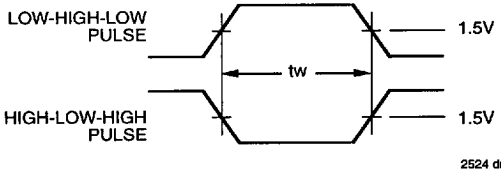
$R_T$ = Termination resistance: should be equal to $Z_{OUT}$ of the Pulse Generator.

## SET-UP, HOLD AND RELEASE TIMES



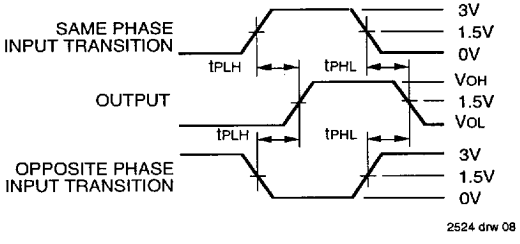

2524 drw 06

## PULSE TIMES



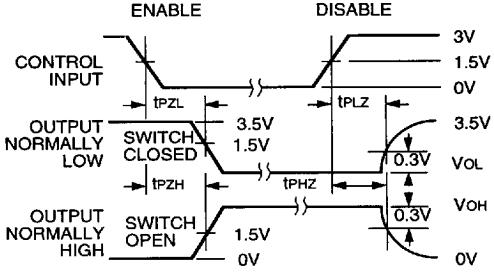

2524 drw 07

## PROPAGATION DELAY




2524 drw 08

## ENABLE AND DISABLE TIMES




2524 drw 10

**NOTES:**

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $t_F$ ≤ 2.5ns; $t_R$ ≤ 2.5ns

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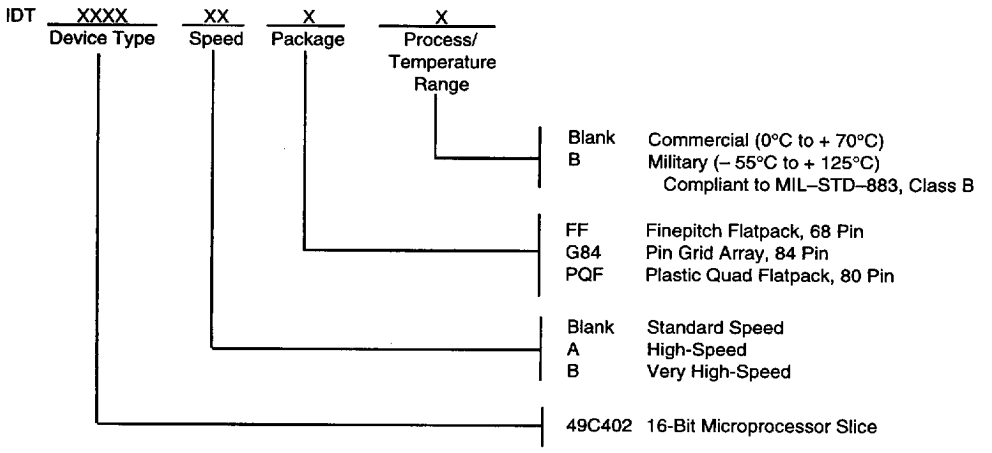
## ORDERING INFORMATION




2524 drw 09