Integrated Device Technology, Inc.

16-BIT CMOS MICROPROCESSOR SLICE

IDT 49C403
IDT 49C403A

FEATURES:

- Monolithic 16-bit CMOS μP Slice
- Replaces four 2903As/29203s and a 2902A
- Fast
  - 50% faster than four 2903As/29203s and a 2902
- Low power CMOS
  - Commercial: 250mA (max.)
  - Military: 275mA (max.)
- Performs binary and BCD Arithmetic
- Expanded two-address architecture with independent, simultaneous access to two, expandable 64 x 16 register files
- Word/Byte Control
- Expanded 4 x 16 Q Register
- Performs Byte Swap and Word/Byte Operation
- Fully cascadable without the need for additional carry lookahead
- Incorporates three 16-bit Bidirectional Busses
- Includes Serial Protocol Channel (SPC ™)
  - Flexible on-chip diagnostics
  - Serially monitors all pin states
  - Reads and Writes to Register File
- High Output Drive
  - Commercial: 16mA (max.)
  - Military: 12mA (max.)
- Available in 108-pin PGA
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT49C403 is a high-speed, fully cascadable 16-bit CMOS microprocessor slice. It combines the standard function of four 2903s/29203s and one 2902 with additional control features aimed at enhancing the performance of all bit-slice microprocessor designs.

Included in this extremely low power, yet fast IDT49C403 device are 3 bidirectional data buses, 64 word x 16-bit two-port expandable RAM, 4 word x 16-bit Q Register, parity generation, sign extension, multiplication/division and normalization logic. Additionally, the IDT49C403 offers the special feature of enhanced byte support through both word/byte control and byte swap control.

The IDT49C403 easily supports fast 100ns microcycles and will enhance the speed of all existing quad 2903A/29203 systems by 50%. Being specified at an extremely low 250mA, the IDT device offers an immediate system power savings and improved reliability.

Also featured on the IDT49C403 is an innovative diagnostics capability known as Serial Protocol Channel (SPC). This on-chip feature greatly simplifies the task of writing and debugging microcode, field maintenance debug and test, along with system testing during manufacturing.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

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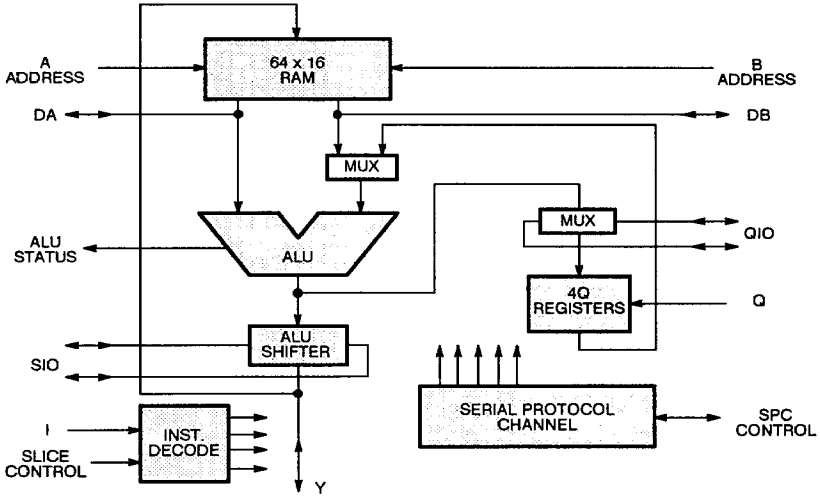
FUNCTIONAL BLOCK DIAGRAM



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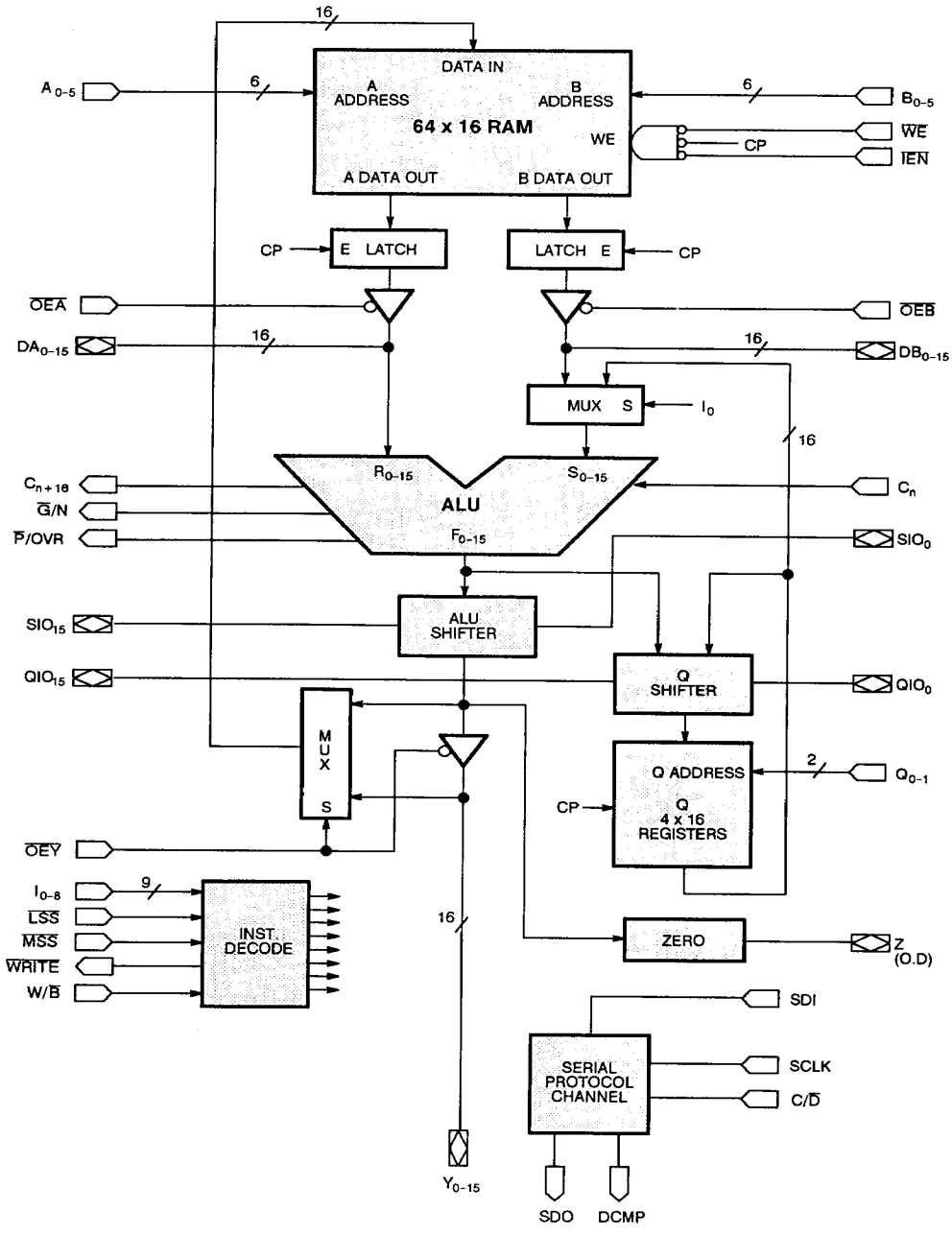
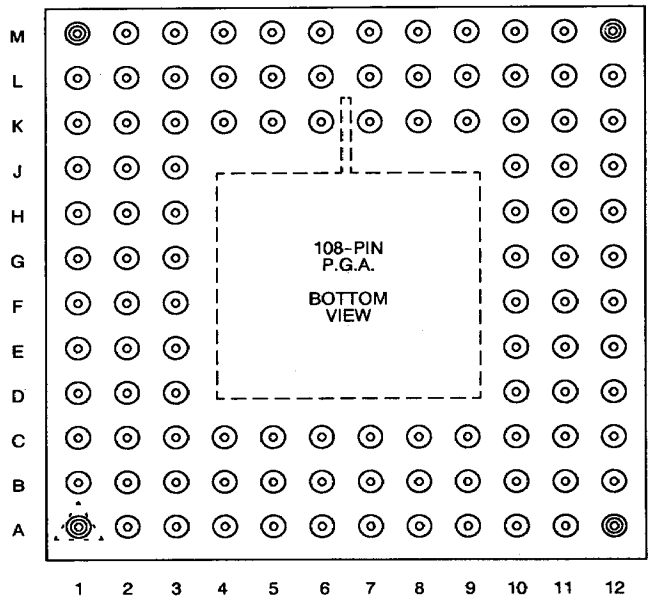
DETAILED BLOCK DIAGRAM



PIN CONFIGURATION



PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME
A1	N/C	B4	DB7	C7	DCMP	E10	W/$\overline{B}$	H1	DA2	K4	DA8	L7	$\overline{WE}$	M10	Q_0
A2	V_{CC}	B5	DB4	C8	I_5	E11	$\overline{OEY}$	H2	DA3	K5	DA12	L8	B_2	M11	V_{CC}
A3	$\overline{OEB}$	B6	DB1	C9	$\overline{IEN}$	E12	SIO_0	H3	DA5	K6	N/C	L9	B_5	M12	N/C
A4	DB5	B7	$\overline{MSS}$	C10	Y_2	F1	GND	H10	Y_{13}	K7	B_0	L10	Q_1		
A5	DB3	B8	I_7	C11	Y_5	F2	DB15	H11	Y_{11}	K8	B_4	L11	SCLK		
A6	DB0	B9	C_{n+16}	C12	Y_6	F3	DB14	H12	Y_{10}	K9	$\overline{WRITE}$	L12	C/$\overline{D}$		
A7	GND	B10	$\overline{P}$/OVR	D1	DB11	F10	QIO_0	J1	DA4	K10	GND	M1	V_{CC}		
A8	I_8	B11	Y_1	D2	DB9	F11	SIO_{15}	J2	DA6	K11	SDO	M2	A_5		
A9	I_6	B12	Y_3	D3	I_3	F12	QIO_{15}	J3	A_1	K12	Y_{15}	M3	DA10		
A10	$\overline{G}$/N	C1	DB8	D10	Y_4	G1	$\overline{OEA}$	J10	SDI	L1	A_2	M4	DA13		
A11	Y_0	C2	I_4	D11	Y_7	G2	DA0	J11	Y_{14}	L2	A_4	M5	DA15		
A12	V_{CC}	C3	GND	D12	Z	G3	DA1	J12	Y_{12}	L3	DA9	M6	GND		
B1	I_2	C4	I_0	E1	DB13	G10	Y_9	K1	DA7	L4	DA11	M7	CP		
B2	I_1	C5	DB6	E2	DB12	G11	Y_8	K2	A_0	L5	DA14	M8	B_1		
B3	C_n	C6	DB2	E3	DB10	G12	GND	K3	A_3	L6	$\overline{LSS}$	M9	B_3		

PIN DESCRIPTION

PIN NAME	I/O	DESCRIPTION
A_{0-5}	I	Six address inputs to the RAM containing the address of the RAM word appearing at output port A.
B_{0-5}	I	Six address inputs to the RAM which selects one of the words in the RAM, the contents of which is displayed through the B port. It also selects the location into which new data can be written when the $\overline{WE}$ input and CP input are low.
DA_{0-15}	I/O	Sixteen bi-directional data pins acting as operands R for entering external data into the ALU. DA_0 is the LSB. The DA lines also function as an external output for RAM port A.
DB_{0-15}	I/O	Sixteen bi-directional data pins for entering external data into the ALU. The DB lines act as either RAM port B output data, or as input operands S to the ALU.
$\overline{WE}$	I	The RAM write enable input, which when LOW causes the Y I/O port data to be written into the RAM when the CP input is low. When $\overline{WE}$ is HIGH writing data into the RAM is inhibited.
$\overline{OEA}$	I	Output enable, which, when HIGH selects DA_{0-15} as the ALU R operand, and, when LOW, selects RAM output A as the ALU R operand and the DA_{0-15} output data.
$\overline{OEB}$	I	Output enable, which, when HIGH selects DB_{0-15} as the ALU S operand, and, when LOW, selects RAM output B as the ALU S operand and the DB_{0-15} output data.
SIO_0 SIO_{15}	I/O	Bidirectional serial shift inputs/outputs for the ALU shifter. SIO_0 is an input and SIO_{15} is an output during a shift-up operation. SIO_{15} is an input and SIO_0 is an output during a shift-down operation. Refer to Tables 4 (a, b, c, d) and 5 for an exact definition of these pins.
QIO_0 QIO_{15}	I/O	Bidirectional serial shift inputs/outputs for the Q registers shifter. They operate like SIO_0 and SIO_{15} pins. Refer to Tables 4 (a, b, c, d) and 5 for an exact definition of these pins.
C_n	I	Carry-in input to the ALU.
$\overline{IEN}$	I	Instruction enable input. When LOW, it enables writing into the Q register and the Sign Compare flip-flop. When HIGH, the Q register and the Sign Compare flip-flop are in hold mode. $\overline{IEN}$ does not affect $\overline{WRITE}$, but internally disables the RAM write enable.
$\overline{LSS}$	I	Input pin, when held LOW, causes the chip to act as either stand alone slice (SA) or the least significant slice (LSS). When $\overline{LSS}$ is held HIGH, the chip acts as either an intermediate slice or most significant slice.
$\overline{MSS}$	I	Input pin, when held LOW, programs the chip to act as either stand alone slice (SA) or the most significant slice (MSS), and holding it HIGH programs the chip to act either as an intermediate slice (IS) or the least significant slice (LSS).
$\overline{WRITE}$	O	The $\overline{WRITE}$ signal is LOW when an instruction which causes data to be written into the RAM is being executed. This pin is normally connected to the $\overline{WE}$ pin.
C_{n+16}	O	This output indicates the carry out of the ALU. Refer to Tables 6a and 6b for an exact definition of this pin.
Z	I/O	An open drain bidirectional pin. When HIGH it indicates that all outputs are LOW. Z is used as an input pin for some special functions. Refer to Tables 6a and 6b for an exact definition of this pin.
$\overline{G}$/N	O	$\overline{G}$ indicates the carry generate function at the least significant and intermediate slices, and indicates the sign, N, of the ALU result at the most significant slice. Refer to Tables 6a and 6b for an exact definition of this pin.
$\overline{OEY}$	I	A control input pin. When LOW the ALU shifter output data is enabled onto the Y_{0-15} lines. When HIGH the Y_{0-15} three-state output buffers are disabled.
CP	I	Clock input. The Sign Compare flip-flop and the Q register are clocked on the LOW-to-HIGH transition of the CP signal. When $\overline{WE}$ and CP are LOW, data is written into the RAM.
$\overline{P}$/OVR	O	$\overline{P}$ indicates the carry propagate function at the least significant and intermediate slices, and indicates the conventional two's complement overflow, OVR, signal at the most significant slice. Refer to Tables 6a and 6b for an exact definition of this pin.
Y_{0-15}	I/O	Sixteen bi-directional data pins. Controlled by $\overline{OEY}$ input, the ALU shifter output data can be enabled onto these lines, or external data is written directly into the RAM using these lines as data inputs.
I_{0-8}	I	The nine instruction inputs used to select the IDT49C403 operation to be performed.
Q_{0-1}	I	Two address pins to select one of the four Q registers.
W/$\overline{B}$	I	Word/$\overline{Byte}$ control pin. Used only in the standard function mode, it selects Word mode when held HIGH and Byte mode when held LOW. Must be tied HIGH when the special functions are being used.
SDI	I	Serial Data Input pin, used for receiving diagnostic data and commands from a host system or from the SDO pin of a cascaded processor.
SDO	O	Serial Data Output pin, used for transmitting diagnostic data and commands to a host system or a cascaded processor via its SDI pin.
C/$\overline{D}$	I	Input pin, when LOW defines the bit pattern being received at the SDI pin as Data, and when HIGH defines the incoming pattern as a Command for executing diagnostic functions. This pin should be tied HIGH when the diagnostics feature is not being used.
SCLK	I	Input pin used for clocking in diagnostic data and command information at the SDI pin. This pin should be tied LOW when the diagnostics function is not being used.
DCMP	O	Output pin, which, when HIGH indicates that the internal comparison between the Y or Q bus data and the data from the diagnostics data register resulted in a TRUE (they were equal). This feature is used for breakpoint detection. It is an open-drain pin and can be wire AND with other DCMP pins.

DEVICE ARCHITECTURE

The IDT49C403 CMOS microprocessor slice is configured sixteen bits wide and is cascadable to any number of bits (32, 48, 64, etc.). Key elements which make up this sixteen-bit microprocessor slice are: (1) the RAM file (a 64 x 16 dual-port RAM) with latches on both outputs. (2) a high-performance ALU with shifter, (3) a flexible Q register file (4 x 16 bits) with shifter input, (4) a nine-bit instruction decoder, and (5) Serial Protocol Channel.

The IDT49C403 incorporates Serial Protocol Channel (SPC™). For system testing and debugging purposes SPC is a method by which data can be entered into and extracted from a device through a serial data input output, thus providing access to all internal registers.

REGISTER FILE

The Register File is composed of 64 x 16 bit RAM locations. The RAM data is read from the A-port as controlled by the 6-bit A address field input. Simultaneously, data can be read from the B port as defined by the 6-bit B address field input. If the same address is applied at both the A input field and the B input field, identical data will appear at the two respective output ports. Data is written into the RAM when $\overline{WE}$, $\overline{IEN}$ and the clock CP are LOW. Both the RAM output data latches are transparent while CP is HIGH and latch the data when CP is LOW. The three-state output enable $\overline{OEB}$ allows RAM B port data to be read at the DB I/O port, while $\overline{OEA}$ performs the same function for the A port data at the DA I/O port.

New data is written into the RAM word defined by the B address field. External data at the Y I/O port can be written directly into the RAM, or the ALU shifter output data can be enabled onto the Y I/O port and written into the RAM.

ALU

The ALU can perform seven arithmetic and nine logic operations on the two 16-bit input words S and R. Multiplexers at the ALU inputs allow selection of various pairs of ALU source operands. The $\overline{OEA}$ input selects either external DA data or RAM A port output data as the 16-bit R source operand. The $\overline{OEB}$ and I_0 inputs provide selection of either RAM B port output, external DB data or the Q register file output as the 16-bit S source operand. Also, during certain ALU operations, zeroes are forced at the ALU operand inputs. Thus, the ALU can operate on data from two external sources, from an external and an internal source, or from two internal sources. Table 1 shows all possible pairs of source operands as selected by $\overline{OEA}$, $\overline{OEB}$, and I_0 inputs.

Table 1. ALU Operand Sources(1)

$\overline{OEA}$	I_0	$\overline{OEB}$	ALU OPERAND R	ALU OPERAND S
L	L	L	Ram Output A	Ram Output B
L	L	H	Ram Output A	DB_{0-15}
L	H	X	Ram Output A	Q Register
H	L	L	DA_{0-15}	Ram Output B
H	L	H	DA_{0-15}	DB_{0-15}
H	H	X	DA_{0-15}	Q Register

NOTE:
1. L = LOW, H = HIGH, X = DON'T CARE

The ALU performs special functions when instruction bits I_3, I_2, I_1, and I_0 are LOW. Table 5 defines these special functions and the operation which the ALU performs for each instruction. When the ALU executes instructions other than the special functions, the operation is defined by instruction bits I_4, I_3, I_2, and I_1. Table 2 defines the operation as a function of these four instruction bits.

Table 2. IDT49C403 ALU Functions(1)

I_4	I_3	I_2	I_1	I_0	ALU FUNCTIONS
L	L	L	L	L	Special Functions
L	L	L	L	H	F_i = HIGH
L	L	L	H	X	$F = S-R-1+C_n$
L	L	H	L	X	$F = R-S-1+C_n$
L	L	H	H	X	$F = R+S+C_n$
L	H	L	L	X	$F = S+C_n$
L	H	L	H	X	$F = \overline{S}+C_n$
L	H	H	L	L	Reserved Special Functions
L	H	H	L	H	$F = R+C_n$
L	H	H	H	L	Reserved Special Functions
L	H	H	H	H	$F = \overline{R}+C_n$
H	L	L	L	L	Special Functions
H	L	L	L	H	F_i = LOW
H	L	L	H	X	$F_i = \overline{R}$ AND S
H	L	H	L	X	$F_i = R_i$ EXCLUSIVE NOR S_i
H	L	H	H	X	$F_i = R_i$ EXCLUSIVE OR S_i
H	H	L	L	X	$F_i = R_i$ AND S_i
H	H	L	H	X	$F_i = R_i$ NOR S_i
H	H	H	L	X	$F_i = R_i$ NAND S_i
H	H	H	H	X	$F_i = R_i$ OR S_i

NOTE:
1. L = LOW, H = HIGH, i = 0 to 15, X = Don't Care

The IDT49C403 may be cascaded in either a ripple carry or carry lookahead fashion. When configured as cascaded ALUs, the IDT49C403s must be programmed to be a most significant slice (MSS), an intermediate slice (IS), or a least significant slice (LSS) of the array. The carry generate, $\overline{G}$, and carry propagate, $\overline{P}$, signals that are necessary in a cascaded system are available as outputs on the IDT49C403 least significant and intermediate slices.

The IDT49C403 provides a carry-out signal C_{n+16} which is available as an output of each slice. The carry-in, C_n, and carry-out, C_{n+16}, are both active HIGH. Two other status outputs are generated by the ALU. These are the negative, N, and the overflow, OVR. The N output indicates positive or negative results, while the OVR output indicates that the arithmetic operation performed exceeded the available two's complement range. Thus the pins $\overline{G}$/N and $\overline{P}$/OVR indicate carry generate or propagate on the least significant and intermediate slice, and sign and overflow on the most significant slice.

Refer to Tables 6a and 6b for an exact definition of these four signals.

ALU DESTINATION CONTROL

The following tables show how the shifter at the output of the ALU should function for non-special instructions. The main addition with respect to the IDT39C203 is the built in byte capability.

The 49C403 has two write enables internally. One for the upper byte and one for the lower byte. The enables are controlled by the instruction decode, external $\overline{WE}$ and the W/$\overline{B}$ input. For convenience to the user, the unused bits on the Y bus (MSB, ..., 8) are zero during byte operation. The $\overline{WE}$ input must be directly connected to the WRITE output, or indirectly through some amount of gating (i.e., expansion RAM decoding gates).

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The sign extend function is an exception to the rule with regard to the internal byte write enables. When executed, all of the write enables are active, irrespective of W/$\overline{B}$. In the SA and LSS slices, the contents of bit 7 is replicated on bits 8 to 15 and SIO_{15} in the byte mode. In the word mode bit 15 is placed on SIO_{15}. In this way an 8-bit word (byte) or a 16-bit word can be extended to the entire width of the native data path. Extends of larger words than these, such as 24 and 32 bits, can be achieved by steering the $\overline{MSS}$ and $\overline{LSS}$ inputs of the IS slices to inform which device has the sign bit to extend. As Sign Extend requires internal gating of the write enables to the upper and lower portions of RAM, the instruction will not work with locations in memory expansion RAM.

ALU SHIFTER

The ALU shifter shifts the ALU output data under instruction control. It can shift up one bit position (2F), shift down one bit position (F/2), or pass the ALU output non-shifted (F). An arithmetic shift operation shifts the data around the most significant (Sign) bit of the most significant slice and a logical shift operation shifts the data through the most significant bit. Figure 1 shows these shift patterns. The SIO_0 and SIO_{15} are bidirectional serial shift input/output pins. During a shift-up operation, SIO_0 is generally an input while SIO_{15} is an output, whereas during a shift-down operation SIO_0 is generally an output while SIO_{15} acts as an input. Refer to Tables 4 (a, b, c, d) and 5 for an exact definition of these pins.

The ALU shifter also provides sign extension and parity generating/checking capabilities. Under instruction control, the SIO_0 (Sign) input can be extended through $Y_0, Y_1, Y_2, ...Y_{15}$ and propagated to the SIO_{15} output. A cascadable, five-bit parity generator/checking generates parity for the $F_0, F_1, F_2, ...F_{15}$ ALU outputs and SIO_{15} input and, under instruction control, is made available at the SIO_0 output.

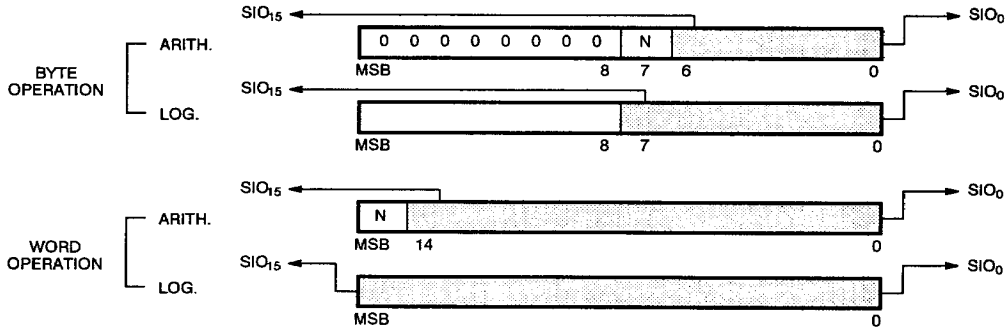

Figure 1. IDT49C403 Arithmetic and Logical Shift Operations

Table 5 defines the special functions and the operation the ALU shifter performs for each instruction. For instructions other than the special functions, the ALU shifter operation is determined by instruction bits I_8, I_7, I_6, and I_5. Table 4 (a, b, c, d) defines the ALU shifter operation as a function of these four bits.

WORD/BYTE CONTROL AND BYTE SWAP

In addition to the special ALU functions, the IDT49C403 also provides a Word and Byte control and Byte Swap features.

The W/$\overline{B}$ pin at the Instruction Decoder input selects ALU operation on either a Word or a Byte. When W/$\overline{B}$ is HIGH, the ALU operates on a Word and, when W/$\overline{B}$ is LOW, the ALU operates on a Byte. Table 4 (a, b, c, d) shows the ALU Destination Controls for Word and Byte operations for each instruction mode.

The Byte Swap special function allows the positions of the Upper and Lower bytes to be swapped before entering them as the ALU S operand. The ALU function then adds C_n to this swapped word as its F output. Table 5 shows the instruction set that allows the ALU to operate the Byte Swap feature.

Q REGISTER FILE

The Q register is a separate 4-word by 16-bit file intended primarily for multiplication and division routines and can also be used as an accumulator or holding register for other types of applications. The ALU output, F, can be loaded into the Q register and/or the Q register output can be selected as one of the ALU S operands. The shifter at the input to the Q register performs only logical shifts. It can shift-up the data one bit position (2Q) or down one bit position (Q/2). For a shift-up operation, QIO_0 acts as an input while QIO_{15} acts as an output; whereas, for a shift-down operation, QIO_0 is an output and QIO_{15} is an input. By connecting QIO_{15} of the most significant slice to SIO_0 of the least significant slice, double-length arithmetic and logical shifting is possible with cascaded IDT49C403s.

The Q_0 and Q_1 inputs enable selection of any one of the four 16-bit Q register files. Once a specific Q register has been selected, access to the other three Q registers is disabled and can be gained only after changing Q_0 and Q_1 levels to enable a different Q register.

Table 5 defines the special functions and the operations which the Q register and shifter perform for selected instruction inputs. While executing instructions other than the special functions, the Q register and shifter operation is controlled by instruction bits I_8, I_7, I_6 and I_5. Table 4 (a, b, c, d) defines the Q register and shifter operation as a function of these four bits.

INSTRUCTION DECODER

The internal control signals necessary for the operation of the IDT49C403 are generated by the instruction decoder as a function of the nine instruction inputs, I_{0-8}; the instruction enable input, $\overline{IEN}$; the $\overline{LSS}$ input; the $\overline{MSS}$ input; the W/$\overline{B}$ input and the $\overline{WRITE}$ output.

The $\overline{WRITE}$ output is LOW when an instruction which writes data into the RAM is executed. Refer to Tables 4 (a, b, c, d) and 5 for

a definition of the $\overline{WRITE}$ output as a function of the instruction inputs.

When $\overline{IEN}$ is HIGH, the Q register and Sign Compare Flip-Flop contents are preserved. When $\overline{IEN}$ is LOW, the $\overline{WRITE}$ output is enabled and the Q register and Sign Compare Flip-Flop can be written according to the IDT49C403 instruction. The Sign Compare Flip-Flop is an on-chip flip-flop which is used during a divide operation. See Figure 2.

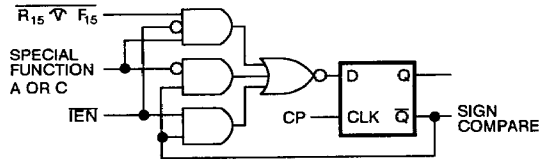

Figure 2. Sign Compare Flip-Flop

SLICE POSITION PROGRAMMING

The IDT49C403 can be programmed to operate in either a cascaded application or in the standalone mode. Table 3 shows its four programmed modes.

Table 3. SLICE Programming

SLICE PROGRAM INPUTS		MODE OF OPERATION
$\overline{MSS}$	$\overline{LSS}$	
LOW	LOW	Stand Alone Slice (SA)
LOW	HIGH	Most Significant Slice (MSS)
HIGH	HIGH	Intermediate Slice (IS)
HIGH	LOW	Least Significant Slice (LSS)

SPECIAL FUNCTIONS

Seventeen special functions are provided on the IDT49C403 which permit the implementation of the following operations:

- Single and Double Length Normalization
- Two's Complement Division
- Unsigned and Two's Complement Multiplication
- Conversion Between Two's Complement and Sign/Magnitude Representation
- Incrementation and Decrementation by One or Two
- BCD Add, Subtract, and Divide by Two
- Single and Double-precision BCD-to Binary and Binary-to-BCD Conversion
- Byte Swap

Adjusting a single-precision or double-precision floating-point number in order to bring its mantissa within a specified range can be performed using the single-length and double-length normalization operations.

Three special functions can be used to perform a two's complement, non-restoring divide operation. They provide single and double-precision divide operations and can be performed in "n" clock cycles (where "n" is the number of bits in the quotient).

The unsigned multiply special function and the two two's complement multiply special functions can be used to multiply two n-bit, unsigned or two's complement numbers respectively, in 'n' clock cycles. During the last cycle of the two's complement multiplication, a conditional subtraction rather than addition is performed due to the fact that the sign bit of the multiplier carries negative weight.

The sign/magnitude—two's complement special function can be used to convert number representation systems. A number expressed in sign/magnitude representation can be converted to the two's complement representation, and vice-versa, in one clock cycle.

Incrementing an unsigned or two's complement number by one or two is easily accomplished using the increment by one or two special function.

In addition to BCD arithmetic special functions to add or subtract two BCD numbers, a BCD divide by two adjust instruction can be used to obtain a valid BCD representation after shifting a number down by one bit.

The BCD/Binary conversion special function instructions permit single and double-precision algorithms to convert from BCD-to-Binary and from Binary-to-BCD.

The Byte Swap feature allows the swapping of Lower and Upper bytes of a word before presenting them as the ALU S operand. The ALU then adds the carry C_n to this swapped word to form its F output. This feature functions only for the ALU S operand.

SERIAL DIAGNOSTICS

The Serial Protocol Channel ™ (SPC) is a flexible on-chip feature of the IDT49C403 and is a set of pins by which data can be entered into and extracted from a device through a serial data input and output port.

SPC can be used at many points in the life of a product for diagnostic purposes such as system level design debug and development; system test during manufacturing and field maintenance debug and test. It allows for observation of critical signals deep within the system. During system test, when an error is observed, these signals may be modified in order to zero in on the fault in the system. Serial diagnostics is primarily a scheme utilizing only four pins to examine and alter the internal state of a system for the purpose of monitoring and diagnosing system faults.

Detailed SPC Architecture of the IDT49C403 Bit-Slice Microprocessor

The IDT49C403, a quad Am2903/29203 16-bit microprocessor slice, which includes an ALU and register file, is one of the devices on which IDT has incorporated the Serial Protocol Channel. The implementation of SPC on the IDT49C403 is shown in Figure 3.

Only four SPC pins (SDI, SDO, SCLK and C/$\overline{D}$) are used to serially access the I/O pad cells, as well as the internal ALU registers and buses. To control or monitor a section (such as the ALU), the appropriate command is loaded into the SPC command register. The desired function is then executed and the status information captured in the data register. The status information can then be serially shifted out and observed to verify proper system functionality.

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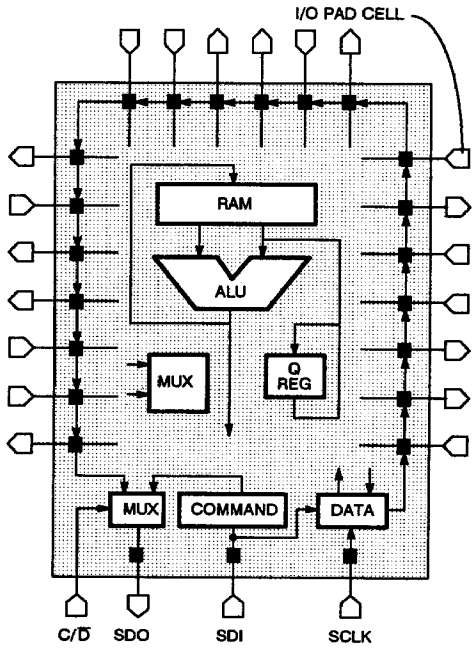

Figure 3. Conceptual Diagram of IDT49C403 Die Incorporating SPC Scan Path

The block diagram in Figure 4 shows the detailed SPC architecture for the IDT49C403. It primarily consists of serial registers for command, data, addresses and decode/control logic. The SPC command register consists of a four-bit field (signals 4-7) and four discrete control lines (signals 3, 2, 1, 0). The four-bit field coordinates the transfer of data between RAM and the SPC data register, as well as controls an on-chip break detect mechanism. The other discrete signals control the serial scan path through the I/O cells.

The SPC data register is in series with a RAM address register and I/O pad scan. The SPC data register is connected to the internal bus to gain access to the RAM register file as well as a data break point feature. The point of connection is the Y bus from the ALU back into the RAM.

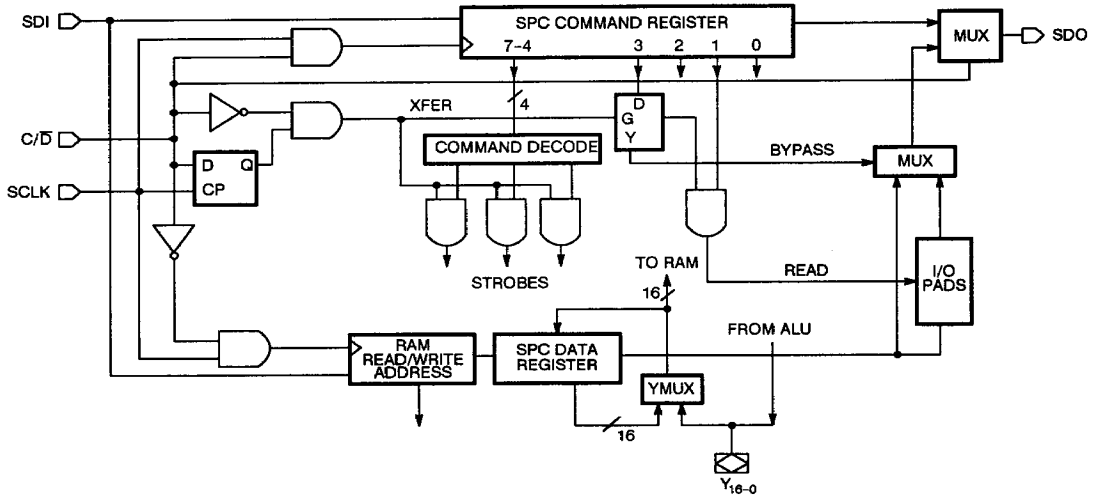

Figure 4. Internal Organization of the SPC

The multiplexer at the output transmits information via the SDO pin selecting data from either the SPC data register and the I/O pads or the command string from the SPC command register.

IDT49C403 SPC Command Opcodes

The SPC command register consists of an 8-bit field, as shown in Figure 5. Bit 1 enables the READ function of the I/O pad cells. Bit 3 enables the BYPASS function to bypass the I/O pad cells and scan out only the RAM address and data registers. Bits 0 and 2 are reserved. Bits 4 through 7 form the opcode field for reading and writing into the device.

The 4-bit command opcode field gives 16 possible command opcodes. The first 8 are reserved for writing data from the SPC data register into the registers and RAM on the device. The second 8 opcodes are reserved for reading data from registers and RAM into the 16-bit SPC data register.

8

COMMAND OPCODES	
OPCODE	**FUNCTION**
0	Write RAM
1	Write Q Registers
2	Write Break Control
3	Write Break Data
4	Reserved
5	Reserved
6	Reserved
7	Reserved
8	Read RAM
9	Read Q Registers
10	Read Break Control
11	Read Break Data
12	View Y
13	Reserved
14	Reserved
15	NOP

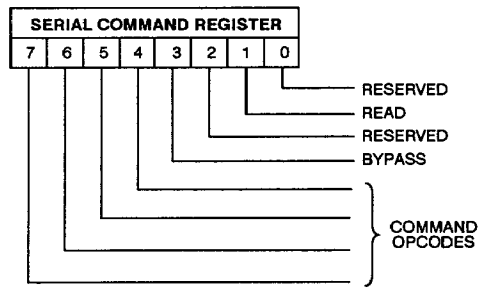

Figure 5. SPC Command Register and Opcodes for the IDT49C403

The command with opcode 0 causes a write to the internal device RAM. Opcode 1 is used to write to the Q registers. Opcodes 2 and 3 are used to write data from SPC data register into the break data register and break control registers, respectively. Opcodes 4 through 7 are reserved opcodes.

Opcode 8 is used for reading RAM data into the SPC data register. Opcode 9 is used to read a value out of the Q registers. (Here, also, the address register supplies the address of the Q register to be accessed). Opcodes 10 and 11 are used for reading the break control register and the break data register, respectively. Opcode 12 is used to strobe data from the Z bus into the 16-bit diagnostics data register. Opcodes 13 and 14 are reserved opcodes. The last opcode, 15, is a no-operation opcode. This opcode can be used to scan the data in and out of the I/O pad cells and use the device in a pass-through mode (in a cascaded application) without affecting normal device operation.

All the reserved opcodes, if executed, perform a no-operation; however, they should not be relied upon to always perform NOPs as future upgrades may make use of reserved opcodes.

Accessing the Contents of the IDT49C403 Register File

To read data from the device's internal RAM or other logic circuitry into the SPC data register, the address and don't care bits (for the SPC data register) are shifted in. The command is shifted into the SPC command register. The command register must be decoded to determine what data paths are to be steered in order to get data into the SPC data register. The read strobe, generated by the strobe logic, must then strobe this data (in parallel) into the SPC data register. The data can now be shifted out via the SDO pin and its contents disassembled and observed.

To perform the write operation, address and data must first be shifted into the SPC data register. The command is then shifted into the SPC command register via the command mode. This register provides information as to what data paths are to be steered. The address is supplied by the address register in the data scan path. The write strobe is then generated between the time the C/$\overline{D}$ line is lowered and the SCLK line is raised. This is the strobe which actually clocks the data into the RAM or register in the device.

Pad Cell Scan Path

Each I/O cell on the IDT49C403 contains a flip-flop which can be used to store the state of that cell and then be scanned out. Figure 6 shows the logic configuration. The READ line is enabled by a bit in the SPC command register and gated by the XFER signal, thus loading the scan flip-flops in parallel. The SCLK is then used to scan the data out of the SDO pin in series with the address and SPC data registers.

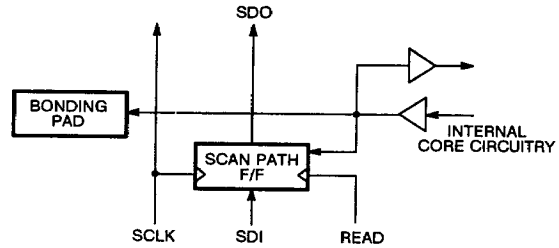

Figure 6. Serial Scan in the I/O Cell

The BYPASS bit in the SPC command register selects whether the shifting of the I/O cells will be bypassed such that only the RAM address and data registers are scanned out. When the READ bit is HIGH, data is transferred from the pins to the scan register when SCLK transitions HIGH after C/D has transitioned LOW. The BYPASS bit in the command register is active HIGH so that a HIGH level bypasses scanning the I/O cells.

Figure 7 shows the order in which the I/O pad cells are scanned. The clocking will shift out the data on the Y_{15} pin first and continue in series until the WRITE pin is shifted out last.

0	Y15
1	Y14
2	Y13
3	Y12
4	Y11
5	Y10
6	Y9
7	Y8
8	QIO15
9	SIO15
10	QIO0
11	SIO0
12	$\overline{OEY}$
13	Z
14	W/$\overline{B}$
15	Y7
16	Y6
17	Y5
18	Y4
19	Y3
20	Y2
21	Y1
22	Y0
23	$\overline{IEN}$
24	$\overline{P}$/N

25	$\overline{G}$/N
26	CN16
27	15
28	16
29	17
30	18
31	DCMP
32	$\overline{MSS}$
33	DB0
34	DB1
35	DB2
36	DB3
37	DB4
38	DB5
39	DB6
40	DB7
41	$\overline{OEB}$
42	CN
43	I0
44	I1
45	I2
46	I3
47	I4
48	DB8
49	DB9

50	DB10
51	DB11
52	DB12
53	DB13
54	DB14
55	DB15
56	$\overline{OEA}$
57	DA0
58	DA1
59	DA2
60	DA3
61	DA4
62	DA5
63	DA6
64	DA7
65	A0
66	A1
67	A2
68	A3
69	A4
70	A5
71	DA8
72	DA9
73	DA10
74	DA11

75	DA12
76	DA13
77	DA14
78	DA15
79	$\overline{LSS}$
80	CP
81	$\overline{WE}$
82	B0
83	B1
84	B2
85	B3
86	B4
87	B5
88	Q0
89	Q1
90	$\overline{WRITE}$

Figure 7. Shift Order of I/O Pad Cells

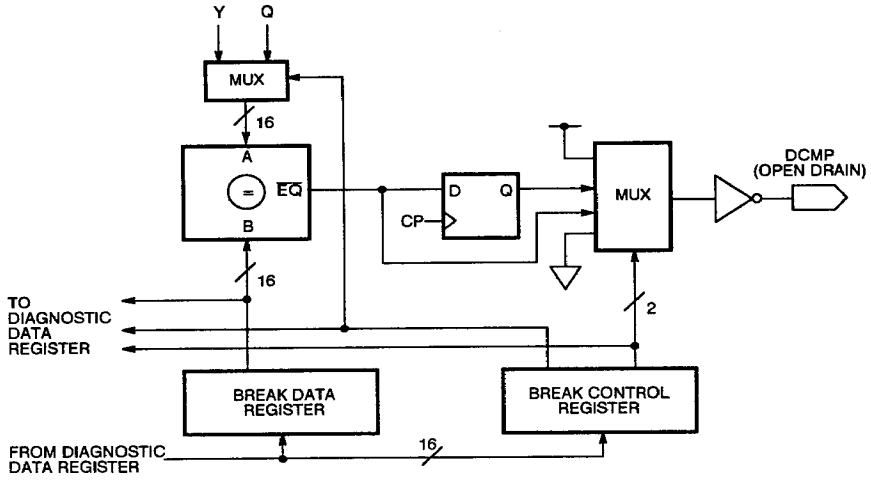

Figure 8. Breakpoint Detect Circuitry

Breakpoint Detection on the IDT49C403

Figure 8 shows the diagnostics breakpoint detection circuit on the IDT49C403. This circuit is designed to allow the user to monitor certain key data buses and detect the data patterns on the Y and Q buses. When a data pattern is detected, a breakpoint compare signal is generated on the DCMP pin and is used to halt the system operation. The DCMP is an open drain signal and should be wire-ORed with DCMP lines of other similar devices and monitored by the main sequencer in the system. The breakpoint detection mechanism thus allows for an easier debug of microcode with regard to the data path.

At the heart of the breakpoint detection circuit is a comparator which compares data from the break data register with data from either the Y bus or the Q bus. The break control register determines which of the two buses is selected for a comparison. The break control register also steers a multiplexer at the output of the comparator. This multiplexer selects between the equal-to signal, latched equal-to, V_{CC} or GND. The latched equal-to input into the multiplexer gives the user the ability to pipeline the match signal, thus shortening the system cycle time in the diagnostics mode. The V_{CC} and GND inputs to the multiplexer allow the programmer to disable the break compare feature by forcing the DCMP pin either LOW or HIGH, respectively.

When a match is made, the DCMP line goes HIGH. Thus, if any one slice in a cascade application does not match, the wire-ANDed DCMP will be low. Selecting V_{CC} via the multiplexer will disable matches altogether. To select GND, disable any one slice from the comparison.

Figure 9 shows the format of the break data and break control register. The break data pattern is 16 bits wide, with bit 16 being the most significant bit and last to be shifted in. The Break Control register contains three fields. Bits 0 and 1 control the DCMP output and bit 2 selects between the Y and the Q bus to be compared with the break data register. Bits 3 to 15 are reserved for future expansion.

BREAK DATA REGISTER FORMAT

15	0
BREAK DATA PATTERN	

BREAK CONTROL REGISTER FORMAT

15 ••• 3	2	1	0
•••	BUS SEL	DCMP CONTROL	

BREAK POINT CONTROL ACCESS

BUS SEL	BUS
0	Y
1	Q

DCMP CONTROL		DCMP STATUS
0	0	LOW
0	1	PIPELINED
1	0	NON-PIPELINED
1	1	HIGH

Figure 9. Breakpoint Control Registers and Opcodes

The SPC version allows data to be transferred into and out of a device and can also accommodate addresses and commands using the same number of pins. This is accomplished with a reconfiguration of the function of the diagnostic pins and internal logic. With this vastly expanded capability, SPC can conveniently be used in RAMs, peripherals an complex logic functions. These new capabilities allow the user to monitor and modify all of the storage elements and pins of a device. With a simple hardware interface and appropriate software, any type personal or mini computer can be turned into a development system for IDT parts with serial diagnostics.

Figure 10 shows the Serial Protocol Channel being used with a writable control store in a microprogrammed design. The control store can be initialized through the SPC path. A register with SPC is used for the instruction register going into the IDT49C410 (16-bit microprogram sequencer) as well as data registers around the IDT49C403. In this way, the designer may use the Serial Protocol Channel to observe and modify the microcode coming out of the writable control store, as well as observing and being able to modify data and instructions in the overall machine.

The block diagram of the diagnostics ring shows how the devices with diagnostics are hooked together in a serial ring via the SDI and SDO signals. The diagnostics signals may be generated through registers which are hooked up to a microprocessor. This microprocessor could conceivably be an IBM PC.

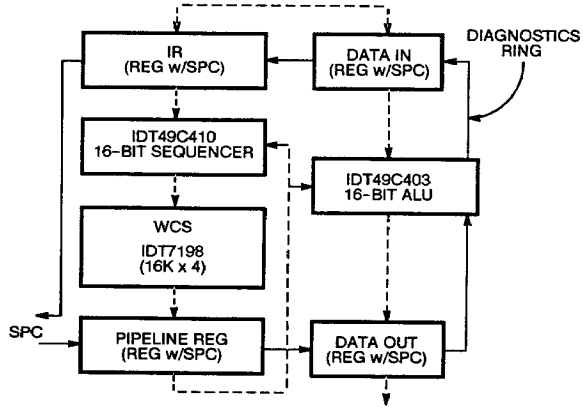

Figure 10. Typical Microprogram Application with SPC

Table 4a. ALU Destination Control (Word Mode) for I_0, I_1, I_2 or I_3 = HIGH, $\overline{IEN}$ = LOW

I_8 I_7 I_6 I_5	ALU SHIFTER FUNCTION	HEX	SIO_{15} SA	SIO_{15} MSS	SIO_{15} IS	SIO_{15} LSS	SIO_0	$\overline{WRITE}$	Q REGISTER AND SHIFTER FUNCTION	QIO_{15}	QIO_0
L L L L	Arith. F/2→Y	0	Input				F_0	L	Hold	Z	Z
L L L H	Log. F/2→Y	1						L	Hold	Z	Z
L L H L	Arith. F/2→Y	2						L	Log. Q/2→Q	Input	Q_0
L L H H	Log. F/2→Y	3						L	Log. Q/2→Q	Input	Q_0
L H L L	F→Y	4					Parity	L	Hold	Z	Z
L H L H	F→Y	5						H	Log. Q/2→Q	Input	Q_0
L H H L	F→Y	6						H	F→Q	Z	Z
L H H H	F→Y	7						L	F→Q	Z	Z
H L L L	Arith. 2F→Y	8	F_{14}	F_{14}	F_{15}	F_{15}	Input	L	Hold	Z	Z
H L L H	Log. 2F→Y	9	F_{15}	F_{15}				L	Hold	Z	Z
H L H L	Arith. 2F→Y	A	F_{14}	F_{14}				L	Log. 2Q→Q	Q_{15}	Input
H L H H	Log. 2F→Y	B	F_{15}	F_{15}				L	Log. 2Q→Q	Q_{15}	Input
H H L L	F→Y	C						H	Hold	Z	Z
H H L H	F→Y	D						H	Log. 2Q→Q	Q_{15}	Input
H H H L	Sign Extend	E		SIO_0	SIO_0			L	Hold	Z	Z
H H H H	F→Y	F		F_{15}	F_{15}			L	Hold	Z	Z

Table 4b. ALU Destination Control (Byte Mode) for I_0, I_1, I_2 or I_3 = HIGH, $\overline{IEN}$ = LOW

I_8 I_7 I_6 I_5	ALU SHIFTER FUNCTION	HEX	SIO_{15} SA	SIO_{15} MSS	SIO_{15} IS	SIO_{15} LSS	SIO_0 SA	SIO_0 MSS	SIO_0 IS	SIO_0 LSS	$\overline{WRITE}$	Q REGISTER AND SHIFTER FUNCTION	QIO_{15} MSS/IS	QIO_{15} SA/LSS	QIO_0 MSS/IS	QIO_0 SA/LSS
L L L L	Arith. F/2→Y	0	Input				F_0	SIO_{15}	SIO_{15}	F_0	L	Hold	Z			
L L L H	Log. F/2→Y	1									L	Hold	Z			
L L H L	Arith. F/2→Y	2									L	Log. Q/2→Q	Input		QIO_{15}	Q_0
L L H H	Log. F/2→Y	3									L	Log. Q/2→Q	Input		QIO_{15}	Q_0
L H L L	F→Y	4					Parity			Parity	L	Hold	Z			
L H L H	F→Y	5									H	Log. Q/2→Q	Input		QIO_{15}	Q_0
L H H L	F→Y	6									H	F→Q	Z			
L H H H	F→Y	7									L	F→Q				
H L L L	Arith. 2F→Y	8	F_8	SIO_0	SIO_0	F_8	Input				L	Hold				
H L L H	Log. 2F→Y	9	F_7			F_7					L	Hold				
H L H L	Arith. 2F→Y	A	F_8			F_8					L	Log. 2Q→Q	QIO_0	Q_7	Input	
H L H H	Log. 2F→Y	B	F_7			F_7					L	Log. 2Q→Q	QIO_0	Q_7	Input	
H H L L	F→Y	C									H	Hold	Z			
H H L H	F→Y	D									H	Log. 2Q→Q	QIO_0	Q_7	Input	
H H H L	Sign Extend	E									L	Hold	Z			
H H H H	F→Y	F									L	Hold	Z			

Parity = $F_{15} \oplus F_{14} \ldots\ldots \oplus F_3 \oplus F_2 \oplus F_1 \oplus F_0 \oplus SIO_{15}$
$\oplus$ = Exclusive OR

L = LOW
H = HIGH
Z = High Impedance

SA = Stand Alone
MSS = Most Significant Slice
IS = Intermediate Slice
LSS = Least Significant Slice

Table 4c. ALU Destination Control for I_0, I_1, I_2 or I_3 = HIGH, $\overline{IEN}$ = LOW

I_8 I_7 I_6 I_5	ALU SHIFTER FUNCTION	HEX	SIO_{15}								Y_{15}								Y_{14}							
			SA		MSS		IS		LSS		SA		MSS		IS		LSS		SA		MSS		IS		LSS	
			Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word
L L L L	Arith. F/2→Y	0	Input →								0	F_{15}	0	F_{15}	0	SIO_{15}	0	SIO_{15}	0	SIO_{15}	0	SIO_{15}	0	F_{15}	0	F_{15}
L L L H	Log. F/2→Y	1										SIO_{15}		SIO_{15}		F_{15}		F_{15}		F_{15}		SIO_{15}		F_{15}		F_{14}
L L H L	Arith. F/2→Y	2										F_{15}		F_{15}		SIO_{15}		SIO_{15}		F_{15}		F_{15}		F_{14}		F_{13}
L L H H	Log. F/2→Y	3										SIO_{15}		SIO_{15}		F_{15}		F_{15}		F_{14}		F_{14}		F_{13}		F_{12}
L H L L	F→Y	4										F_{15}		F_{15}		F_{14}		F_{14}		F_{13}		F_{13}		F_{12}		F_{11}
L H L H	F→Y	5										F_{14}		F_{14}		F_{13}		F_{13}		F_{12}		F_{12}		F_{11}		F_{10}
L H H L	F→Y	6										F_{13}		F_{13}		F_{12}		F_{12}		F_{11}		F_{11}		F_{10}		F_9
L H H H	F→Y	7										F_{12}		F_{12}		F_{11}		F_{11}		F_{10}		F_{10}		F_9		F_8
H L L L	Arith. 2F→Y	8	F_8	F_{14}	SIO_0	F_{14}	SIO_0	F_{15}	F_8	F_{15}		F_{14}		F_{14}		F_{15}		F_{15}		F_{14}		F_{14}		F_{13}		F_{12}
H L L H	Log. 2F→Y	9	F_7	F_{15}		F_{15}		F_{15}	F_7			F_{15}		F_{15}		F_{14}		F_{14}		F_{13}		F_{13}		F_{12}		F_{11}
H L H L	Arith. 2F→Y	A	F_8	F_{14}		F_{14}		F_8				F_{14}		F_{14}		F_{13}		F_{13}		F_{12}		F_{12}		F_{11}		F_{10}
H L H H	Log. 2F→Y	B	F_7	F_{15}		F_{15}		F_7				F_{13}		F_{13}		F_{12}		F_{12}		F_{11}		F_{11}		F_{10}		F_9
H H L L	F→Y	C										F_{12}		F_{12}		F_{11}		F_{11}		F_{10}		F_{10}		F_9		F_8
H H L H	F→Y	D										F_{11}		F_{11}		F_{10}		F_{10}		F_9		F_9		F_8		F_7
H H H L	Sign Extend	E				SIO_0		SIO_0			F_7		SIO_0	SIO_0	SIO_0	SIO_0	F_7		F_7		SIO_0	SIO_0	SIO_0	SIO_0	F_7	
H H H H	F→Y	F				F_{15}		F_{15}			0		0	F_{15}	0	F_{15}	0		0		0	F_{14}	0	F_{14}	0	

Table 4c. ALU Destination Control for I_0, I_1, I_2 or I_3 = HIGH, $\overline{IEN}$ = LOW (cont'd.)

I_8 I_7 I_6 I_5	ALU SHIFTER FUNCTION	HEX	Y_{13-9}								Y_8								Y_7							
			SA		MSS		IS		LSS		SA		MSS		IS		LSS		SA		MSS		IS		LSS	
			Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word
L L L L	Arith. F/2→Y	0	0	F_{i+1}	0	F_{i+1}	0	F_{i+1}	0	F_{i+1}	0	F_9	0	F_9	0	F_9	0	F_9	F_7	F_8	0	F_8	0	F_8	F_7	F_8
L L L H	Log. F/2→Y	1																	SIO_{15}						SIO_{15}	
L L H L	Arith. F/2→Y	2																	F_7						F_7	
L L H H	Log. F/2→Y	3																	SIO_{15}						SIO_{15}	
L H L L	F→Y	4		F_i		F_i		F_i		F_i		F_8		F_8		F_8		F_8	F_7	F_7		F_7		F_7	F_7	F_7
L H L H	F→Y	5																	F_6						F_6	
L H H L	F→Y	6																	F_7						F_7	
L H H H	F→Y	7																	F_6						F_6	
H L L L	Arith. 2F→Y	8		F_{i-1}		F_{i-1}		F_{i-1}		F_{i-1}		F_7		F_7		F_7		F_7	F_6	F_6		F_6		F_6	F_6	F_6
H L L H	Log. 2F→Y	9																	F_6						F_6	
H L H L	Arith. 2F→Y	A																	F_7						F_7	
H L H H	Log. 2F→Y	B																	F_6						F_6	
H H L L	F→Y	C		F_i		F_i		F_i		F_i		F_8		F_8		F_8		F_8	F_7	F_7		F_7		F_7	F_7	F_7
H H L H	F→Y	D				F_i		F_i						F_8		F_8						F_7		F_7		
H H H L	Sign Extend	E	F_7		SIO_0	SIO_0	SIO_0	SIO_0	F_7		F_7		SIO_0	SIO_0	SIO_0	SIO_0	F_7				SIO_0	SIO_0	SIO_0	SIO_0		
H H H H	F→Y	F	0		0	F_i	0	F_i	0		0		0	F_8	0	F_8	0				0	F_7	0	F_7		

Table 4c. ALU Destination Control (cont'd.) for I_0, I_1, I_2 or I_3 = HIGH, $\overline{IEN}$ = LOW

I_8 I_7 I_6 I_5	ALU SHIFTER FUNCTION	HEX	Y_6								Y_{5-1}								Y_0							
			SA		MSS		IS		LSS		SA		MSS		IS		LSS		SA		MSS		IS		LSS	
			Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word
L L L L	Arith. F/2→Y	0	SIO_{15}	F_7	0	F_7	0	F_7	SIO_{15}	F_7	F_{i+1}	F_{i+1}	0	F_{i+1}	0	F_{i+1}	F_{i+1}	F_{i+1}	F_1	F_1	0	F_1	0	F_1	F_1	F_1
L L L H	Log. F/2→Y	1	F_7						F_7																	
L L H L	Arith. F/2→Y	2	SIO_{15}						SIO_{15}																	
L L H H	Log. F/2→Y	3	F_7						F_7																	
L H L L	F→Y	4	F_6	F_6		F_6		F_6	F_6	F_6	F_i	F_i		F_i		F_i	F_i	F_i	F_0	F_0		F_0		F_0	F_0	F_0
L H L H	F→Y	5																								
L H H L	F→Y	6																								
L H H H	F→Y	7																								
H L L L	Arith. 2F→Y	8	F_5	F_5		F_5		F_5	F_5	F_5	F_{i-1}	F_{i-1}		F_{i-1}		F_{i-1}	F_{i-1}	F_{i-1}	SIO_0	SIO_0		SIO_0		SIO_0	SIO_0	SIO_0
H L L H	Log. 2F→Y	9																								
H L H L	Arith. 2F→Y	A																								
H L H H	Log. 2F→Y	B																								
H H L L	F→Y	C	F_6	F_6		F_6		F_6	F_6	F_6	F_i	F_i		F_i		F_i	F_i	F_i	F_0	F_0		F_0		F_0	F_0	F_0
H H L H	F→Y	D				F_6		F_6						F_i		F_i						F_0		F_0		
H H H L	Sign Extend	E			SIO_0	SIO_0	SIO_0	SIO_0					SIO_0	SIO_0	SIO_0	SIO_0					SIO_0	SIO_0	SIO_0	SIO_0		
H H H H	F→Y	F			0	F_6	0	F_6					0	F_i	0	F_i					0	F_0	0	F_0		

i = 1 to 6 (for F_{5-1})
i = 9 to 14 (for F_{13-9})

SA = Stand Alone
MSS = Most Significant Slice
IS = Intermediate Slice
LSS = Least Significant Slice

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Table 4c. ALU Destination Control (cont'd.) for I_0, I_1, I_2 or I_3 = HIGH, $\overline{IEN}$ = LOW

I_8 I_7 I_6 I_5	ALU SHIFTER FUNCTION	HEX	SIO_0							
			SA		MSS		IS		LSS	
			Byte	Word	Byte	Word	Byte	Word	Byte	Word
L L L L	Arith. F/2→Y	0	F_0	F_0	SIO_{15}	F_0	SIO_{15}	F_0	F_0	F_0
L L L H	Log. F/2→Y	1								
L L H L	Arith. F/2→Y	2								
L L H H	Log. F/2→Y	3								
L H L L	F→Y	4	Parity	Parity		Parity		Parity	Parity	Parity
L H L H	F→Y	5								
L H H L	F→Y	6								
L H H H	F→Y	7								
H L L L	Arith. 2F→Y	8	Input →							
H L L H	Log. 2F→Y	9								
H L H L	Arith. 2F→Y	A								
H L H H	Log. 2F→Y	B								
H H L L	F→Y	C								
H H L H	F→Y	D								
H H H L	Sign Extend	E								
H H H H	F→Y	F								

Table 4d. ALU Destination Control for I_0, I_1, I_2 or I_3 = HIGH, $\overline{IEN}$ = LOW

I_8 I_7 I_6 I_5	Q REGISTER AND SHIFTER FUNCTION	HEX	QIO_{15}				Q_{15}				Q_{14-9}				Q_8			
			MSS/IS		SA/LSS		MSS/IS		SA/LSS		MSS/IS		SA/LSS		MSS/IS		SA/LSS	
			Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word
L L L L	Hold	0	Z				Hold				Hold				Hold			
L L L H	Hold	1	Z															
L L H L	Log. Q/2→Q	2	Input				QIO_{15}		QIO_{15}		Q_{i+1}		Q_{i+1}		Q_9		Q_9	
L L H H	Log. Q/2→Q	3	Input				QIO_{15}		QIO_{15}		Q_{i+1}		Q_{i+1}		Q_9		Q_9	
L H L L	Hold	4	Z				Hold		Hold		Hold		Hold		Hold		Hold	
L H L H	Log. Q/2→Q	5	Input				QIO_{15}		QIO_{15}		Q_{i+1}		Q_{i+1}		Q_9		Q_9	
L H H L	F→Q	6	Z				F_{15}		F_{15}		F_i		F_i		F_8		F_8	
L H H H	F→Q	7					F_{15}		F_{15}		F_i		F_i		F_8		F_8	
H L L L	Hold	8					Hold		Hold		Hold		Hold		Hold		Hold	
H L L H	Hold	9					Hold		Hold		Hold		Hold		Hold		Hold	
H L H L	Log. 2Q→Q	A	QIO_0	Q_{15}	Q_7	Q_{15}	Q_{14}		Q_{14}		Q_{i-1}		Q_{i-1}		Q_7		Q_7	
H L H H	Log. 2Q→Q	B	QIO_0	Q_{15}	Q_7	Q_{15}	Q_{14}		Q_{14}		Q_{i-1}		Q_{i-1}		Q_7		Q_7	
H H L L	Hold	C	Z				Hold		Hold		Hold		Hold		Hold		Hold	
H H L H	Log. 2Q→Q	D	QIO_0	Q_{15}	Q_7	Q_{15}	Q_{14}		Q_{14}		Q_{i-1}		Q_{i-1}		Q_7		Q_7	
H H H L	Hold	E	Z				Hold		Hold		Hold		Hold		Hold		Hold	
H H H H	Hold	F	Z				Hold		Hold		Hold		Hold		Hold		Hold	

Table 4d. ALU Destination Control for I_0, I_1, I_2 or I_3 = HIGH, $\overline{IEN}$ = LOW (cont'd.)

I_8 I_7 I_6 I_5	Q REGISTER AND SHIFTER FUNCTION	HEX	Q_7				Q_{6-1}				Q_0				QIO_0			
			MSS/IS		SA/LSS		MSS/IS		SA/LSS		MSS/IS		SA/LSS		MSS/IS		SA/LSS	
			Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word	Byte	Word
L L L L	Hold	0	Hold				Hold				Hold				Z			
L L L H	Hold	1													Z			
L L H L	Log. Q/2→Q	2	Q_8	QIO_{15}	Q_8		Q_{i+1}				Q_1				QIO_{15}	Q_0		
L L H H	Log. Q/2→Q	3	Q_8	QIO_{15}	Q_8		Q_{i+1}				Q_1				QIO_{15}	Q_0		
L H L L	Hold	4	Hold				Hold				Hold				Z			
L H L H	Log. Q/2→Q	5	Q_8	QIO_{15}	Q_8		Q_{i+1}				Q_1				QIO_{15}	Q_0		
L H H L	F→Q	6	F_7				F_i				F_0				Z			
L H H H	F→Q	7	F_7				F_i				F_0							
H L L L	Hold	8	Hold				Hold				Hold							
H L L H	Hold	9	Hold				Hold				Hold							
H L H L	Log. 2Q→Q	A	Q_6				Q_{i-1}				QIO_0				Input			
H L H H	Log. 2Q→Q	B	Q_6				Q_{i-1}				QIO_0				Input			
H H L L	Hold	C	Hold				Hold				Hold				Z			
H H L H	Log. 2Q→Q	D	Q_6				Q_{i-1}				QIO_0				Input			
H H H L	Hold	E	Hold				Hold				Hold				Z			
H H H H	Hold	F	Hold				Hold				Hold				Z			

Parity = F_{15} ⊕ F_{14} ..... ⊕ F_3 ⊕ F_2 ⊕ F_1 ⊕ F_0 ⊕ SIO_{15}
⊕ = Exclusive OR

i = 1 to 6 (for Q_{6-1})
i = 9 to 14 (for Q_{14-9})

Z = High Impedance
SA = Stand Alone
MSS = Most Significant Slice
IS = Intermediate Slice
LSS = Least Significant Slice

Table 5. Special Functions [7]

HEX I_8 I_7 I_6 I_5	I_4	HEX I_3 I_2 I_1 I_0	SPECIAL FUNCTION	ALU FUNCTION	ALU SHIFTER FUNCTION	SIO_{15}		SIO_0	Q REGISTER & SHIFTER FUNCTION	QIO_{15}	QIO_0	$\overline{WRITE}$
						MSS	OTHER SLICES					
0	L	0	Unsigned Multiply	F=S+C_n if Z=L F=R+S+C_n if Z=H	Log F/2→Y (1)	HZ	Input	F_0	Log Q/2→Q	Input	Q_0	L
1	L	0	BCD-to-Binary Conversion	(4)	Log F/2→Y	Input	Input	F_0	Log Q/2→Q	Input	Q_0	L
1	H	0	Multiprecision BCD-to-Binary	(4)	Log F/2→Y	Input	Input	F_0	Hold	HZ	Q_0	L
2	L	0	Two's Complement Multiply	F=S+C_n if Z=L F=R+S+C_n if Z=H	Log F/2→Y (2)	HZ	Input	F_0	Log Q/2→Q	Input	Q_0	L
3	L	0	Decrement by One or Two	F=S−2+C_n	F→Y	Input	Input	Parity	Hold	HZ	HZ	L
4	L	0	Increment by One or Two	F=S+1+C_n	F→Y	Input	Input	Parity	Hold	HZ	HZ	L
4	H	0	Byte Swap + C_n	F=(S_{LB}, S_{UB})+C_n	F→Y	Input	Input	Parity	Hold	HZ	HZ	L
5	L	0	Sign/Magnitude Two's Complement	F=S+C_n if Z=L F=$\overline{S}$+C_n if Z=H	F/2→Y (3)	Input	Input	Parity	Hold	HZ	HZ	L
6	L	0	Two's Complement Multiply, Last Cycle	F=S+C_n if Z=L F=S−R−1+C_n if Z=H	Log F/2→Y (2)	HZ	Input	F_0	Log Q/2→Q	Input	Q_0	L
7	L	0	BCD Divide by Two	(4)	F→Y	Input	Input	Parity	Hold	HZ	HZ	L
8	L	0	Single Length Normalize	F=S+C_n	F→Y	F_{15}	F_{15}	HZ	Log 2Q→Q	Q_{15}	Input	L
9	L	0	Binary-to-BCD Conversion	(5)	Log 2F→Y	F_{15}	F_{15}	Input	Log 2Q→Q	Q_{15}	Input	L
9	H	0	Multiprecision Binary-to-BCD	(5)	Log 2F→Y	F_{15}	F_{15}	Input	Hold	HZ	Input	L
A	L	0	Double Length Normalize and First Divide Op	F=S+C_n	Log 2F→Y	R_{15} V F_{15}	F_{15}	Input	Log 2Q→Q	Q_{15}	Input	L
B	L	0	BCD Add	F=R+S+C_n BCD [6]	F→Y	0	0	HZ	Hold	HZ	HZ	L
C	L	0	Two's Complement Divide	F=S+R+C_n if Z=L F=S−R−1+C_n if Z=H	Log 2F→Y	R_{15} V F	F_{15}	Input	Log 2Q→Q	Q_{15}	Input	L
D	L	0	BCD Subtract	F=R−S−1+C_n BCD [6]	F→Y	0	0	HZ	Hold	HZ	HZ	L
E	L	0	Two's Complement Divide Correction and Remainder	F=S+R+C_n if Z=L F=S−R−1+C_n if Z=H	F→Y	F_{15}	F_{15}	HZ	Log 2Q→Q	Q_{15}	Input	L
F	L	0	BCD Subtract	F=S−R−1+C_nBCD [6]	F→Y	0	0	HZ	Hold	HZ	HZ	L

NOTES:

1. At the most significant slice only, the C_{n+16} signal is internally gated to the Y output.
2. At the most significant slice only, F_{15} ⊽ OVR is internally gated to the Y output.
3. At the most significant slice only, S_{15} ⊽ F_{15} is generated at the Y output.
4. On each nibble, F = S if magnitude of S is less than 8, and F = S minus three if magnitude of S is 8 or greater.
5. On each nibble, F = S if magnitude of S is less than 5, and F = S plus three if magnitude of S is 5 or greater. Addition is modulo 16.
6. Additions and Subtractions are BCD adds and subtracts. Results are undefined if R or S are not in valid BCD format.
7. The Q register cannot be used explicitly as an operand for any Special Functions. It is defined implicitly within the functions.
8. BCD Nibble propagate: $\overline{PN}_I = (\overline{P}_{4I+0} + \overline{P}_{4I+3})\,(\overline{P}_{4I+0} + \overline{G}_{4I+2})\,(\overline{P}_{4I+0} + \overline{G}_{4I+1} + \overline{P}_{4I+2})$
   BCD Slice propage: $P = PN_3\,PN_2\,PN_1\,PN_0$
9. BCD Nibble generate: $\overline{GN}_I = \overline{G}_{4I+3}\,(\overline{G}_{4I+0} + \overline{G}_{4I+1} + \overline{P}_{4I+2})\,(\overline{G}_{4I+0} + \overline{G}_{4I+1})\,(\overline{P}_{4I+1} + \overline{G}_{4I+2})\,(\overline{P}_{4I+3} + \overline{P}_{4I+1} \cdot \overline{P}_{4I+2} \cdot \overline{G}_{4I+0})$
   BCD Slice generate: $G = GN_3\ V\ GN_2\,PN_3\ V\ GN_1\,PN_2\,PN_3\ V\ GN_0\,PN_1\,PN_2\,PN_3$

L = LOW LB = Lower Byte ⊽ = Exclusive OR
H = HIGH UB = Upper Byte Parity = SIO_{15} ⊽ F_{15} ⊽ F_{14} ⊽ F_{13} ⊽ ..... ⊽ F_0
HZ = High Impedance

Table 6a. IDT49C403 Status Outputs (Word Mode)

HEX $I_8\ I_7\ I_6\ I_5$	HEX $I_4\ I_3\ I_2\ I_1$	I_0	G_i (i = 0 to 15)	P_i (i = 0 to 15)	C_{n+15}	$\overline{P}$/OVR		$\overline{G}$/N		Z ($\overline{OEY}$ = L)			
						MSS/SA	OTHER SLICES	MSS/SA	OTHER SLICES	MSS	ISS	LSS	SA
X	0	H	0	1	0	0	0	F_{15}	$\overline{G}$	f (Y)	f (Y)	f (Y)	f (Y)
X	1	X	$\overline{Ri} \wedge Si$	$\overline{Ri} \vee SI$	G V PC_n	$C_{n+15} \veebar C_{n+16}$	$\overline{P}$	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	2	X	$\overline{Ri} \wedge Si$	$Ri \vee SI$	G V PC_n	$C_{n+15} \veebar C_{n+16}$	$\overline{P}$	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	3	X	$\overline{Ri} \wedge Si$	$Ri \vee Si$	G V PC_n	$C_{n+15} \veebar C_{n+16}$	$\overline{P}$	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	4	X	0	Si	G V PC_n	$C_{n+15} \veebar C_{n+16}$	$\overline{P}$	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	5	X	0	$\overline{Si}$	G V PC_n	$C_{n+15} \veebar C_{n+16}$	$\overline{P}$	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	6	X	0	$\overline{Ri}$	G V PC_n	$C_{n+15} \veebar C_{n+16}$	$\overline{P}$	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	7	X	0	$\overline{Ri}$	G V PC_n	$C_{n+15} \veebar C_{n+16}$	$\overline{P}$	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	8	H	0	1	0	0	0	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	9	X	$\overline{Ri} \wedge Si$	1	0	0	0	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	A	X	$Ri \wedge Si$	$Ri \vee Si$	0	0	0	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	B	X	$\overline{Ri} \wedge Si$	$\overline{Ri} \vee Si$	0	0	0	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	C	X	$Ri \wedge Si$	1	0	0	0	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	D	X	$\overline{Ri} \wedge \overline{Si}$	1	0	0	0	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	E	X	$Ri \wedge Si$	1	0	0	0	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	F	X	$\overline{Ri} \wedge \overline{Si}$	1	0	0	0	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
0	0	L	0 if Z = L $Ri \wedge Si$ if Z = H	Si if Z = L $Ri \vee Si$ if Z = H	G V PC_n	$C_{n+15} \veebar C_{n+16}$	$\overline{P}$	F_{15}	$\overline{G}$	Input	Input	Q_0	Q_0
1	0	L	0	Si	G V PC_n	$C_{n+15} \veebar C_{n+16}$	$\overline{P}$	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
1	8	L	0	Si	0	0	0	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
2	0	L	0 if Z = L $Ri \wedge Si$ if Z = H	Si if Z = L $Ri \vee Si$ if Z = H	G V PC_n	$C_{n+15} \veebar C_{n+16}$	$\overline{P}$	F_{15}	$\overline{G}$	Input	Input	Q_0	Q_0
3	0	L	(6)	(7)	G V PC_n	$C_{n+15} \veebar C_{n+16}$	$\overline{P}$	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
4	0	L	(1)	(2)	G V PC_n	$C_{n+15} \veebar C_{n+16}$	$\overline{P}$	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
4	8	L	(1)	(2)	G V PC_n	$C_{n+15} \veebar C_{n+16}$	$\overline{P}$	F_{15}	$\overline{G}$	f(Y)	f(Y)	f(Y)	f(Y)
5	0	L	0	$\overline{Si}$ if Z = L $\overline{Si}$ if Z = H	G V PC_n	$C_{n+15} \veebar C_{n+16}$	$\overline{P}$	F_{15} if Z = L $F_{15} \veebar S_{15}$ if Z = H	$\overline{G}$	S_{15}	Input	Input	S_{15}
6	0	L	0 if Z = L $\overline{Ri} \wedge Si$ if Z = H	Si if Z = L $\overline{Ri} \vee Si$ if Z = H	G V PC_n	$C_{n+15} \veebar C_{n+16}$	$\overline{P}$	F_{15}	$\overline{G}$	Input	Input	Q_0	Q_0
7	0	L	0	Si	G V PC_n	$C_{n+15} \veebar C_{n+16}$	$\overline{P}$	F_{15}	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
8	0	L	0	Si	(4)	$Q_2 \veebar Q_1$	$\overline{P}$	Q_{15}	$\overline{G}$	f (Q)	f (Q)	f (Q)	f (Q)
9	0	L	0	Si	G V PC_n	$C_{n+15} \veebar C_{n+16}$	$\overline{P}$	F_{15}	$\overline{G}$	f (Q)	f (Q)	f (Q)	f (Q)
9	8	L	0	Si	0	0	0	F_{15}	$\overline{G}$	f (Q)	f (Q)	f (Q)	f (Q)
A	0	L	0	Si	(3)	$F_2 \veebar F_1$	$\overline{P}$	F_{15}	$\overline{G}$	(5)	(5)	(5)	(5)
B	0	L	$Ri \wedge Si$	$Ri \vee Si$	G V PC_n	(8)	(8)	F_{15}	(9)	f(Y)	f (Y)	f (Y)	f (Y)
C	0	L	$Ri \wedge Si$ if Z = L $\overline{Ri} \wedge Si$ if Z = H	$Ri \vee Si$ if Z = L $\overline{Ri} \vee Si$ if Z = H	G V PC_n	$C_{n+15} \veebar C_{n+16}$	$\overline{P}$	F_{15}	$\overline{G}$	Sign Compare FF Output	Input	Input	Sign Compare FF Output
D	0	L	$Ri \wedge \overline{Si}$	$Ri \vee \overline{Si}$	G V PC_n	$C_{n+15} \veebar C_{n+16}$	(8)	F_{15}	(9)	f(Y)	f (Y)	f (Y)	f (Y)
E	0	L	$Ri \wedge Si$ if Z = L $\overline{Ri} \wedge Si$ if Z = H	$Ri \vee Si$ if Z = L $\overline{Ri} \vee Si$ if Z = H	G V PC_n	$C_{n+15} \veebar C_{n+16}$	$\overline{P}$	F_{15}	$\overline{G}$	Sign Compare FF Output	Input	Input	Sign Compare FF Output
F	0	L	$\overline{Ri} \wedge Si$	$\overline{Ri} \vee Si$	G V PC_n	$C_{n+15} \veebar C_{n+16}$	(8)	F_{15}	(9)	f(Y)	f (Y)	f (Y)	f (Y)

Continued next page

NOTES:

1. If $\overline{LSS}$ is LOW, $G_0 = S_0$ and $G_{1,2,3,\ldots,15} = 0$. If $\overline{LSS}$ is HIGH, $G_{0,1,2,3,\ldots,15} = 0$
2. If $\overline{LSS}$ is LOW, $P_0 = 1$ and $P_{1,2,3,\ldots,15} = S_{1,2,3,\ldots,15}$. If $\overline{LSS}$ is HIGH, $P_I = S_I$
3. At the most significant slice, $C_{n+16} = Q_{15} \forall Q_{14}$. At other slices $C_{n+16} = G \vee PC_n$
4. At the most significant slice, $C_{n+16} = F_{15} \forall F_{14}$. At other slices $C_{n+16} = G \vee PC_n$
5. $Z = \overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3 \ldots \overline{Q}_{15}\overline{F}_0\overline{F}_1\overline{F}_2\overline{F}_3 \ldots \overline{F}_{15}$
6. If $\overline{LSS}$ is LOW, $G_0 = 0$ and $G_{1,2,3,\ldots,15} = S_{1,2,3,\ldots,15}$. If $\overline{LSS}$ is HIGH, $G_{0,1,2,3,\ldots,15} = S_{0,1,2,3,\ldots,15}$
7. If $\overline{LSS}$ is LOW, $P_0 = S_0$ and $P_{1,2,3,\ldots,15} = 1$. If $\overline{LSS}$ is HIGH, $P_{0,1,2,3,\ldots,15} = 1$
8. BCD Nibble propagate: $\overline{PN}_I = (\overline{P}_{4I+0} + \overline{P}_{4I+3})(\overline{P}_{4I+0} + \overline{G}_{4I+2})(\overline{P}_{4I+0} + \overline{G}_{4I+1} + \overline{P}_{4I+2})$
   BCD Slice propagate: $P = PN_3\,PN_2\,PN_1\,PN_0$
9. BCD Nibble generate: $\overline{GN}_I = \overline{G}_{4I+3}(\overline{G}_{4I+0} + \overline{G}_{4I+1} + \overline{P}_{4I+2})(\overline{G}_{4I+0} + \overline{G}_{4I+1})(\overline{P}_{4I+1} + \overline{G}_{4I+2})(\overline{P}_{4I+3} + \overline{P}_{4I+1} \cdot \overline{P}_{4I+2} \cdot \overline{G}_{4I+0})$
   BCD Slice generate: $G = GN_3 \vee GN_2\,PN_3 \vee GN_1\,PN_2\,PN_3 \vee GN_0\,PN_1\,PN_2\,PN_3$

V = OR
Λ = AND
$\forall$ = Exclusive-OR
$P = P_{15}P_{14} \ldots\ldots P_3P_2P_1P_0$
$G = G_{15} \vee G_{14}P_{15} \vee G_{13}P_{14}P_{15} \vee G_{12}P_{13}P_{14}P_{15} \vee G_{11}P_{12}P_{13}P_{14}P_{15} \vee \ldots\ldots \vee G_1P_2P_3P_4 \ldots P_{15}$

$f(Y) = \overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3 \ldots\ldots \overline{Y}_{15}$
$f(Q) = \overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3 \ldots\ldots \overline{Q}_{15}$
L = LOW = 0
H = HIGH = 1

Table 6b. IDT49C403 Status Outputs (Byte Mode)

HEX $I_8\,I_7\,I_6\,I_5$	HEX $I_4\,I_3\,I_2\,I_1$	I	Q_I (I=0 to 7)	P_I (I=0 to 7)	C_{n+7}	$\overline{P}$/OVR		$\overline{G}$/N		Z ($\overline{OEY}$ = L)			
						MSS/SA	OTHER SLICES	MSS/SA	OTHER SLICES	MS	ISS	LSS	SA
X	0	H	0	1	0	0	0	F_7	$\overline{G}$	f (Y)	f (Y)	f (Y)	f (Y)
X	1	X	$\overline{Ri} \wedge Si$	$\overline{Ri} \vee Si$	$G \vee PC_n$	$C_{n+7} \forall C_{n+8}$	$\overline{P}$	F_7	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	2	X	$\overline{Ri} \wedge Si$	$Ri \vee SI$	$G \vee PC_n$	$C_{n+7} \forall C_{n+8}$	$\overline{P}$	F_7	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	3	X	$\overline{Ri} \wedge Si$	$Ri \vee Si$	$G \vee PC_n$	$C_{n+7} \forall C_{n+8}$	$\overline{P}$	F_7	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	4	X	0	Si	$G \vee PC_n$	$C_{n+7} \forall C_{n+8}$	$\overline{P}$	F_7	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	5	X	0	$\overline{Si}$	$G \vee PC_n$	$C_{n+7} \forall C_{n+8}$	$\overline{P}$	F_7	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	6	X	0	Ri	$G \vee PC_n$	$C_{n+7} \forall C_{n+8}$	$\overline{P}$	F_7	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	7	X	0	$\overline{Ri}$	$G \vee PC_n$	$C_{n+7} \forall C_{n+8}$	$\overline{P}$	F_7	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	8	H	0	1	0	0	0	F	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	9	X	$\overline{Ri} \wedge Si$	1	0	0	0	F	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	A	X	$Ri \wedge Si$	$Ri \vee Si$	0	0	0	F	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	B	X	$\overline{Ri} \wedge Si$	$\overline{Ri} \vee Si$	0	0	0	F	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	C	X	$Ri \wedge Si$	1	0	0	0	F	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	D	X	$\overline{Ri} \wedge \overline{Si}$	1	0	0	0	F	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	E	X	$Ri \wedge Si$	1	0	0	0	F	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)
X	F	X	$\overline{Ri} \wedge \overline{Si}$	1	0	0	0	F	$\overline{G}$	f(Y)	f (Y)	f (Y)	f (Y)

NOTES:

$f(Y) = \overline{Y}_0\overline{Y}_1\overline{Y}_2\overline{Y}_3 \ldots\ldots \overline{Y}_7$
$f(Q) = \overline{Q}_0\overline{Q}_1\overline{Q}_2\overline{Q}_3 \ldots\ldots \overline{Q}_7$
L = LOW = 0
H = HIGH = 1

V = OR
Λ = AND
$\forall$ = Exclusive OR
$P = P_7P_6 \ldots\ldots P_3P_2P_1P_0$
$G = G_7 \vee G_6P_7 \vee G_5P_6P_7 \vee G_4P_5P_6P_7 \vee G_3P_4P_5P_6P_7 \vee \ldots\ldots \vee G_1P_2P_3P_4 \ldots P_7$

8

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.5	1.5	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER (1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	15	pF

NOTE:

1. This parameter is sampled and not 100% tested.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level (4)			2.0	–	–	V
V_{IL}	Input LOW Level (4)			–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		–	0.1	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0V		–	-0.1	-5	µA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	V
			I_{OH} = -6mA MIL.	2.4	4.3	–	
			I_{OH} = -8mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	V
			I_{OL} = 12mA MIL.	–	0.3	0.5	
			I_{OL} = 16mA COM'L.	–	0.3	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0V	–	–	-40	µA
			V_O = V_{CC} (max.)	–	–	40	
I_{OS}	Output Short Circuit Current	V_{CC} = Min., V_{OUT} = 0V (3)		-15	–	–	mA

NOTES:

1. For conditions shown as max. or min. use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. These input levels provide zero noise immunity and should only be static tested in a noise-free environment. Guaranteed by Design.

DC ELECTRICAL CHARACTERISTICS (Cont'd)

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQH}	Quiescent Power Supply Current CP = H (CMOS Inputs)	V_{CC} = Max. $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$ f_{CP} = 0, CP = H		–	150	250	mA
I_{CCQL}	Quiescent Power Supply Current CP = L (CMOS Inputs)	V_{CC} = Max. $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$ f_{CP} = 0, CP = L		–	50	100	mA
I_{CCT}	Quiescent Input Power Supply [5] Current (per Input @ TTL High)	V_{CC} = Max. V_{IN} = 3.4V, f_{CP} = 0		–	0.3	0.5	mA/Input
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$ Outputs Open, $\overline{OE}$ = L	MIL.	–	3.6	7.7	mA/MHz
			COM'L.	–	3.6	5.2	
I_{CC}	Total Power Supply Current [6]	V_{CC} = Max., f_{CP} = 10MHz Outputs Open, $\overline{OE}$ = L CP = 50% Duty cycle $V_{HC} \le V_{IN}$, $V_{IN} \le V_{LC}$	MIL.	–	136	252	mA
			COM'L.	–	136	227	
		V_{CC} = Max., f_{CP} = 10MHz Outputs Open, $\overline{OE}$ = L CP = 50% Duty cycle V_{IH} = 3.4V, V_{IL} = 0.4V	MIL.	–	150	275	
			COM'L.	–	150	250	

NOTES:

5. I_{CCT} is derived by measuring the total current with all the inputs tied together at 3.4V, subtracting out I_{CCQH}, then dividing by the total number of inputs.
6. Total Supply Current is the sum of the Quiescent current and the Dynamic current (at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:

$$I_{CC} = I_{CCQH}(CD_H) + I_{CCQL}(1 - CD_H) + I_{CCT}(N_T \times D_H) + I_{CCD}(f_{CP})$$

CD_H = Clock duty cycle high period.
D_H = Data duty cycle TTL high period (V_{IN} = 3.4V).
N_T = Number of dynamic inputs driven at TTL levels.
f_{CP} = Clock input frequency.

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IDT49C403A GUARANTEED COMMERCIAL AND MILITARY RANGE PERFORMANCE

The tables below specify the guaranteed performance of the IDT49C403A over the commercial operating range of 0 to +70°C with V_{CC} from 4.75 to 5.25V, and over the military operating range of −55 to +125°C with V_{CC} from 4.5 to 5.5V. All data are in nanoseconds, with input switching between 0 and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

Table 7. Clock and Write Pulse Characteristics All Functions

	COM'L	MIL	UNIT
Minimum Clock Low Time	10	11	ns
Minimum Clock High Time	10	11	ns
MInimum Time CP and WE both Low to Write	10	11	ns

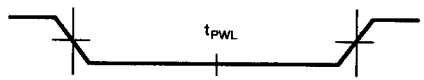
NOTE:
Guaranteed by Design.

Table 8. Enable/Disable Times All Functions

FROM	TO	ENABLE COM'L	ENABLE MIL	DISABLE COM'L	DISABLE MIL	UNIT
$\overline{OE}_Y$	Y	12	20	10	12	ns
$\overline{OE}_B$	DB	14	22	12	13	ns
$\overline{OE}_A$	DA	15	22	13	14	ns
I_8	SIO	23	25	12	13	ns
I_8	QIO	16	24	21	22	ns
$I_{8, 7, 6, 5}$	QIO	17	28	19	22	ns
$I_{4, 3, 2, 1, 0}$	QIO	21	31	19	22	ns

NOTE:
C_L = 5.0pF for output disable tests. Measurement is made to a 0.5V change on the output.

Table 9. Set-up and Hold Times All Functions



FROM	WITH RESPECT TO	SET-UP COM'L	SET-UP MIL	HOLD COM'L	HOLD MIL	SET-UP COM'L	SET-UP MIL	HOLD COM'L	HOLD MIL	UNIT	COMMENTS
Y	CP	–	–	–	–	8	9	2	2	ns	Store Y in RAM/Q (1)
$\overline{WE}$ HIGH	CP	7	8	2	2	–	–	2	2	ns	Prevent Writing
$\overline{WE}$ LOW	CP	–	–	–	–	10	11	0	0	ns	Write into RAM
A, B Source	CP	11	12	2	2	–	–	–	–	ns	Latch Data from RAM Out
B Destination (3)	CP	6	7	(3)	(3)	(3)	(3)	2	2	ns	Write Data into B Address
B Destination (3)	$\overline{IEN}$	6	7	(3)	(3)	(3)	(3)	2	2	ns	Write Data into B Address
B Destination (3)	$\overline{WE}$	6	7	(3)	(3)	(3)	(3)	2	2	ns	Write Data into B Address
$QIO_{0, 15}$	CP	–	–	–	–	5	6			ns	Shift Q
$I_{8, 7, 6, 5}$	CP	–	–	–	–	23	25	0	0	ns	Write into Q and RAM (2)
$\overline{IEN}$ HIGH (3)	CP	7	8	(3)		–	–			ns	Prevent Writing into Q and RAM (2)
$\overline{IEN}$ LOW (3)	CP	–	–	–	–	10	11			ns	Write into Q and RAM
$I_{4, 3, 2, 1, 0}$	CP	–	–	–	–	16	18			ns	Write into Q and RAM (2)
Q_0, Q_1	CP	–	–	–	–	8	9	2	2	ns	Write into Q
C_n	CP	–	–	–	–	28	30	0	0	ns	ALU Carry In to RAM

NOTES:
1. The internal Y-bus to RAM set-up condition will be met 5ns after valid Y output ($\overline{OE}_Y$ = 0)
2. The set-up time with respect to CP falling edge is to prevent writing. The set-up time with respect to CP rising edge is to enable writing.
3. The writing of data is controlled by CP, $\overline{IEN}$, and $\overline{WE}$; all must be LOW in order to write. The set-up time of B destination address is with respect to the last of these three inputs to go LOW, and the hold time is with respect to the first to go HIGH.
4. A "–" implies this path does not exist.

IDT49C403A GUARANTEED COMMERCIAL AND MILITARY RANGE PERFORMANCE STANDARD AND INCREMENT (SF-4) /DECREMENT (SF-3) BY ONE OR TWO INSTRUCTIONS

FROM	TO: SLICE	Y Com'l.	Y Mil.	$C_{n=16}$ Com'l.	$C_{n=16}$ Mil.	$\overline{G}, \overline{P}$ Com'l.	$\overline{G}, \overline{P}$ Mil.	Z Com'l.	Z Mil.	N Com'l.	N Mil.	OVR Com'l.	OVR Mil.	DA, DB Com'l.	DA, DB Mil.	$\overline{WRITE}$ Com'l.	$\overline{WRITE}$ Mil.	$QIO_{0,15}$ Com'l.	$QIO_{0,15}$ Mil.	SIO_0 Com'l.	SIO_0 Mil.	SIO_{15} Com'l.	SIO_{15} Mil.	SIO_0 PARITY Com'l.	SIO_0 PARITY Mil.	UNITS
A, B Addr	Any	41	48	44	48	44	48	42	45	47	58	47	57	26	33	–	–	–	–	41	48	40	48	52	56	ns
DA, DB	Any	34	38	28	33	28	34	29	31	36	42	34	40	–	–	–	–	–	–	24	29	27	33	46	50	ns
C_n	Any	27	35	15	19	–	–	22	24	26	29	23	28	–	–	–	–	–	–	24	29	26	30	26	30	ns
I_{8-0}	Any	38	43	32	34	23	35	48	51	36	38	42	45	–	–	18	25	24	27	28	38	37	40	41	50	ns
CP	Any	43	46	44	48	39	42	39	42	51	55	54	58	20	25	–	–	26	30	36	39	37	40	41	45	ns
MSS	Any	21	35	–	–	21	23	38	43	21	25	20	23	–	–	–	–	–	–	–	–	20	23	–	–	ns
$SIO_{0,15}$	Any	21	27	–	–	–	–	17	19	–	–	–	–	–	–	–	–	–	–	–	–	19	23	16	20	ns

MULTIPLY INSTRUCTIONS (SF-0, 2 & 6)

FROM	TO: SLICE	Y Com'l.	Y Mil.	$C_{n=16}$ Com'l.	$C_{n=16}$ Mil.	$\overline{G}, \overline{P}$ Com'l.	$\overline{G}, \overline{P}$ Mil.	Z Com'l.	Z Mil.	N Com'l.	N Mil.	OVR Com'l.	OVR Mil.	DA, DB Com'l.	DA, DB Mil.	$\overline{WRITE}$ Com'l.	$\overline{WRITE}$ Mil.	$QIO_{0,15}$ Com'l.	$QIO_{0,15}$ Mil.	SIO_0 Com'l.	SIO_0 Mil.	UNITS
A, B Addr	Any	49	58	53	58	53	58	–	–	56	70	56	68	31	40	–	–	–	–	49	58	ns
DA, DB	Any	41	46	34	40	34	41	–	–	43	50	41	48	–	–	–	–	–	–	29	35	ns
C_n	Any	32	42	18	23	–	–	–	–	31	35	28	34	–	–	–	–	–	–	29	35	ns
I_{8-0}	Any	46	52	38	41	28	42	58	61	43	46	50	54	–	–	22	30	29	32	34	46	ns
CP	Any	52	55	53	58	47	50	–	–	61	66	65	70	24	30	–	–	31	36	43	47	ns
Z ($\overline{OE}_Y$ = low)	Any	47	48					–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns
$SIO_{0,15}$	Any	25	32	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns

Unsigned Multiply

SF 0: F=S+C_n if Z=L
F=S+R+C_n if Z=H
Y15=C_n+16 (MSS)
Z=Q0 (LSS)
Y=Log F/2
Q=Log Q/2

Two's Complement Multiply

SF 2: F=S+C_n if Z=L
F=S+R+C_n if Z=H
Y15=F15 V OVR (MSS)
Z=Q0 (LSS)
Y=Log F/2
Q=Log Q/2

Two's Complement Multiply Last Cycle

SF 6: F=S+C_n if Z=L
F=S−R−1+C_n if Z=H
Y15=OVR V F15 (MSS)
Z=Q0 (LSS)
Y=Log F/2
Q=Log Q/2

NOTES:
1. A "–" means the delay path does not exist.
2. An "*" means the output may be enabled or disabled by the input; refer to function table.
3. This specification is not tested.

IDT49C403A GUARANTEED COMMERCIAL AND MILITARY RANGE PERFORMANCE
BCD INSTRUCTIONS (SF-1, 7, 9, B, D & F)

FROM	TO: SLICE	Y		$C_{n=16}$		$\overline{G}, \overline{P}$		Z		N		OVR		DA, DB		$\overline{WRITE}$		$QIO_{0,15}$		SIO_0		SIO_{15}		SIO_0 PARITY		UNITS
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
A, B Addr	Any	49	58	53	58	53	58	50	54	56	70	56	68	31	40	–	–	–	–	49	58	48	58	62	67	ns
DA, DB	Any	41	46	34	40	34	41	35	37	43	50	41	48	–	–	–	–	–	–	29	35	32	40	55	64	ns
C_n	Any	32	42	18	23	–	–	26	29	31	35	28	34	–	–	–	–	–	–	29	35	31	36	31	36	ns
I_{8-0}	Any	46	52	38	41	28	42	58	61	43	46	50	54	–	–	22	30	29	32	34	46	44	48	49	60	ns
CP	Any	52	55	53	58	47	50	47	50	61	66	65	70	24	30	–	–	31	36	43	47	44	48	49	54	ns
$SIO_{0,15}$	Any	25	32	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns

NOTE:
1. Binary to BCD and multiprecision Binary to BCD instructions only

BCD to Binary conversion (SF 1) Binary to BCD conversion (SF 9) BCD substract (SF F)
BCD divide by two (SF 7) BCD add (SF B)

SIGN MAGNITUDE TO TWO'S COMPLEMENT CONVERSION (SF-5)

FROM	TO: SLICE	Y		$C_{n=16}$		$\overline{G}, \overline{P}$		Z		N		OVR		DA, DB		$\overline{WRITE}$		$QIO_{0,15}$		SIO_0		UNITS
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
A, B Addr	Any	49	58	53	58	53	58	50	54	56	70	56	68	31	40	–	–	–	–	49	58	ns
DA, DB	Any	41	46	34	40	34	41	35	37	43	50	41	48	–	–	–	–	–	–	29	35	ns
C_n	Any	32	42	18	23	–	–	–	–	31	35	28	34	–	–	–	–	–	–	29	35	ns
I_{8-0}	Any	46	52	38	41	28	42	58	61	43	46	50	54	–	–	22	30	29	32	34	46	ns
CP	Any	52	55	53	58	47	50	47	50	61	66	65	70	24	30	–	–	31	36	43	47	ns
Z ($\overline{OE}_Y$ = low)	Any							–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns
$SIO_{0,15}$	Any	25	32	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns

SF 5: F=S+C_n if Z=L
F=S+C_n if Z=H
Y15=S15 ↑ F15 (MSS)
Z=S15 (MSS)

Y=F
Q=Q
N=F15; Z=L
N=F15 ↑ S15; Z=H

NOTES:
1. A "–" means the delay path does not exist.
2. An "*" means the output may be enabled or disabled by the input; refer to function table.
3. This specification is not tested.

IDT49C403A GUARANTEED COMMERCIAL AND MILITARY RANGE PERFORMANCE
DIVIDE INSTRUCTIONS (SF-A, C & E)

FROM	TO: SLICE	Y Com'l.	Y Mil.	C_{n+16} Com'l.	C_{n+16} Mil.	$\overline{G}, \overline{P}$ Com'l.	$\overline{G}, \overline{P}$ Mil.	Z Com'l.	Z Mil.	N Com'l.	N Mil.	OVR Com'l.	OVR Mil.	DA, DB Com'l.	DA, DB Mil.	$\overline{WRITE}$ Com'l.	$\overline{WRITE}$ Mil.	$QIO_{0,15}$ Com'l.	$QIO_{0,15}$ Mil.	SIO_{15} Com'l.	SIO_{15} Mil.	UNITS
A, B Addr	Any	49	58	53	58	53	58	50	54	56	70	56	68	31	40	–	–	–	–	49	58	ns
DA, DB	Any	41	46	34	40	34	41	35	37	43	50	41	48	–	–	–	–	–	–	32	40	ns
C_n	Any	32	42	18	23	–	–	26	29	31	35	28	34	–	–	–	–	–	–	31	36	ns
I_{8-0}	Any	46	52	38	41	28	42	58	61	43	46	50	54	–	–	22	30	29	32	44	48	ns
CP	Any	52	55	53	58	47	50	47	50	61	66	65	70	24	30	–	–	31	36	44	48	ns
Z ($\overline{OE}_Y$ = low)	Any							–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns
$SIO_{0,15}$	Any	25	32	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns

NOTES:
1. Only 1st divide and normalization
2. Only two's complement divide and two's complement divide correction

Double Length Normalize and First Divide Op

SFA: F = S + C_n
N = F15 (MSS)
SIO_{15} = F15 ⊕ R15 (MSS)
C_{n+16} = F15 ⊕ F14 (MSS)
OVR = F2 ⊕ F1 (MSS)
Z = $\overline{Q0}$ $\overline{Q1}$ $\overline{Q2}$ $\overline{Q3}$ . . . $\overline{Q15}$ F0 F1 F2 F3 . . . F15
Y = Log 2F
Q = Log 2Q

Two's Complement Divide

SFC: F = S + R + C_n if Z = L
F = S − R − 1 + C_n if Z = H
SIO_{15} = F15 ⊕ R15 (MSS)
Z = F15 ⊕ R15 (MSS) from previous cycle
Y = Log 2F
Q = Log 2Q

Two's Complement Divide Correction and Remainder

SFE: S = C_n if Z = L
S − R − 1 + C_n if Z = H
Z = F15 ⊕ R15 (MSS) from previous cycle
Y = F
Q = Log 2Q

SINGLE LENGTH NORMALIZATION (SF-8)

FROM	TO: SLICE	Y Com'l.	Y Mil.	C_{n+16} Com'l.	C_{n+16} Mil.	$\overline{G}, \overline{P}$ Com'l.	$\overline{G}, \overline{P}$ Mil.	Z Com'l.	Z Mil.	N Com'l.	N Mil.	OVR Com'l.	OVR Mil.	DA, DB Com'l.	DA, DB Mil.	$\overline{WRITE}$ Com'l.	$\overline{WRITE}$ Mil.	$QIO_{0,15}$ Com'l.	$QIO_{0,15}$ Mil.	SIO_{15} Com'l.	SIO_{15} Mil.	UNITS
A, B Addr	Any	49	58	53	58	53	58	–	–	–	–	–	–	31	40	–	–	–	–	48	58	ns
DA, DB	Any	41	46	34	40	34	41	–	–	–	–	–	–	–	–	–	–	–	–	32	40	ns
C_n	Any	32	42	18	23	–	–	–	–	–	–	–	–	–	–	–	–	–	–	31	36	ns
I_{8-0}	Any	46	52	38	41	28	42	58	61	43	46	50	54	–	–	22	30	29	32	44	48	ns
CP	Any	52	55	53	58	47	50	47	50	61	66	65	70	24	30	–	–	31	36	44	48	ns
$SIO_{0,15}$	Any	25	32	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns

NOTES:
1. A "–" means the delay path does not exist.
2. An "*" means the output may be enabled or disabled by the input; refer to function table.
3. This specification is not tested.

IDT49C403 GUARANTEED COMMERCIAL AND MILITARY RANGE PERFORMANCE

The tables below specify the guaranteed performance of the IDT49C403 over the commercial operating range of 0 to 70°C with V_{CC} from 4.75 to 5.25V, and over the military operating range of -55 to +125°C with V_{CC} from 4.5 to 5.5V. All data are in nanoseconds, with input switching between 0 and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

Table 10. Clock and Write Pulse Characteristics All Functions

	COM'L.	MIL.	UNIT
Minimum Clock Low Time	12	13	ns
Minimum Clock High Time	12	13	ns
Minimum Time CP and WE both Low to Write	12	13	ns

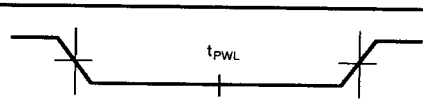
NOTE:
Guaranteed by design.

Table 11. Enable/Disable Times All Functions

FROM	TO	ENABLE COM'L.	ENABLE MIL.	DISABLE COM'L.	DISABLE MIL.	UNIT
$\overline{OE}_Y$	Y	15	24	12	14	ns
$\overline{OE}_B$	DB	17	26	15	16	ns
$\overline{OE}_A$	DA	18	26	16	17	ns
I_8	SIO	28	30	15	16	ns
I_8	QIO	20	29	25	27	ns
$I_{8,7,6,5}$	QIO	21	34	22	26	ns
$I_{4,3,2,1,0}$	QIO	25	37	22	26	ns

NOTE:
C_L = 5.0pF for output disable tests. Measurement is made to a 0.5V change on the output.

Table 12. Set-up and Hold Times All Functions



FROM	WITH RESPECT TO	SET-UP COM'L.	SET-UP MIL.	HOLD COM'L.	HOLD MIL.	SET-UP COM'L.	SET-UP MIL.	HOLD COM'L.	HOLD MIL.	UNIT	COMMENTS
Y	CP	–	–	–	–	10	11	2	2	ns	Store Y in RAM/Q (1)
$\overline{WE}$ HIGH	CP	8	9	2	2	–	–	2	2	ns	Prevent Writing
$\overline{WE}$ LOW	CP	–	–	–	–	12	13	0	0	ns	Write into RAM
A, B Source	CP	14	15	2	2	–	–	–	–	ns	Latch Data from RAM Out
B Destination (3)	CP	7	8	(3)	(3)	(3)	(3)	2	2	ns	Write Data into B Address
B Destination (3)	$\overline{IEN}$	7	8	(3)	(3)	(3)	(3)	2	2	ns	Write Data into B Address
B Destination (3)	$\overline{WE}$	7	8	(3)	(3)	(3)	(3)	2	2	ns	Write Data into B Address
$QIO_{0,15}$	CP	–	–	–	–	6	7			ns	Shift Q
$I_{8,7,6,5}$	CP	–	–	–	–	27	30	0	0	ns	Write into Q and RAM (2)
$\overline{IEN}$ HIGH (3)	CP	8	9	(3)	(3)	(3)	(3)			ns	Prevent Writing into Q and RAM (2)
$\overline{IEN}$ LOW (3)	CP	–	–	–	–	10	11			ns	Write into Q and RAM
$I_{4,3,2,1,0}$	CP	–	–	–	–	19	21			ns	Write into Q and RAM (2)
Q_0, Q_1	CP	–	–	–	–	10	11	2	2	ns	Write into Q
C_n	CP	–	–	–	–	34	36	0	0	ns	ALU Carry In to RAM

NOTES:
1. The internal Y-bus to RAM set-up condition will be met 5ns after valid Y output ($\overline{OE}_Y$ = 0)
2. The set-up time with respect to CP falling edge is to prevent writing. The set-up time with respect to CP rising edge is to enable writing.
3. The writing of data is controlled by CP, $\overline{IEN}$, and $\overline{WE}$; all must be LOW in order to write. The set-up time of B destination address is with respect to the last of these three inputs to go LOW, and the hold time is with respect to the first to go HIGH.
4. A "–" implies this path does not exist.

IDT49C403 GUARANTEED MILITARY AND COMMERCIAL RANGE PERFORMANCE STANDARD AND INCREMENT (SF-4) /DECREMENT (SF-3) BY ONE OR TWO INSTRUCTIONS

FROM	TO: SLICE	Y		$C_{n=16}$		$\overline{G}, \overline{P}$		Z		N		OVR		DA, DB		$\overline{WRITE}$		$QIO_{0,15}$		SIO_0		SIO_{15}		SIO_0 PARITY		UNITS
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
A, B Addr	Any	49	53	53	57	53	57	50	54	56	65	56	64	32	37	–	–	–	–	50	54	48	54	63	67	ns
DA, DB	Any	40	43	34	36	34	38	35	37	43	47	40	45	–	–	–	–	–	–	29	33	33	37	55	59	ns
C_n	Any	33	39	18	21	–	–	27	29	32	34	28	30	–	–	–	–	–	–	29	33	32	34	32	34	ns
I_{8-0}	Any	46	49	39	41	39	41	56	59	43	46	51	54	–	–	21	28	29	32	34	43	45	47	49	56	ns
CP	Any	51	55	53	56	47	51	47	51	62	66	65	70	24	28	–	–	32	34	43	46	45	47	49	53	ns
MSS	Any	26	39	–	–	26	28	46	50	26	28	24	26	–	–	–	–	–	–	–	–	24	26	–	–	ns
$SIO_{0,15}$	Any	25	30	–	–	–	–	20	21	–	–	–	–	–	–	–	–	–	–	–	–	23	26	19	23	ns

MULTIPLY INSTRUCTIONS (SF-0, 2 & 6)

FROM	TO: SLICE	Y		$C_{n=16}$		$\overline{G}, \overline{P}$		Z		N		OVR		DA, DB		$\overline{WRITE}$		$QIO_{0,15}$		SIO_0		UNITS
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
A, B Addr	Any	59	64	64	68	64	68	–	–	67	78	67	77	38	44	–	–	–	–	60	65	ns
DA, DB	Any	48	52	41	43	41	46	–	–	52	56	48	54	–	–	–	–	–	–	35	40	ns
C_n	Any	40	47	22	25	–	–	–	–	38	41	34	36	–	–	–	–	–	–	35	40	ns
I_{8-0}	Any	55	59	47	49	47	49	67	71	52	55	61	65	–	–	25	34	35	38	41	52	ns
CP	Any	61	66	64	67	58	61	–	–	74	79	78	84	29	34	–	–	38	41	52	55	ns
Z ($\overline{OE}_Y$ = low)	Any	65	70					–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns
$SIO_{0,15}$	Any	30	36	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns

Unsigned Multiply
SF 0: F = S + C_n if Z = L
F = S + R + C_n if Z = H
Y15 = C_n + 16 (MSS)
Z = Q0 (LSS)
Y = Log F/2
Q = Log Q/2

Two's Complement Multiply
SF 2: F = S + C_n if Z = L
F = S + R + C_n if Z = H
Y15 = F15 V OVR (MSS)
Z = Q0 (LSS)
Y = Log F/2
Q = Log Q/2

Two's Complement Multiply Last Cycle
SF 6: F = S + C_n if Z = L
F = S – R – 1 + C_n if Z = H
Y15 = OVR V F15 (MSS)
Z = Q0 (LSS)
Y = Log F/2
Q = Log Q/2

NOTES:
1. A "–" means the delay path does not exist.
2. An "*" means the output may be enabled or disabled by the input; refer to function table.
3. This specification is not tested.

IDT49C403 GUARANTEED MILITARY AND COMMERCIAL RANGE PERFORMANCE
BCD INSTRUCTIONS (SF-1, 7, 9, B, D & F)

FROM	SLICE	TO: Y		$C_{n=16}$		$\overline{G}, \overline{P}$		Z		N		OVR		DA, DB		$\overline{WRITE}$		$QIO_{0,15}$		SIO_0		SIO_{15}		SIO_0 PARITY		UNITS
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
A, B Addr	Any	59	64	64	68	64	68	60	65	67	78	67	77	38	44	–	–	–	–	60	65	58	65	76	80	ns
DA, DB	Any	48	52	41	43	41	46	42	44	52	56	48	54	–	–	–	–	–	–	35	40	40	44	66	71	ns
C_n	Any	40	47	22	25	–	–	32	35	38	41	34	36	–	–	–	–	–	–	35	40	38	41	38	41	ns
I_{8-0}	Any	55	59	47	49	47	49	67	61	52	55	61	65	–	–	25	34	35	38	41	52	54	56	59	67	ns
CP	Any	61	66	64	67	56	61	56	61	74	79	78	84	29	34	–	–	38	41	52	55	54	56	59	64	ns
$SIO_{0,15}$	Any	30	36	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns

NOTE:
1. Binary to BCD and multiprecision Binary to BCD instructions only

BCD to Binary conversion (SF1)
BCD divide by two (SF7)
Binary to BCD conversion (SF8)
BCD add (SF8)
BCD substract (SFF)

SIGN MAGNITUDE TO TWO'S COMPLEMENT CONVERSION (SF-5)

FROM	SLICE	TO: Y		$C_{n=16}$		$\overline{G}, \overline{P}$		Z		N		OVR		DA, DB		$\overline{WRITE}$		$QIO_{0,15}$		SIO_0		UNITS
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
A, B Addr	Any	59	64	64	68	64	68	60	65	67	78	67	77	38	44	–	–	–	–	60	65	ns
DA, DB	Any	48	52	41	43	41	46	42	44	52	56	48	54	–	–	–	–	–	–	35	40	ns
C_n	Any	40	47	22	25	–	–	–	–	38	41	34	36	–	–	–	–	–	–	35	40	ns
I_{8-0}	Any	55	59	47	49	47	49	67	71	52	55	61	65	–	–	25	34	35	38	41	52	ns
CP	Any	61	66	64	67	56	61	56	61	74	79	78	84	29	34	–	–	38	41	52	55	ns
Z ($\overline{OE}_Y$ = low)	Any							–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns
$SIO_{0,15}$	Any	30	36	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns

SF 5: F = S + C_n If Z = L
F = S + C_n If Z = H
Y15 = S15 ⊕ F15 (MSS)
Z = S15 (MSS)

Y = F
Q = Q
N = F15; Z = L
N = F15 ⊕ S15; Z = H

NOTES:
1. A "–" means the delay path does not exist.
2. An "*" means the output may be enabled or disabled by the input; refer to function table.
3. This specification is not tested.

IDT49C403 GUARANTEED MILITARY AND COMMERCIAL RANGE PERFORMANCE
DIVIDE INSTRUCTIONS (SF-A, C & E)

FROM	SLICE	TO: Y Com'l.	Y Mil.	$C_{n=16}$ Com'l.	$C_{n=16}$ Mil.	$\overline{G}, \overline{P}$ Com'l.	$\overline{G}, \overline{P}$ Mil.	Z Com'l.	Z Mil.	N Com'l.	N Mil.	OVR Com'l.	OVR Mil.	DA, DB Com'l.	DA, DB Mil.	$\overline{WRITE}$ Com'l.	$\overline{WRITE}$ Mil.	$QIO_{0,15}$ Com'l.	$QIO_{0,15}$ Mil.	SIO_{15} Com'l.	SIO_{15} Mil.	UNITS
A, B Addr	Any	59	64	64	68	64	68	60	65	67	78	67	77	38	44	–	–	–	–	58	65	ns
DA, DB	Any	48	52	41	43	41	46	42	44	52	56	48	54	–	–	–	–	–	–	40	44	ns
C_n	Any	40	47	22	25	–	–	32	35	38	41	34	36	–	–	–	–	–	–	38	41	ns
I_{8-0}	Any	55	59	47	49	47	49	67	71	52	55	61	65	–	–	25	34	35	38	54	56	ns
CP	Any	61	66	64	67	56	61	56	61	74	79	78	84	29	34	–	–	38	41	54	56	ns
Z ($\overline{OE}_Y$ = low)	Any							–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns
$SIO_{0,15}$	Any	30	36	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns

NOTES:
1. Only 1st divide and normalization
2. Only two's complement divide and two's complement divide correction

Double Length Normalize and First Divide Op

SFA: $F = S + C_n$
$N = F15$ (MSS)
$SIO15 = F15 \uparrow R15$ (MSS)
$C_n + 16 = F15 \uparrow F14$ (MSS)
$OVR = F2 \uparrow F1$ (MSS)
$Z = \overline{Q0}\ \overline{Q1}\ \overline{Q2}\ \overline{Q3} \ldots \overline{Q15}\ F0\ F1\ F2\ F3 \ldots F15$
$Y = Log\ 2F$
$Q = Log\ 2Q$

Two's Complement Divide

SFC: $F = S + R + C_n$ if $Z = L$
$F = S - R - 1 + C_n$ if $Z = H$
$SIO15 = \overline{F15 \uparrow R15}$ (MSS)
$Z = \overline{F15 \uparrow R15}$ (MSS) from previous cycle
$Y = Log\ 2F$
$Q = Log\ 2Q$

Two's Complement Divide Correction and Remainder

SFE: $S = C_n$ if $Z = L$
$S - R - 1 + C_n$ if $Z = H$
$Z = \overline{F15 \uparrow R15}$ (MSS) from previous cycle
$Y = F$
$Q = Log\ 2Q$

SINGLE LENGTH NORMALIZATION (SF-8)

FROM	SLICE	TO: Y Com'l.	Y Mil.	$C_{n=16}$ Com'l.	$C_{n=16}$ Mil.	$\overline{G}, \overline{P}$ Com'l.	$\overline{G}, \overline{P}$ Mil.	Z Com'l.	Z Mil.	N Com'l.	N Mil.	OVR Com'l.	OVR Mil.	DA, DB Com'l.	DA, DB Mil.	$\overline{WRITE}$ Com'l.	$\overline{WRITE}$ Mil.	$QIO_{0,15}$ Com'l.	$QIO_{0,15}$ Mil.	SIO_{15} Com'l.	SIO_{15} Mil.	UNITS
A, B Addr	Any	59	64	64	68	64	68	–	–	–	–	–	–	38	44	–	–	–	–	58	65	ns
DA, DB	Any	48	52	41	43	41	46	–	–	–	–	–	–	–	–	–	–	–	–	40	44	ns
C_n	Any	40	47	22	25	–	–	–	–	–	–	–	–	–	–	–	–	–	–	38	41	ns
I_{8-0}	Any	55	59	47	49	47	49	67	71	52	55	61	65	–	–	25	34	35	38	54	56	ns
CP	Any	61	66	64	67	56	61	56	61	74	79	78	84	29	34	–	–	38	41	54	56	ns
$SIO_{0,15}$	Any	30	36	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	ns

NOTES:
1. A "–" means the delay path does not exist.
2. An "*" means the output may be enabled or disabled by the input; refer to function table.
3. This specification is not tested but is guaranteed by correlation to the Standard Function Table.

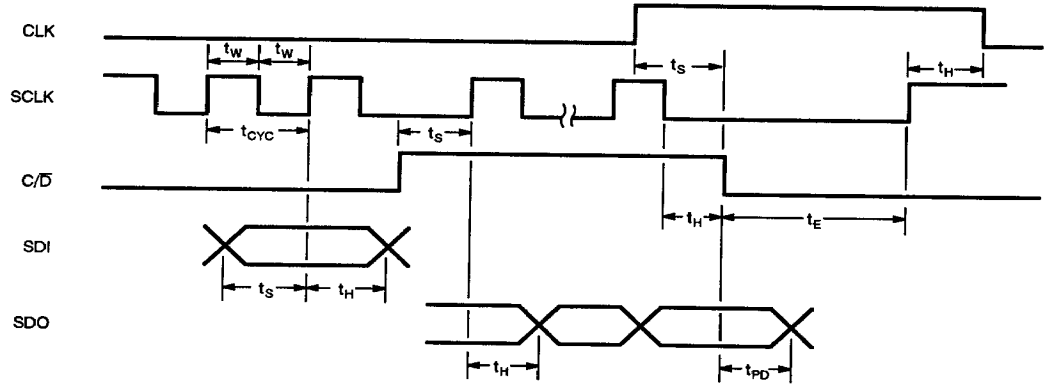


Figure 11. IDT49C403 SPC Timing Waveforms

IDT49C403/A SPC AC TIMING

SYMBOL	PARAMETERS	TEST CONDITIONS	MIN.	MAX.	UNIT
t_{PD}	SCLK TO SDO	R_L = 500Ω C_L = 50pF	3	15	ns
t_{PD}	C/$\overline{D}$ to SDO		3	50	ns
t_S	C/$\overline{D}$ to SCLK		5	–	ns
t_S	CLK to C/$\overline{D}$		20	–	ns
t_S	SDI to SCLK		10	–	ns
t_H	C/$\overline{D}$ to SCLK		5	–	ns
t_H	CLK to SCLK		5	–	ns
t_H	SDI to SCLK		5	–	ns
t_W	Pulse Width SCLK		20	–	ns
t_{CYC}	SCLK Period		50	–	ns
t_E	Execution, C/$\overline{D}$ to SCLK		50	–	ns

CMOS TESTING CONSIDERATIONS

There are certain testing considerations which must be taken into account when testing high-speed CMOS devices in an automatic environment. These are:

1) Proper decoupling at the test head is necessary. Placement of the capacitor set and the value of capacitors used is critical in reducing the potential erroneous failures resulting from large V_{CC} current changes. Capacitor lead length must be short and as close to the DUT power pins as possible.
2) All input pins should be connected to a voltage potential during testing. If left floating, the device may begin to oscillate causing improper device operation and possible latchup.
3) Definition of input levels is very important. Since many inputs may change coincidentally, significant noise at the device pins may cause the V_{IL} and V_{IH} levels not to be met until the noise has settled. To allow for this testing/board induced noise, IDT recommends using $V_{IL} \leq 0V$ and $V_{IH} \geq 3V$ for AC tests.
4) Device grounding is extremely important for proper device testing. The use of multi-layer performance boards with radial decoupling between power and ground planes is required. The ground plane must be sustained from the performance board to the DUT interface board. All unused interconnect pins must be properly connected to the ground pin. Heavy gauge stranded wire should be used for power wiring and twisted pairs are recommended to minimize inductance.

IDT49C403 INPUT/OUTPUT INTERFACE CIRCUITRY

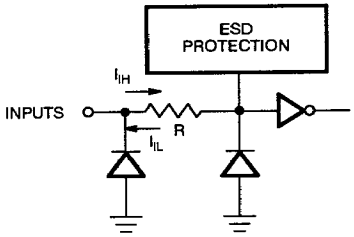


Figure 12. Input Structure (All Inputs)

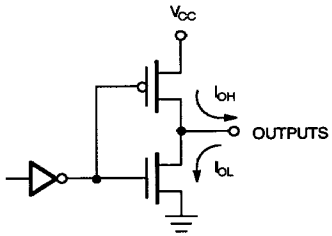


Figure 13. Output Structure (All Outputs)

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 15

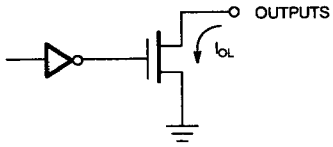
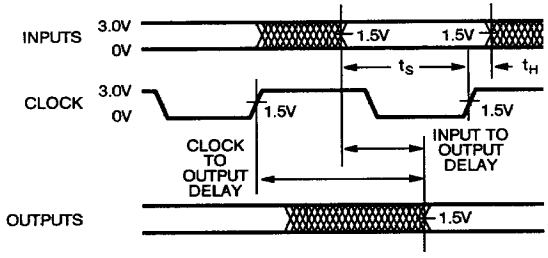


Figure 14. Open Drain Structure

8

SWITCHING WAVEFORMS



TEST LOAD CIRCUIT

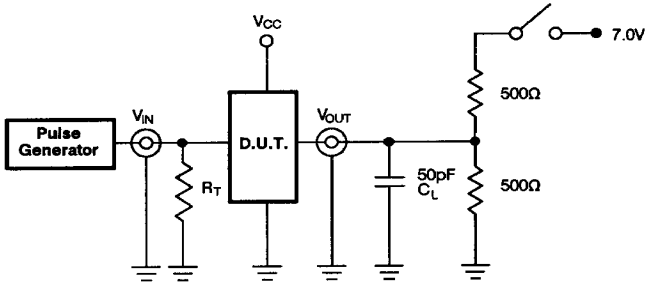


Figure 15. Test Load Circuit

TEST	SWITCH
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

DEFINITIONS

C_L = Load capacitance includes jig and probe capacitance

R_T = Termination resistance: should be equal to Z_{OUT} of the pulse generator

ORDERING INFORMATION