Integrated Device Technology, Inc.

32-BIT CMOS MICROPROGRAM MICROPROCESSOR

ADVANCE INFORMATION
IDT49C404
IDT49C404A

MICROSLICE™ PRODUCT

FEATURES:

- High speed CMOS
  - Microcycle Time: 80ns
- Three bi-directional 32-bit data I/O ports
  - DA, DB, Y
- 64-word x 32-bit expandable 7-port register file
  - 3 input ports and 4 output ports
  - Writes 3 operands and reads 4 operands in one cycle
- 64-bit in, 32-bit out cascadable funnel shifter
  - Fast alignment to any bit boundary
- 32-bit high-speed ALU cascadable to 64 bits
  - Selects status flags from any bit boundary
- Flexible mask generator and merge logic
  - Selects bit-fields on any width, on any boundary
- Priority encoder
- Powerful orthogonal instruction set
- Built-in multiplication/division support
- Counter function
- Includes Serial Protocol Channel (SPC™)
  - Flexible on-chip diagnostics
  - Serially monitors all pin states
  - Reads and writes to Register File
- Single 5V supply
- Available in 208-pin PGA
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT49C404 is a cascadable, microprogrammable, high-speed CMOS 32-bit microprocessor slice. This monolithic, highly parallel, 3-port device consists of a 7-port 64-word by 32-bit working RAM, 64 bits in/32 bits out cascadable funnel shifter, high-speed multi-function 32-bit ALU and 32-bit mask generation and merge logic.

The IDT49C404 uniquely incorporates shift, ALU and merge functions into a single cycle and utilizes an orthogonal instruction set to create a highly parallel architecture that achieves added performance.

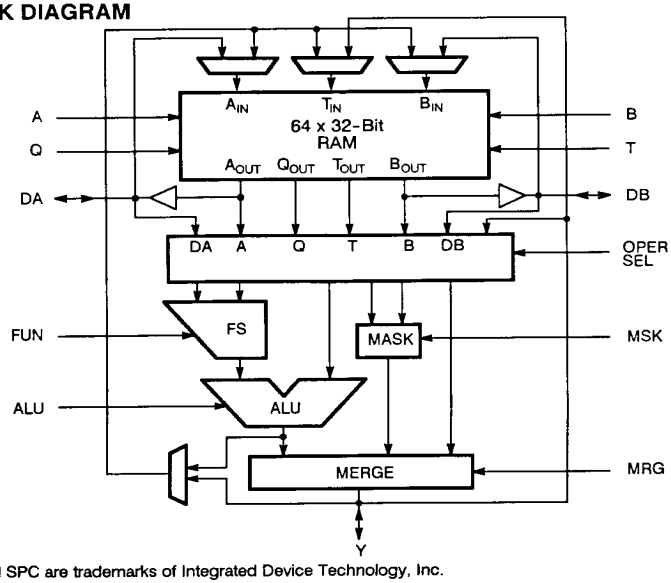
Supporting ultra-fast cycle times, the IDT49C404 offers a very-low-power CMOS alternative to existing bipolar counterparts.

This 32-bit device has been optimized, both architecturally and instruction set-wise, for use in all types of dedicated intelligent controllers such as high-speed graphics engines, array processors, fast disk and communication controllers, robotics, data base manipulation, design automation and AI.

Also featured on the IDT49C404 is an innovative diagnostics capability known as Serial Protocol Channel (SPC). This on-chip feature greatly simplifies the task of writing and debugging microcode, field maintenance debug and test, along with system testing during manufacturing.

The IDT49C404 is fabricated using CEMOS™, IDT's advanced CMOS technology designed for high-performance and high-reliability. The device is packaged in a 208-lead pin grid array. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making them ideally suited to military temperature applications demanding the highest level of performance and reliability.

SIMPLIFIED BLOCK DIAGRAM



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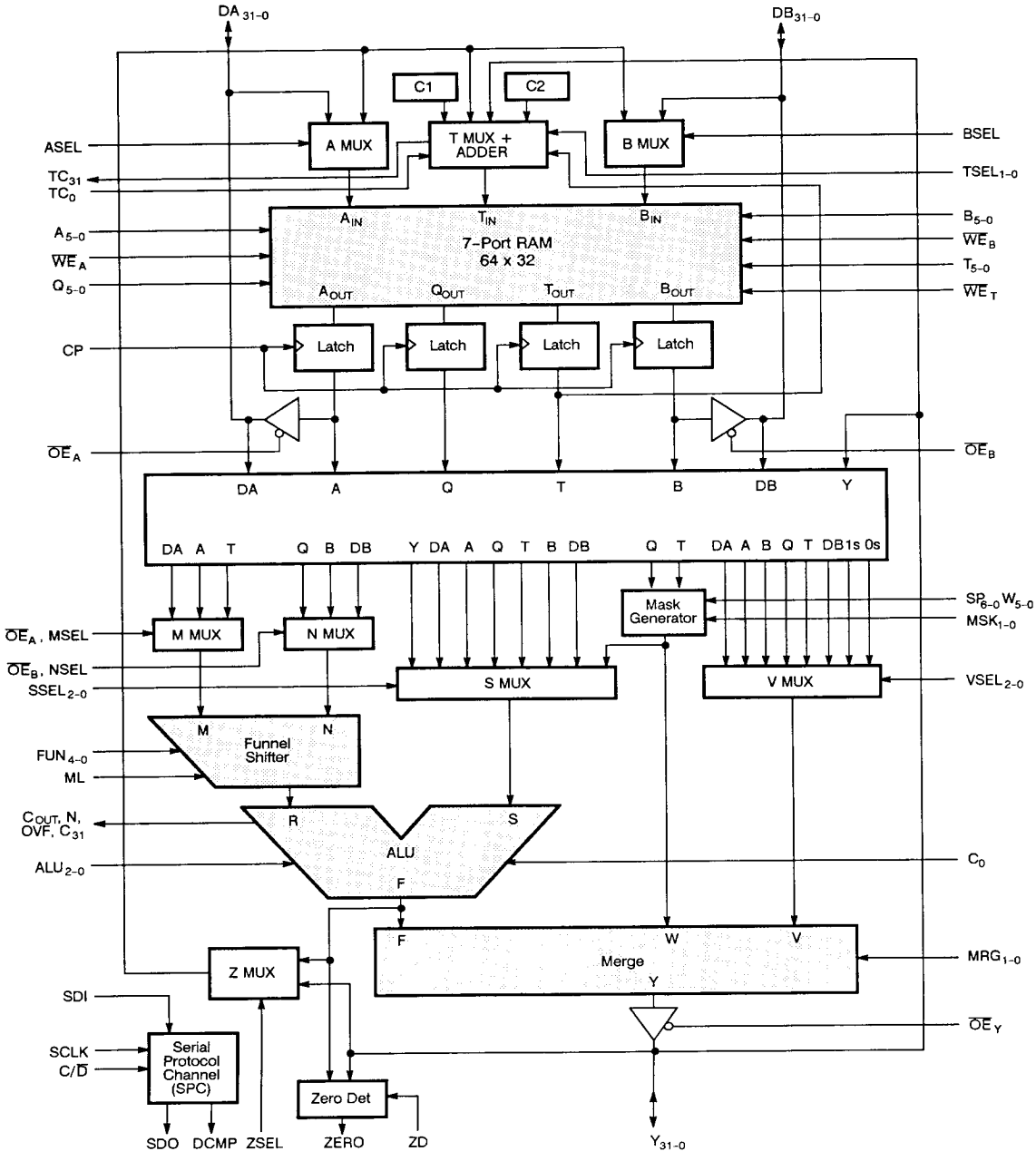
FUNCTIONAL BLOCK DIAGRAM



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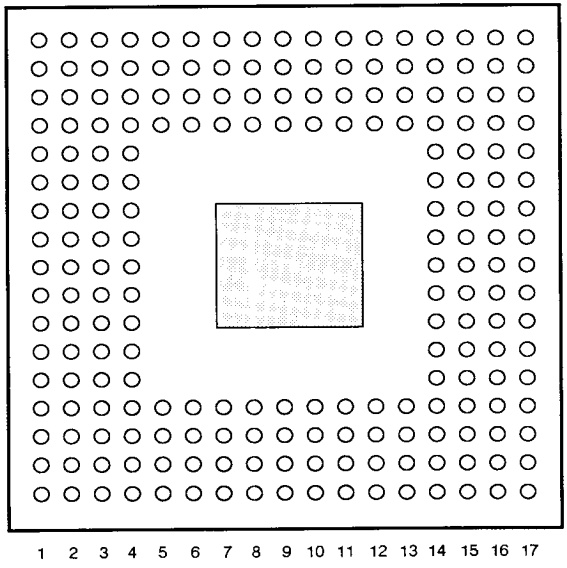
IDT49C404 PIN CONFIGURATION



PGA
BOTTOM
VIEW

PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME
A1		B1		C1		D1		E1	
A2		B2		C2		D2		E2	
A3		B3		C3		D3		E3	
A4		B4		C4		D4		E4	
A5		B5		C5		D5		E14	
A6		B6		C6		D6		E15	
A7		B7		C7		D7		E16	
A8		B8		C8		D8		E17	
A9		B9		C9		D9		F1	
A10		B10		C10		D10		F2	
A11		B11		C11		D11		F3	
A12		B12		C12		D12		F4	
A13		B13		C13		D13		F14	
A14		B14		C14		D14		F15	
A15		B15		C15		D15		F16	
A16		B16		C16		D16		F17	
A17		B17		C17		D17		G1	

PIN NO.	PIN NAME	PIN NO.	PIN NAME	PIN NO.	PIN NAME
G2		M3		Q11	
G3		M4		Q12	
G4		M14		Q13	
G14		M15		Q14	
G15		M16		Q15	
G16		M17		Q16	
G17		N1		Q17	
H1		N2		R1	
H2		N3		R2	
H3		N4		R3	
H4		N14		R4	
H14		N15		R5	
H15		N16		R6	
H16		N17		R7	
H17		P1		R8	
J1		P2		R9	
J2		P3		R10	
J3		P4		R11	
J4		P5		R12	
J14		P6		R13	
J15		P7		R14	
J16		P8		R15	
J17		P9		R16	
K1		P10		R17	
K2		P11		S1	
K3		P12		S2	
K4		P13		S3	
K14		P14		S4	
K15		P15		S5	
K16		P16		S6	
K17		P17		S7	
L1		Q1		S8	
L2		Q2		S9	
L3		Q3		S10	
L4		Q4		S11	
L14		Q5		S12	
L15		Q6		S13	
L16		Q7		S14	
L17		Q8		S15	
M1		Q9		S16	
M2		Q10		S17	

PIN DESCRIPTIONS

PIN NAME	DESCRIPTION
DA_{31-0}	Thirty-two-bit data input/output port is under control of the signal $\overline{OE}_A$. When the $\overline{OE}_A$ is low, RAM output port A can be directly read on these lines. Data on these lines can be selected as the source for the ALU, funnel-shifter or loaded into port A of the working RAM.
DB_{31-0}	Thirty-two-bit data input/output port is under control of the signal $\overline{OE}_B$. When the $\overline{OE}_B$ is low, RAM output port B can be directly read on these lines. Data on these lines can be selected as the source for the ALU, funnel-shifter or loaded into port B of the working RAM.
Y_{31-0}	Thirty-two-bit data input/output port is under control of the signal $\overline{OE}_Y$. When $\overline{OE}_Y$ is low, the merge output can be directly read on these lines. Data on the lines can be loaded into port T of the working RAM or selected as the source for the ALU when $\overline{OE}_Y$ is high.
$\overline{OE}_Y$	A control input pin which, when low, enables the output of merge-logics on the lines Y_{31-0} and, when high, disables the Y_{31-0} three-state output buffers.
$\overline{WE}_A$	The write control signal for RAM input port A. If the signal $\overline{WE}_A$ is low, the data on the DA lines or Z bus is written into the RAM (input port A) when the clock signal is low.
$\overline{WE}_B$	The write control signal for RAM input port B. If the signal $\overline{WE}_B$ is low, the data on the DB lines or Z bus is written into the RAM (input port B) when the clock signal is low.
$\overline{WE}_T$	The write control signal for RAM input port T. If the signal $\overline{WE}_T$ is low, the data on the Z lines, Y lines, T + C1 or T + C2 is written into the RAM (input port T) when clock signal is low.
$\overline{OE}_A$	A control input for data input/output port DA. When $\overline{OE}_A$ is low, RAM output port A is read on the DA line. When $\overline{OE}_A$ is high, the data on the data lines can be selected as the source for the ALU or loaded into port A of the working RAM.
$\overline{OE}_B$	A control input for data input/output port DB. When $\overline{OE}_B$ is low, RAM output port B can be read on these lines. When is $\overline{OE}_B$ high, the data on the DB lines can be selected as the source for the ALU or loaded into port T of the working RAM.
CP	The clock input to the IDT49C404. When clock is low, data is written in the seven-port RAM.
TC_0	Used as carry input for the T counter.
TC_{31}	Used as carry output for the T counter.
ML	The input pin which can be used to load the external bit in order to fill in the vacant positions of a word in shift-linkage.
C_0	The carry input to the least significant bit of the ALU.
C_{OUT}	Indicates the carry-output.
N	Indicates the sign N of the ALU operation.
OVF	Indicates the conventional two's complement overflow.
C_{31}	The carry output pin which is used to ripple the carry in the expansion mode (64-bit).
ZERO	The open drain input/output pin which, when high, generally indicates that all outputs are low.
ALU_{2-0}	Instruction inputs are used to select the operations for the ALU.
A_{5-0}	Six RAM address inputs which contains the address of the RAM word appearing at RAM output port A and into which new data is written when $\overline{WE}_A$ is low.
B_{5-0}	Six RAM address inputs which contains the address of the RAM word appearing at RAM output port B and into which new data is written when $\overline{WE}_B$ is low.
T_{5-0}	Six RAM address inputs which contains the address of the RAM word appearing at output port T and into which new data is written under control of TSEL.
ASEL	Defines what data RAM port A receives, either DA or Z bus.
BSEL	Defines what data RAM port B receives, either DB or Z bus.
Q_{5-0}	Six RAM address inputs which contain the address of the RAM word appearing at output port Q.
SP_{6-0}	The seven pins are used to specify the start positions or the number of shift positions.
W_{5-0}	The six pins are used to specify the word width.
ZSEL	Selects the source of the Z bus between the output of the ALU (F) or the Y bus.
MSEL	Taken together with $\overline{OE}_A$, selects the source of the M input into the funnel shifter.
NSEL	Taken together with $\overline{OE}_B$, selects the source of the N input into the funnel shifter.
$VSEL_{2-0}$	Selects the source of the V bus used for merging with the output of the ALU.
ZD	Chooses zero detect of the ALU output (F) or the Y bus.
$SSEL_{2-0}$	Selects the source of the S operand input to the ALU.
FUN_{4-0}	Controls the operation of the funnel shifter.
MSK_{1-0}	Selects the function of the mask generator.
MRG_{1-0}	Controls the merge function.

PIN DESCRIPTIONS (Cont'd)

PIN NAME	DESCRIPTION
$TSEL_{1-0}$	Selects the source of the data to be written into the T port of the RAM.
SDI	Serial data input to the SPC command and data registers for diagnostics.
SDO	Serial data output from SPC command and data registers for diagnostics.
SCLK	SHIFT clock for loading the SPC command and data registers for diagnostics.
C/$\overline{D}$	Command/data control input for SPC operation.
DCMP	The open drain compare output for SPC diagnostics.
VCC_{7-0}	Eight pins for power supply 5 volt, all of which must be connected to 5 volts.
GND_{16-0}	Sixteen pins for ground, all of which must be connected to ground.

DEVICE ARCHITECTURE

The IDT49C404 is a high-speed 32-bit microprogrammable CMOS microprocessor slice which can be cascaded to 64-bits. It allows simple, yet high-speed, arithmetic and logic operations on subfields, shift, rotate, mask and merge.

In general, the IDT49C404 can be viewed as a 7-port working RAM feeding into a funnel shifter, then into an ALU and then into merge logic. The control of each of these blocks is orthogonal, allowing the user to select data from registers, shift it, operate on it with the ALU and then merge it in only one cycle. Optionally, the funnel shifter or ALU can be bypassed, allowing the user additional flexibility. In this way, the designer may avoid paying a performance penalty when a particular algorithm requires only one or the other. Thus, the cycle time can be tailored to match the processing requirements.

The IDT49C404 can be divided into the following functional segments:

- Three 32-bit bidirectional I/O ports
- Seven-port 64-word x 32-bit RAM
- 64 bits in/32 bits out cascadable funnel shifter
- 32-bit ALU
- Mask generator
- Merge logic
- Diagnostics circuitry

THREE BUS ARCHITECTURE

The IDT49C404's 3-bus architecture consists of three bi-directional 32-bit ports (DA, DB and Y). The DA and DB bi-directional buses connect respectively to the A and B RAM outputs and A and B RAM inputs. Thus, data can be read out of the RAM on DA and DB or data can be brought in independently on DA and DB. This special feature allows for easy RAM expansion. Since data can be brought out on the DA and DB buses, other ALU elements can be connected externally which extend the overall ALU, funnel shifter, mask and merge capabilities.

The third 32-bit bus, Y, is the output of the merge logic and also the input back into the RAM ports A, B and T via the Z bus or internal Y bus.The Z MUX multiplexes between the ALU or the Y bus. By selecting the output of the ALU, the results of the ALU operation can be stored back into the RAM while data may be brought out through the merge path onto the Y bus. This results in an ALU operation in parallel with the extraction of data out of the register file. Additionally, there is an alternate data path which allows the Y bus to connect directly into the T MUX such that data can be written from the ALU back into the RAM while data is being brought in, at the same time, through the Y bus to the RAM.

This three bus approach allows for the easy data accessibility necessary when designing high-performance microprocessor-based systems.

SEVEN-PORT RAM

The IDT49C404 incorporates a 64-word by 32-bit RAM which has seven ports—four read ports and three write ports. The four read ports are A, B, Q and T. The A and B ports are considered the data path ports and can be used interchangeably. During most cycles, they supply data to the funnel shifter, ALU and merge logic. These ports can be considered to be similar to the A and B ports of the IDT39C203. The Q and T output ports are used mainly for controlling such things as start and width for the funnel shifter and mask generation for merge operations. Since the Q and T ports are outputs of the RAM, the start positions may be computed on previous cycles using the ALU, thus providing extensive programmer flexibility.

There are three write ports; A, B and T. The A and B ports are typically used for results from the current cycle and the T port is used for incrementing counter values in the RAM, as well as loading data from the Y bus in parallel with ALU operations. There are four address buses controlling A, B, Q and T. In one cycle, the seven-port RAM is capable of writing to three locations while reading from four locations. This feature highlights the IDT49C404's highly parallel architecture.

64-BIT FUNNEL SHIFTER

The funnel shifter accepts two 32-bit operands (A, B, Q, DA, DB or T) which are operated on as a 64-bit word. The output of the funnel shifter is the result of selecting any consecutive 32-bit word within the 64-bit operand. The 32-bit word can start on any bit boundary between 0 and 31. The M and N input muxes allow the user to swap the data as well as duplicate it, allowing for barrel shifting. The funnel shifter also has the capability of taking any 32-bit word as an input and extending the sign, as well as providing zero fill. Through special hooks in the architecture, the funnel shifter can be expanded along with the ALU/merge logic to perform 64-bit operations in a single cycle.

ALU

The output of the funnel shifter feeds the 32-bit ALU. The ALU can perform conventional binary operations such as logic, addition, subtraction, as well as multiplication and division. Also, the sum of the start and the width information can be used to select the bit boundary from which the carry, sign and overflow flags will output as status. This allows for true arbitrary subfield operations. The other ALU inputs are selected from A, B, Q, T or mask generator.

MASK GENERATION AND MERGE LOGIC

The mask generation and merge logic allows for field manipulation within the 32-bit resulting word. The mask generator, which determines how the bits will be merged between V and F, is controlled by start and width input pins. The start and width can also come from Q or T. T is used for start and Q is used for width, thus start/width can be calculated, stored in the register file and used in the mask generator. An alternate to the mask generator is a mask

which comes directly from the Q or T outputs of the RAM, allowing for totally arbitrary masks.

The V input of the merge logic comes from a multiplexer which can select any output of the RAM, DA, DB, all 1s or all 0s. The F input is connected to the output of the ALU. The mask is used to merge the V and F input on a bit-by-bit basis, which results in the Y output.

Included in the merge logic is a priority detect circuit. It is used to produce a binary weighted code to indicate the location of the highest order one on its input.

SERIAL DIAGNOSTICS

The Serial Protocol Channel (SPC) is a set of pins by which data can be entered into and extracted from a device (such as the IDT49C404) through a serial data input and output port. SPC can be used at many points in the life of a product for diagnostic purposes such as: system level design debug and development, system test during manufacturing and field maintenance debug and test. SPC is of significant benefit as board level packing densities increase. This is because access to test and debug points becomes difficult. This is particularly true in double-sided surface mount technologies.

As companies like IDT continue to integrate more onto each device and put each device into smaller and smaller packages such as surface mount devices, the board level testing becomes more complex for the designer and the manufacturing divisions of companies. To help this situation, a serial diagnostics scheme was developed. It allows for observation of critical signals deep within the system. During system test, when an error is observed, these signals may be modified in order to zero in on the fault in the system.

SPC is primarily a scheme utilizing only four pins SDI, SDO, SCLK, C/$\overline{D}$ to examine and alter the internal state of a system, for the purpose of monitoring and diagnosing system faults. The SPC has been defined in such a way that it can be implemented with a small number of gates. In many cases, SPC can be added by utilizing less than 5% of the total logic gates. As more gates are added to each device and the number of pins increase, the overhead for diagnostics decreases.

In the following block diagram of a typical application, the Serial Protocol Channel is shown being used with a writable control store in a microprogrammed design. The control store can be initialized through the SPC path. A register with SPC is used for the instruction register going into the IDT49C410 (16-bit microprogram sequencer), as well as data registers around the IDT49C404. In this way, the designer may use the Serial Protocol Channel to observe and modify the microcode coming out of the writable control store, as well as observing and being able to modify data and instructions in the overall machine.

The block diagram of the diagnostics ring in Figure 1 shows how the devices with diagnostics are hooked together in a serial ring via the SDI and SDO signals. The diagnostics signals may be generated through registers which are hooked up to a microprocessor. This microprocessor could conceivably be an IBM PC.

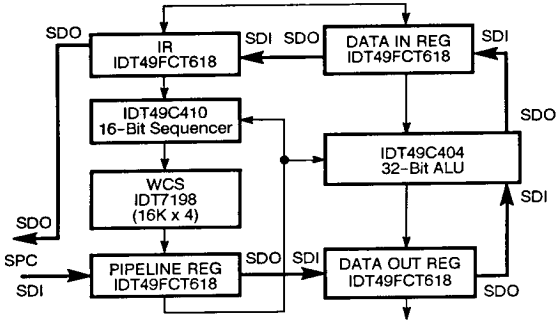


Figure 1. Typical Microprogram Application With SPC

The IDT49C404 accommodates a variety of diagnostics operations. It not only includes the standard Serial Protocol Channel but also the ability to scan data out of the I/O pad cells (as shown in Figure 2) which are connected to the pins of the device. In this way, the state of external connections can be observed, thus telling a lot about the system surrounding the IDT49C404. The scan path through the I/O pad cells is in series with the serial data register.

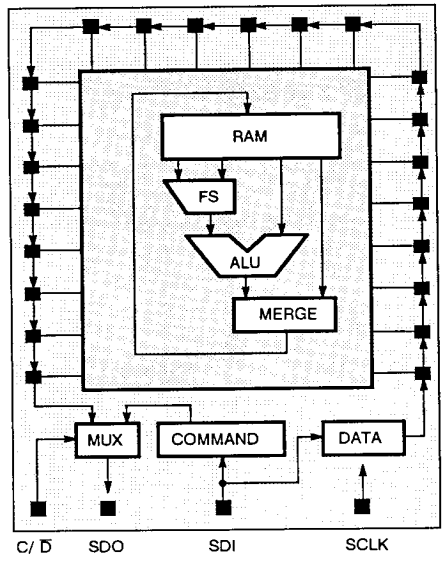


Figure 2. Conceptual Diagram of IDT49C404 Die Incorporating SPC Scan Path

CONTROL INPUTS

The control inputs of the IDT49C404 which make up the instruction set are highly orthogonal and provide the user with the highest degree of control over each individual functional unit. Each major unit in the IDT49C404 has its own set of control lines. The following diagrams show the microprogram word layout of the individual fields, as well as the opcodes and functions for each of the fields.

In order to maintain simplicity and orthogonality, the instruction combinations which are used infrequently and require special extended control (divide, multiply, etc.) are grouped together and labled as special instructions. To use these instructions, a special instruction trap door mechanism was employed in the ALU control field (opcode = 101). In the case of special instructions, the T source select and merge control define the particular instructions to be performed. Some special instructions require immediate operands which are provided by other fields such as start, width, funnel shift control, etc.

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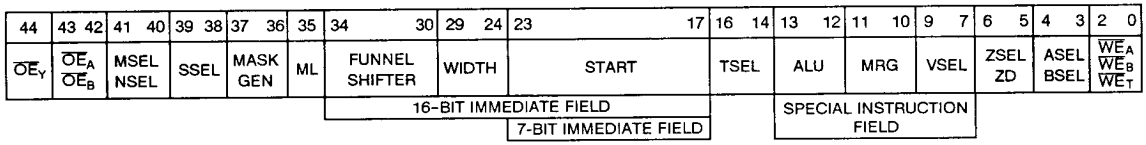
IDT49C404 INSTRUCTION FIELDS



INSTRUCTION SET SUMMARY

M SOURCE SELECTION			
MNEMONIC	$\overline{OE}_A$	MSEL	M SOURCE
AOE	0	0	A
T	0	1	T
A	1	0	A
DA	1	1	DA

MASK SOURCE			
MNEMONIC	MSK		SOURCE
EXT	0	0	Start and Width from Instruction
INT	0	1	T & Q Supply Start and Width
T32	1	0	T as a 32-Bit Mask
Q32	1	1	Q as a 32-Bit Mask

ALU				
MNEMONIC	ALU			FUNCTION
ADD	0	0	0	R + S + C_0
SUBR	0	0	1	S - R - 1 + C_0
SUBS	0	1	0	R - S - 1 + C_0
OR	0	1	1	R or S
AND	1	0	0	R and S
–	1	0	1	Special Instruction
EXOR	1	1	0	R exor S
EXNOR	1	1	1	R exnor S

V SOURCE				
MNEMONIC	VSEL			SOURCE
DA	0	0	0	DA
A	0	0	1	A
Q	0	1	0	Q
T	0	1	1	T
B	1	0	0	B
DB	1	0	1	DB
ZEROS	1	1	0	0's
ONEs	1	1	1	1's

N SOURCE SELECTION			
MNEMONIC	$\overline{OE}_B$	NSEL	N SOURCE
BOE	0	0	B
Q	0	1	Q
B	1	0	B
DB	1	1	DB

S SOURCE				
MNEMONIC	SSEL			SOURCE
DA	0	0	0	DA
A	0	0	1	A
Q	0	1	0	Q
T	0	1	1	T
B	1	0	0	B
DB	1	0	1	DB
Y	1	1	0	Y
MASK	1	1	1	MASK

MERGE CONTROL			
MNEMONIC	MRG		FUNCTION
F	0	0	Pass F
V	0	1	Pass V
F to V	1	0	Merge F/V
V to F	1	1	Merge V/F

SPECIAL INSTRUCTIONS (ALU = 101)								
MNEMONIC	MRG		VSEL			FUNCTION	OPERANDS
UMLT	0	0	0	0	0	Unsigned Multiply	A, B, T
TMLT	0	0	0	0	1	Two's Complement Multiply	A, B, T
TMLTL	0	0	0	1	0	Two's Complement Multiply Last Cycle	A, B, T
DIVF	0	0	0	1	1	First Divide	A, B, T
DIV	0	0	1	0	0	Second Divide	A, B, T
DIVL	0	0	1	0	1	Last Divide	A, B, T
PRF	0	0	1	1	0	Prioritize First Cycle (32 Bits)	S, Mask
PRS	0	0	1	1	1	Prioritize Second Cycle (64 Bits)	S
INC	0	1	0	0	0	S + Imm (7-Bit) + C_0	S, Imm
DEC	0	1	0	0	1	S - Imm (7-Bit) - 1 + C_0	S, Imm
LDI	0	1	0	1	0	Load T with Imm (16-Bit)	16-Bit Imm
LDC1	0	1	0	1	1	Load C1 from Z bus	S
LDC2	0	1	1	0	0	Load C2 from Z bus	S
EXCHG	0	1	1	0	1	Exchange RAM Locations	DA, DB
LDAB	0	1	1	1	0	Load DA into B address	DA
LDBA	0	1	1	1	1	Load DB into A address	DB
SMAGT	1	0	0	0	0	Sign Magnitude/Two's Complement Conversion	S
PROGS	1	0	0	0	1	Program Slice	–

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T SOURCE		
MNEMONIC	TSEL	SOURCE
Z	0 0	Z Bus
Y	0 1	Y Bus
TC1	1 0	T + C1 + TC_0
TC2	1 1	T + C2 + TC_0

A RAM DEST		
MNEMONIC	ASEL	SOURCE
DA	0	DA Bus
Z	1	Z Bus

B RAM DEST		
MNEMONIC	BSEL	SOURCE
Z	0	Z Bus
DB	1	DB Bus

Z BUS CONTROL

Z BUS SOURCE		
MNEMONIC	ZSEL	SOURCE
F	0	F Bus
Y	1	Y Bus

ZERO DETECT SOURCE		
MNEMONIC	ZD	SOURCE
F	0	F Bus
Y	1	Y Bus

FUNNEL SHIFT OPERATIONS							
MNEMONIC	FUN					FUNCTION	OPERANDS
SMLZ	0	0	0	0	0	Shift M and fill with 0	0, M
SNLZ	0	0	0	0	1	Shift N and fill with 0	0, N
SMLM	0	0	0	1	0	Shift M and fill with ML	ML, M
SNLM	0	0	0	1	1	Shift N and fill with ML	ML, N
XNM	0	0	1	0	0	Extract field from	N, M
XMN	0	0	1	0	1	Extract field from	M, N
SMAZ	0	0	1	1	0	Shift M arithmetic and fill 0	Sign, M, 0
SNAZ	0	0	1	1	1	Shift N arithmetic and fill 0	Sign, N, 0
SMAM	0	1	0	0	0	Shift M arithmetic and fill ML	Sign, M, ML
SNAM	0	1	0	0	1	Shift N arithmetic and fill ML	Sign, N, ML
BM	0	1	0	1	0	Barrel shift M	M
BN	0	1	0	1	1	Barrel shift N	N
PM	0	1	1	0	0	Pass M	M
PN	0	1	1	0	1	Pass N	N
PZ	0	1	1	1	0	Pass all 0s	0
PO	0	1	1	1	1	Pass all 1s	1
SMLZBA	1	0	0	0	0	Shift M and fill with 0, Bypass ALU	0, M
SNLZBA	1	0	0	0	1	Shift N and fill with 0, Bypass ALU	0, N
SMLMBA	1	0	0	1	0	Shift M and fill with ML, Bypass ALU	ML, M
SNLMBA	1	0	0	1	1	Shift N and fill with ML, Bypass ALU	ML, N
XNMBA	1	0	1	0	0	Extract field from N & M, Bypass ALU	N, M
XMNBA	1	0	1	0	1	Extract field from M & N, Bypass ALU	M, N
SMAZBA	1	0	1	1	0	Shift M arith. and fill 0, Bypass ALU	Sign, M, 0
SNAZBA	1	0	1	1	1	Shift N arith. and fill 0, Bypass ALU	Sign, N, 0
SMAMBA	1	1	0	0	0	Shift M arith. and fill ML, Bypass ALU	Sign, M, ML
SNAMBA	1	1	0	0	1	Shift N arith. and fill ML, Bypass ALU	Sign, N, ML
BMBA	1	1	0	1	0	Barrel shift M, Bypass ALU	M
BNBA	1	1	0	1	1	Barrel shift N, Bypass ALU	N
POCM	1	1	1	0	0	Pass 1s Complement of M	M
POCN	1	1	1	0	1	Pass 1s Complement of N	N
PMFM	1	1	1	1	0	Pass M and fill ML bit from Bit0 to SP	M
PNFM	1	1	1	1	1	Pass N and fill ML from Bit0 to SP	N

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.8	1.8	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
$C_{I/O}$(2)	I/O Capacitance	V_{OUT} = 0V	15	pF

NOTE:

1. This parameter is sampled and not 100% tested.
2. Includes only output pins.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C V_{CC} = 5.0V ± 5% (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ± 10% (Military)

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level (4)	V_{CC} = Max.		2.0	–	–	V
V_{IL}	Input LOW Level (4)	V_{CC} = Min.		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		–	–	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0V		–	–	-5	µA
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	V
			I_{OH} = -6mA MIL.	2.4	4.3	–	
			I_{OH} = -8mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	V
			I_{OL} = 12mA MIL.	–	0.3	0.5	
			I_{OL} = 15mA COM'L.	–	0.3	0.5	
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0V	–	-0.1	-10	µA
			V_O = V_{CC} (Max.)	–	0.1	10	
I_{OS}	Short Circuit Current	V_{CC} = Min., V_{OUT} = 0V (3)		-15	–	–	mA

NOTES:

1. For conditions shown as max. or min. use appropriate value specified under Electrical Characteristics.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. These input levels provide zero noise immunity and should only be static tested in a noise-free environment.

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DC ELECTRICAL CHARACTERISTICS (Cont'd)

T_A = 0°C to +70°C V_{CC} = 5.0V ±5% (Commercial)
T_A = -55°C to +125°C V_{CC} = 5.0V ±10% (Military)
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS [1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQH}	Quiescent Power Supply Current CP = H	V_{CC} = Max. $V_{IH} \geq V_{HC}$, $V_{IL} \leq V_{LC}$ f_{CP} = 0, CP = V_{CC}		–	–	–	mA
I_{CCQL}	Quiescent Power Supply Current CP = L	V_{CC} = Max. $V_{IH} \geq V_{HC}$, $V_{IL} \leq V_{LC}$ f_{CP} = 0, CP = 0V		–	–	–	mA
I_{CCT}	Quiescent Input Power Supply[5] Current (per Input @ TTL High)	V_{CC} = Max. V_{IL} = 3.4V, f_{CP} = 0		–	–	–	mA
I_{CCD}	Dynamic Power Supply Current	V_{CC} = Max. $V_{HC} \leq V_{IH}$, $V_{IL} \leq V_{LC}$ Outputs Open, $\overline{OE}$ = 0V	MIL.	–	–	–	mA/ MHz
			COM'L.	–	–	–	
I_{CC}	Total Power Supply Current [6]	V_{CC} = Max., f_{CP} = 10MHz Outputs Open, $\overline{OE}$ = 0V 50% Duty cycle $V_{HC} \leq V_{IH}$, $V_{IL} \leq V_{LC}$	MIL.	–	–	–	mA
			COM'L.	–	–	–	
		V_{CC} = Max., f_{CP} = 10MHz Outputs Open, $\overline{OE}$ = 0V 50% Duty cycle V_{IH} = 3.4V, V_{IL} = 0.4V	MIL.	–	300	400	
			COM'L.	–	250	350	

NOTES:

5. I_{CCQT} is derived by measuring the total current with all the inputs tied together at 3.4V, subtracting out I_{CCQCH}, then dividing by the total number of inputs.
6. Total Supply Current is the sum of the Quiescent current and the Dynamic current (at either CMOS or TTL input levels). For all conditions, the Total Supply Current can be calculated by using the following equation:

$$I_{CC} = I_{CCQH}(CD_H) + I_{CCQL}(1 - CD_H) + I_{CCT}(N_T \times D_H) + I_{CCD}(f_{CP})$$

CD_H = Clock duty cycle high period
D_H = Data duty cycle TTL high period (V_{IN} = 3.4V)
N_T = Number of dynamic inputs driven at TTL levels
f_{CP} = Clock Input frequency

CMOS TESTING CONSIDERATIONS

Special test board considerations must be taken into account when applying high-speed CMOS products to the automatic test environment. Large output currents are being switched in very short periods and proper testing demands that test set-ups have minimized inductance and guaranteed zero voltage grounds. The techniques listed below will assist the user in obtaining accurate testing results:

1) All input pins should be connected to a voltage potential during testing. If left floating, the device may oscillate, causing improper device operation and possible latchup.

2) Placement and value of decoupling capacitors is critical. Each physical set-up has different electrical characteristics and it is recommended that various decoupling capacitor sizes be experimented with. Capacitors should be positioned using the minimum lead lengths. They should also be distributed to decouple power supply lines and be placed as close as possible to the DUT power pins.

3) Device grounding is extremely critical for proper device testing. The use of multi-layer performance boards with radial decoupling between power and ground planes is necessary. The ground plane must be sustained from the performance board to the DUT interface board and wiring unused interconnect pins to the ground plane is recommended. Heavy gauge stranded wire should be used for power wiring, with twisted pairs being recommended for minimized inductance.

4) To guarantee data sheet compliance, the input thresholds should be tested per input pin, in a static environment. To allow for testing and hardware-induced noise, IDT recommends using $V_{IL} \leq 0V$ and $V_{IH} \geq 3V$ for AC tests.

IDT49C404 PROPAGATION DELAYS [1]

T_A = 0°C to +70°C, V_{CC} = +5V ±5%

FROM INPUT	TO OUTPUT											
	Y			ZERO			DCMP			STATUS FLAGS		UNIT
	ALU only	FS only	ALU & FS	ALU only	FS only	ALU & FS	ALU only	FS only	ALU & FS	ALU only	ALU & FS	
A, B, Q, T	55	55	75	58	58	78	–	–	–	40	54	ns
DA, DB	37	37	56	40	40	60	–	–	–	40	34	ns
NSEL, MSEL, MS, NS, $\overline{OE}$A, $\overline{OE}$B	–	–	–	–	–	–	–	–	–	–	–	ns
MSK, FS, STR, W	–	–	–	–	–	–	–	–	–	–	–	ns
ALU	–	–	–	–	–	–	–	–	–	–	–	ns
C_0	–	–	36	–	–	–	–	–	–	–	–	ns
MRG, ZD	–	–	–	–	–	–	–	–	–	–	–	ns
Y	–	–	–	–	–	–	–	–	–	–	–	ns

NOTE:

1. On any given cycle, an arithmetic operation without a shift operation can be performed (ALU only) or a shift operation without an arithmetic operation can be performed (FS only) or, finally, both operations in series in one single cycle (ALU + FS).

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP INPUT)

INPUT	CP: 				UNIT
	SET-UP TIME BEFORE H-L	HOLD TIME AFTER H-L	SET-UP TIME BEFORE L-H	HOLD TIME AFTER L-H	
A, B, T, Q Address (Source or Destination)	18	0	–	1	ns
DA, DB	–	–	–	0	ns
C_0, M_L	–	–	–	1	ns
I_{LINES}	–	–	–	0	ns
Y	–	–	–	0	ns

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IDT49C404A PROPAGATION DELAYS [1]

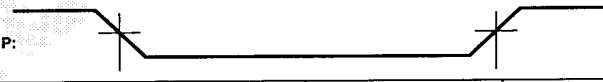
T_A = 0°C to +70°C, V_{CC} = +5V ±5%

FROM INPUT	TO OUTPUT											UNIT
	Y			ZERO			DCMP			STATUS FLAGS		
	ALU only	FS only	ALU & FS	ALU only	FS only	ALU & FS	ALU only	FS only	ALU & FS	ALU only	ALU & FS	
A, B, Q, T	–	–	–	–	–	–	–	–	–	–	–	ns
DA, DB	–	–	–	–	–	–	–	–	–	–	–	ns
NSEL, MSEL, MS, NS, $\overline{OE}$A, $\overline{OE}$B	–	–	–	–	–	–	–	–	–	–	–	ns
MSK, FS, STR, W	–	–	–	–	–	–	–	–	–	–	–	ns
ALU	–	–	–	–	–	–	–	–	–	–	–	ns
C_0	–	–	–	–	–	–	–	–	–	–	–	ns
MRG, ZD	–	–	–	–	–	–	–	–	–	–	–	ns
Y	–	–	–	–	–	–	–	–	–	–	–	ns

NOTE:

1. On any given cycle, an arithmetic operation without a shift operation can be performed (ALU only) or a shift operation without an arithmetic operation can be performed (FS only) or, finally, both operations in series in one single cycle (ALU + FS).

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP INPUT)



INPUT	SET-UP TIME BEFORE H-L	HOLD TIME AFTER H-L	SET-UP TIME BEFORE L-H	HOLD TIME AFTER L-H	UNIT
A, B, T, Q Address (Source or Destination)	–	–	–	–	ns
DA, DB	–	–	–	–	ns
C_0, M_L	–	–	–	–	ns
I_{LINES}	–	–	–	–	ns
Y	–	–	–	–	ns

TEST LOAD CIRCUIT

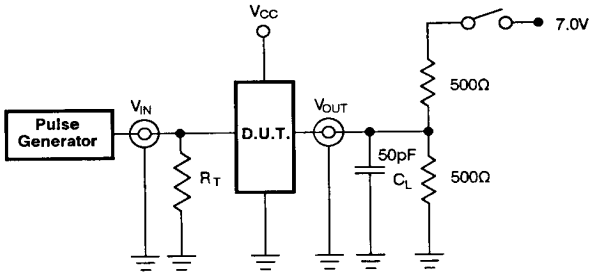


Figure 1. Switching Test Circuits (All Outputs)

SWITCH POSITION

TEST	SWITCH
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

DEFINITIONS

C_L = Load capacitance: includes jig and probe capacitance

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

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ORDERING INFORMATION

IDT XXXXXXX (Device Type) XX (Package) X (Process/Temperature)

BLANK	Commercial (0°C to +70°C)
B	Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B
PG	208-pin Plastic Pin Grid Array
G	208-pin Pin Grid Array
49C404	32-Bit CMOS Microprogram Microprocessor
49C404A	High-Speed 32-Bit CMOS Microprogram Microprocessor