Integrated Device Technology Inc

HIGH SPEED 16-BIT REGISTER WITH SPC™

PRELIMINARY
IDT49FCT618
IDT49FCT618A

FEATURES:

- High-speed non-inverting 16-bit parallel data register for any data path, control path or pipelining application
- Read back path from the data output back to the data input allows for convenient interface to a microprocessor as a parallel high-speed/high-output drive I/O port
- Clock enable and asynchronous clear lines
- High-speed Serial Protocol Channel (SPC™) which provides access to 16 bit parallel data register using four pins
  - Controllability:
    - Serial scan in new machine state
    - Load new machine state "on the fly" synchronous with PCLK
    - Temporarily force Y output bus
    - Temporarily force data out the D input bus (as in loading WCS)
  - Observability:
    - Directly observe D and Y buses
    - Serial scan out current machine state
    - Capture machine state "on the fly" synchronous with PCLK
- I_{OL} = 32mA (commercial), 24mA (military)
- CMOS power levels (5μW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Available in 48-pin DIP and 52-pin LCC/PLCC
- Product available in Radiation Tolerant and Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT49FCT618/A are high-speed, general purpose 16-bit parallel data registers with a Serial Protocol Channel (SPC). The D-to-Y path of the register provides a data path that is designed for normal system operation wherever a high-speed clocked register is required. This device also incorporates a latched read back path from the Y bus to the D bus. The SPC is used to communicate with SPC command and data registers.

The SPC command and data registers are used to observe and control the operation of the 16-bit parallel data register for diagnostic purposes. The SPC command and data registers can be accessed while the system is performing normal system function. Diagnostic operations then can be performed "on the fly", synchronous with the system clock, or can be performed in the "single step" environment. The SPC port utilizes serial data in and out pins (a concept originated at IBM) which can participate in a serial scan loop throughout the system where normal data, address, status and control registers are replaced with the IDT49FCT618/A. The loop can be used to scan in a complete test routine starting point (data, address, etc.). Then, after a specified number of clock cycles, the data can be clocked out and compared with expected results. An "oscilloscope mode" can be achieved by loading data from the SPC data register into the parallel data register synchronous to the system clock (PCLK) using an SPC command which transfers data synchronously. When repeated every Nth clock, the repeating states of the system can be observed on an oscilloscope. When used as a pipeline register, Writable Control Store (WCS) loading can be accomplished by scanning in data through the SPC port and enabling the data onto the D bus pins.

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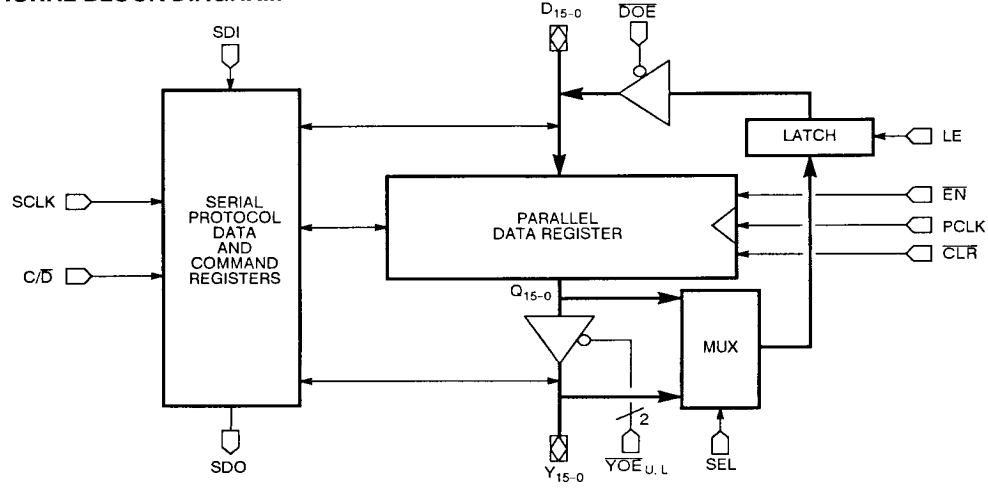
FUNCTIONAL BLOCK DIAGRAM



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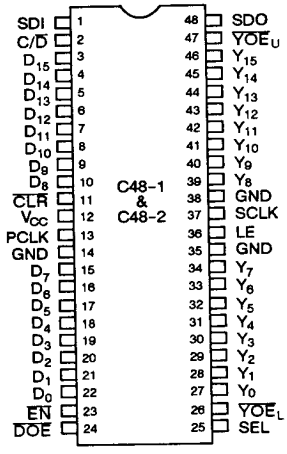
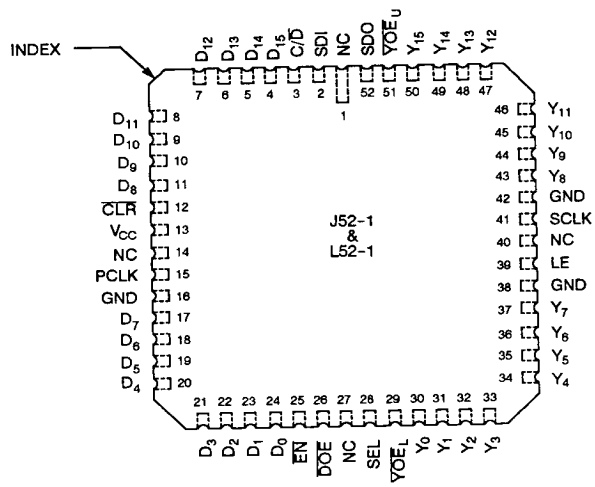
PIN CONFIGURATIONS



DIP
TOP VIEW



LCC/PLCC
TOP VIEW

PIN DESCRIPTION

PIN NAME	I/O	DESCRIPTION
PCLK	I	Parallel Data Register Clock
$\overline{EN}$	I	Clock Enable for PCLK (enabled when low)
$\overline{CLR}$	I	Asynchronous 16-Bit Clear (active low)
D_{15-0}	I/O	Parallel Data Register Input Pins (D_0 = LSB, D_{15} = MSB)
Y_{15-0}	I/O	Parallel Data Register Output Pins (Y_0 = LSB, Y_{15} = MSB)
$\overline{YOE}_{U,L}$	I	Output Enables for Y Bus (Overidden by SPC Inst. 8 and 14)
SEL	I	Selects Between Parallel Data Register Q or Y Bus for Read Back Data
LE	I	Controls a Latch in the Read Back Path (transparent when High)
$\overline{DOE}$	I	Output Enable for D Bus (Overidden by SPC Inst. 9)
SDI	I	Serial Data In for SPC operation
SDO	O	Serial Data Out for SPC operation
C/$\overline{D}$	I	Mode Control for SPC
SCLK	I	Shift clock for SPC operations

TRUTH TABLE [1]

C/$\overline{D}$	SCLK	PCLK	$\overline{EN}$	$\overline{CLR}$	$\overline{DOE}$	SEL	LE	$\overline{YOE}_{U,L}$	D	Y	FUNCTION
X	X	X	X	X	X	X	X	H	X	High Z	Tri-State Y
X	X	X	X	L	X	X	X	H	X	L	Clear Parallel Data Register
X	X	↓	H	H	X	X	X	L	X	NC	Hold Parallel Data Register
X	X	↓	L	H	X	X	X	L	Input	D	Clock D-to-Y
X	X	X	X	H	L	H	H	H	Q	X	Read Back Parallel Data Register
X	X	X	X	H	L	L	H	H	Y	Input	Read Back Y Data Bus
H	↓	X	X	X	X	X	X	X	X	X	Shift Bit into SPC Command Register
L	↓	X	X	X	X	X	X	X	X	X	Shift Bit into SPC Data Register
↑	↓	H or L (Static)	X	X	X	X	X	X	X	X	Execute SPC Command During Time Between C/$\overline{D}$ & SCLK
X	X	X	X	X	L	X	L	X	X	X	Read data stored in feedback latch

NOTE:
H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care, Z = High Impedance, ↓/↑ = Low-to-High/High-to-Low Transition

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ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is guaranteed by characterization data and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V
Commercial: T_A = 0°C to +70°C; V_{CC} = 5.0V±5%
Military: T_A = -55°C to +125°C; V_{CC} = 5.0V±10%

SYMBOL	PARAMETER	TEST CONDITIONS(1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current (Except I/O pins)	V_{CC} = Max.	V_I = V_{CC}	–	–	5	µA
			V_I = 2.7V	–	–	5(4)	
I_{IL}	Input LOW Current (Except I/O pins)		V_I = 0.5V	–	–	-5(4)	
			V_I = GND	–	–	-5	
I_{IH}	Input HIGH Current (I/O pins only)	V_{CC} = Max.	V_I = V_{CC}	–	–	15	µA
			V_I = 2.7V	–	–	15(4)	
I_{IL}	Input LOW Current (I/O pins only)		V_I = 0.5V	–	–	-15(4)	
			V_I = GND	–	–	-15	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = -18mA		–	-0.7	-1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		-60	-120	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32 µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = -300µA	V_{HC}	V_{CC}	–	
			I_{OH} = -12mA MIL.	2.4	4.3	–	
			I_{OH} = -15mA COM'L.	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 24mA MIL.	–	0.3	0.5	
			I_{OL} = 32mA COM'L.	–	0.3	0.5	
V_H	Input Hysteresis on Clocks Only	–		–	200	–	mV

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_i = 0$		–	0.001	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{YOE}_{U,L}$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	–	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{YOE}_{U,L}$ = GND One Bit Toggling at f_i = 5MHz 50% Duty Cycle SEL, $\overline{DOE}$, $\overline{CLR}$, LE, SDI, $\overline{C/D}$, SCLK = V_{CC}	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	1.5	4.0	mA
			V_{IN} = 3.4V or V_{IN} = GND	–	2.0	6.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{YOE}_{U,L}$ = GND Sixteen Bits Toggling at f_i = 2.5MHz 50% Duty Cycle SEL, $\overline{DOE}$, $\overline{CLR}$, LE, SDI, $\overline{C/D}$, SCLK = V_{CC}	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	–	6.8	12.8[5]	
			V_{IN} = 3.4V or V_{IN} = GND	–	11.0	29.8[5]	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL		PARAMETER	CONDITION[1]	IDT49FCT618				IDT49FCT618A				UNIT
				COM'L.		MIL.		COM'L.		MIL.		
				MIN.[2]	MAX.	MIN.[2]	MAX.	MIN.[2]	MAX.	MIN.[2]	MAX.	
t_{PLH} t_{PHL}	T1	PCLK ↑ to Y	C_L = 50pF R_L = 500Ω	3.0	12.5	3.0	14.0					ns
	T2	SCLK ↑ to SDO		3.0	12.5	3.0	14.0					
	T3	SDI to SDO (in stub mode)		3.0	12.5	3.0	14.0					
	T4	C/$\overline{D}$ ↓ to Y ($\overline{YOE}_{U,L}$ = Low Inst. 8 & 14)		3.0	12.5	3.0	14.0					
	T5	SCLK ↑ to Y ($\overline{YOE}_{U,L}$ = High, Inst. 8)		3.0	12.5	3.0	14.0					
	T6	C/$\overline{D}$ to SDO (Inst. 0,1,2,4)		2.0	12.5	3.0	14.0					ns
	T7	LE to D		2.0	12.5	3.0	14.0					
	T8	Y to D		2.0	12.5	3.0	14.0					
	T9	SEL or $\overline{CLR}$ to Y		2.0	12.5	3.0	14.0					
	T10	SEL to D		2.0	12.5	3.0	14.0					
t_{SU}	S1	D to PCLK ↑		2.5	–	3.0	–					ns
	S2	C/$\overline{D}$ to SCLK ↑		12.0	–	14.0	–					
	S3	SDI to SCLK ↑		4.0	–	5.0	–					
	S4	Y or D to C/$\overline{D}$ (Inst. 0, 2 & 4)		2.0	–	2.5	–					
	S5	C/$\overline{D}$ (Low) to PCLK ↑ (Inst. 3 & 13)		8.0	–	9.0	–					
	S6	Y to PCLK ↑ (Inst. 3)		2.0	–	2.5	–					
	S7	Y to LE		3.0	–	4.0	–					
	S8	SEL to LE		3.0	–	4.0	–					
	S9	$\overline{EN}$ to PCLK		3.0	–	4.0	–					
	S10	PCLK ↑ to LE (Low)		3.0	–	4.0	–					
t_H	H1	D to PCLK ↑		2.0	–	2.5	–					ns
	H2	C/$\overline{D}$ to SCLK ↑		12.0	–	14.0	–					
	H3	SDI to SCLK ↑		1.0	–	1.0	–					
	H4	Y or D to C/$\overline{D}$ ↓ (Inst. 0, 2 & 4)		2.0	–	2.5	–					
	H5	SCLK (Low) to PCLK ↑ (Inst. 3 & 13)		2.0	–	2.5	–					
	H6	C/$\overline{D}$ (Low) to PCLK ↑ (Inst. 3 & 13)		2.0	–	2.5	–					
	H7	Y to PCLK ↑ (Inst. 3)		3.0	–	3.0	–					
	H8	Y to LE		2.0	–	2.0	–					
	H9	SEL to LE		2.0	–	2.0	–					
	H10	$\overline{EN}$ to PCLK ↑		2.0	–	2.0	–					

(Continued)

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL		PARAMETER	CONDITION[1]	IDT49FCT618				IDT49FCT618A				UNIT
				COM'L.		MIL.		COM'L.		MIL.		
				MIN.[2]	MAX.	MIN.[2]	MAX.	MIN.[2]	MAX.	MIN.[2]	MAX.	
t_{PHZ} t_{PLZ}	1Z	$\overline{YOE}_{U,L}$ to Y	C_L = 50pF R_L = 500Ω	3.0	8.0	3.0	8.0					ns
	2Z	SCLK ↑ to D (Inst. 9)		3.0	9.0	3.0	9.0					
	3Z	C/$\overline{D}$ ↑ to D or Y (Inst. 9)		3.0	9.0	3.0	9.0					
	4Z	SCLK ↑ to Y ($\overline{YOE}_{U,L}$ = High Inst. 8 & 14)		3.0	9.0	3.0	9.0					
	5Z	C/$\overline{D}$ to ↑ to D or Y ($\overline{YOE}_{U,L}$ = High Inst. 14)		3.0	9.0	3.0	9.0					
	6Z	$\overline{DOE}$ to D		2.0	9.0	3.0	10.0					ns
t_{PZH} t_{PZL}	Z1	$\overline{YOE}_{U,L}$ to Y		3.0	10.0	3.0	10.0					
	Z2	C/$\overline{D}$ ↓ to D (Inst. 9)		3.0	10.0	3.0	10.0					
	Z3	C/$\overline{D}$ ↓ to Y ($\overline{YOE}_{U,L}$ = High Inst. 14)		3.0	10.0	3.0	10.0					
	Z4	$\overline{DOE}$ to D		2.0	9.0	3.0	10.0					
t_W	W1	PCLK (High & Low)		7.0	–	8.0	–					
	W2	SCLK (High & Low)		25.0	–	25.0	–					
	W3	C/$\overline{D}$ (High)		25.0	–	25.0	–					
	W4	LE (High-Low)		7.0	–	8.0	–					
	W5	$\overline{CLR}$ (Low)		7.0	–	8.0	–					

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

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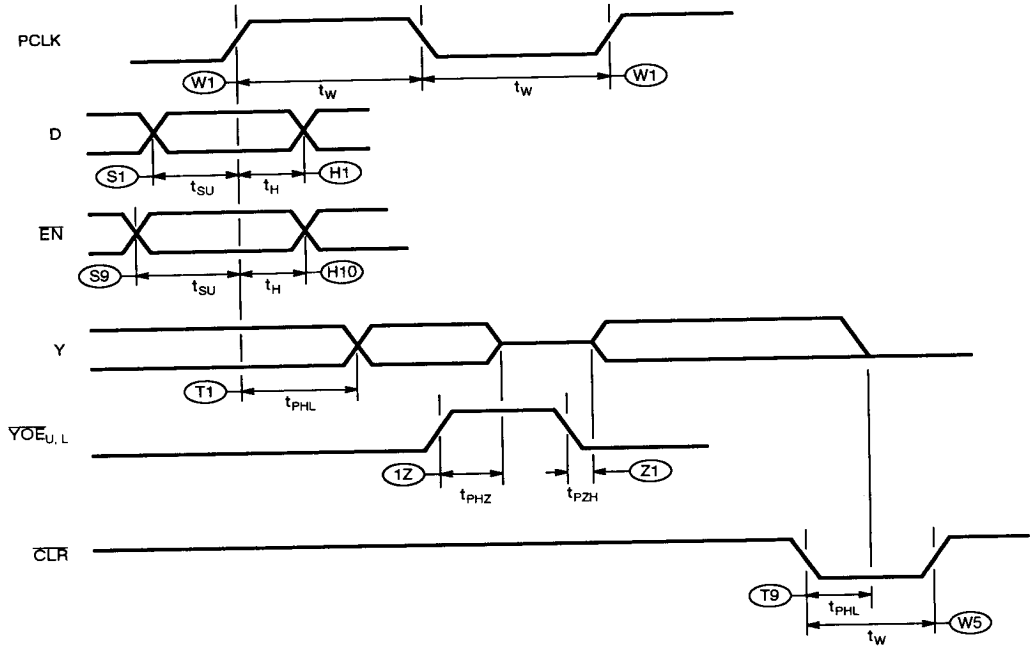
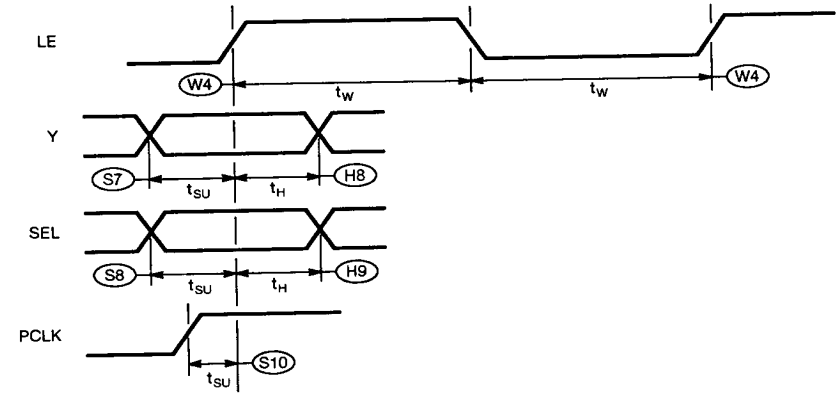
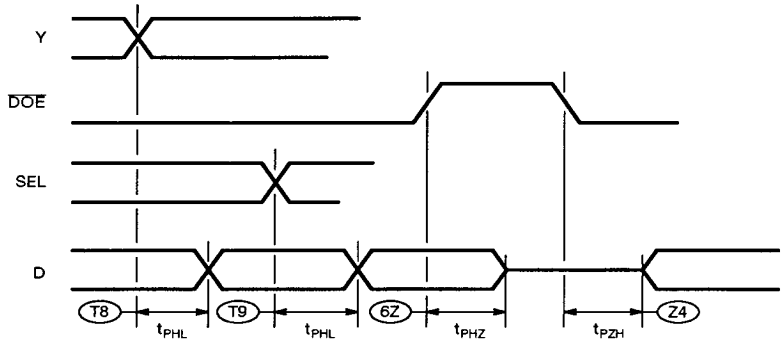
GENERAL WAVEFORMS FOR PARALLEL INPUTS AND OUTPUTS



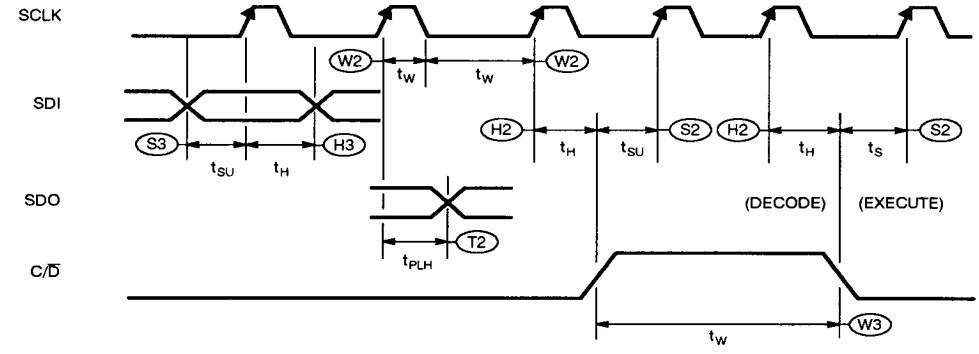
READ BACK LATCH SETUP & HOLD ITEMS



READ BACK PROPOGATION DELAYS



GENERAL WAVEFORMS FOR SERIAL PROTOCOL INPUTS AND OUTPUTS



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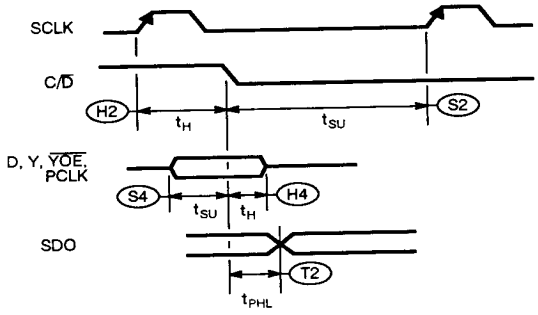
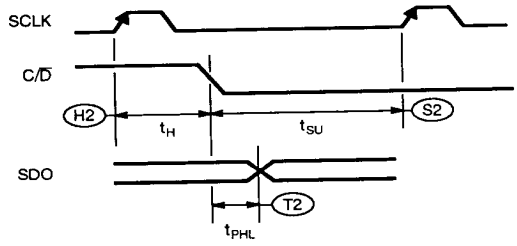
DETAILED WAVEFORMS OF SERIAL PROTOCOL OPERATIONS

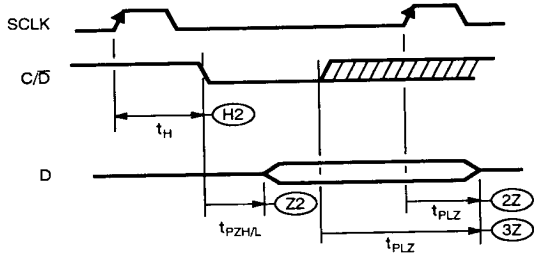
Y ⟶ SPC Data (Inst. 0)
D ⟶ SPC Data (Inst. 2)
STATUS ⟶ SPC Data (Inst. 4)



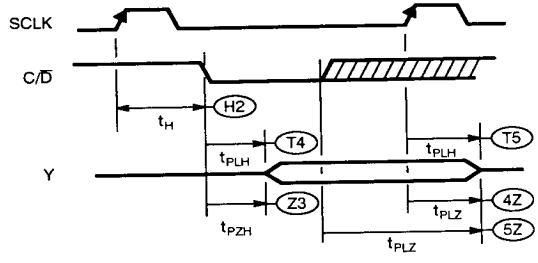
PARALLEL DATA REGISTER ⟶ SPC Data (Inst. 1)
SET SERIAL MODE (Inst. 11)
SET STUB MODE (Inst.12)



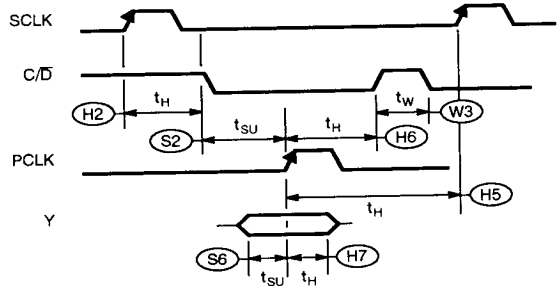
SPC Data ⟶ D (Inst. 9)



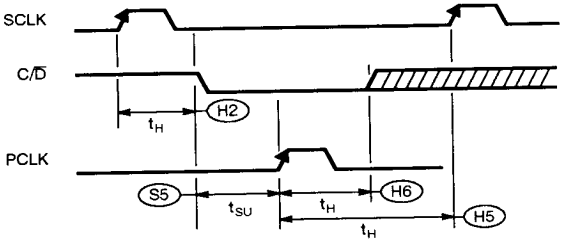
SPC Data ⟶ PARALLEL DATA REGISTER (Inst. 10)
SPC Data ⟶ Y (Inst. 8)
CONNECT D TO Y (Inst. 14)



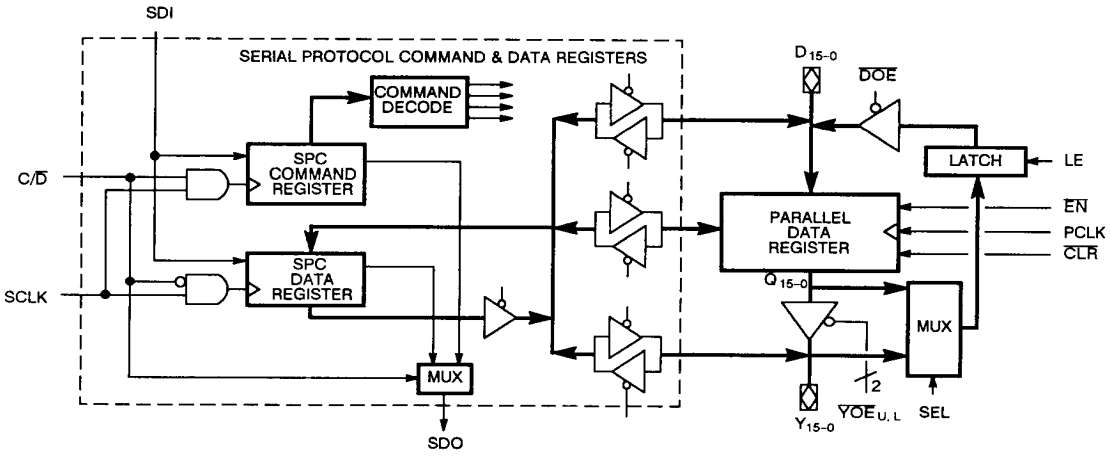
Y ⟶ SPC Data SYNCHRONOUS W/PCLK (INST.3)



SPC Data ⟶ PARALLEL DATA REGISTER SYNCHRONOUS W/PCLK (Inst. 13)



DETAILED FUNCTIONAL BLOCK DIAGRAM



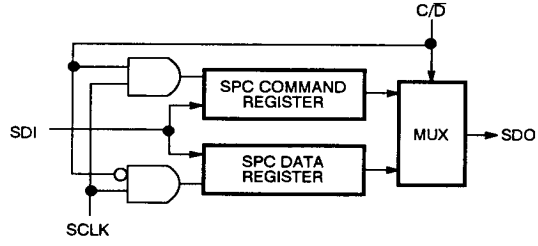
The block diagram consists of three main data paths and two logic blocks. The main data path is from the D inputs down to the parallel data register and through the Y outputs. This is the path that will be used most of the time in normal operation. For serial protocol operations, there are data paths from the Y pins into the SPC data register and control block. Coming out of this block is the data path that allows data to be put back onto the D input pins or into the parallel data register. The PCLK is used to clock the parallel data register. The $\overline{EN}$ signal is a clock enable for the 16-bit parallel data path. The $\overline{CLR}$ line offers an asynchronous 16-bit clear. $\overline{YOE}_{U,L}$ inputs are used to control the tri-state output of the Y pins.

The other main data path is a read back from the output of the 16-bit parallel data register to the D bus. This path is convenient when using the IDT49FCT618 with a processor because it provides the mechanism to read the contents of the data register. The SEL pin selects data from the internal Q bus or the data output pins Y. The LE signal controls a latch in the read back path. In this way data can be latched "on the fly" and allowed to settle before a processor reads it back on the D pins. The $\overline{DOE}$ input is a tri-state control which selects whether the D bus is an input or an output.

SPC data and commands are shifted through the SDI pin which is a serial input pin and the SDO pin which is a serial output pin. Data and commands are shifted in Least Significant Bit first, Most Significant Bit last (Y_0 = LSB, Y_{15} = MSB). The SCLK is used to shift the data through. The C/$\overline{D}$ line is used as a control input to determine whether data or command information is being shifted in.

The Serial Protocol Channel (SPC) has been optimized for the minimum number of pins and maximum flexibility. The data is passed in on a serial data input pin (SDI) and out on a serial data output pin (SDO). The transfer of the data is controlled by a serial clock (SCLK) and a command/data mode input (C/$\overline{D}$). These four pins are the basic SPC pins. To the outside, the SPC appears as two serial shift registers in parallel; one for command and the other data. The serial clock shifts data and the command/data (C/$\overline{D}$) line selects which register is being shifted. The SPC command register is used to control loading of data to and from the parallel data register with other storage elements in the device.

SPC FUNCTIONAL DESCRIPTION



With respect to executing an SPC command, there are four distinct phases: (1) data is shifted in, (2) followed by the SPC command, (3) the SPC command is executed, (4) data is shifted out. During the data mode, data is simultaneously shifted into the SPC data register while the data in the register is shifted out. During the command mode, opcode type information is shifted through the serial ports.

The command is executed when the last bit is shifted in and the C/$\overline{D}$ line is brought low. The execution phase is ended with the next serial clock edge. Execution of SPC commands is performed by stopping the SPC clock, SCLK, and lowering the C/$\overline{D}$ line from high-to-low. Later the SCLK may be transitioned from low-to-high. SPC commands and data can be shifted any time without regard for operation. During the execution phase, care must be taken that there is no conflict between the SPC operation and parallel operation. This means that if the SPC operation attempts to load the parallel data register (opcode 10) while PCLK is in transition, the results are undefined. In general, it is required that the PCLK be static during SPC operations. The synchronous commands (opcodes 3 and 13), however, allow the PCLK to run. In these operations the HIGH-to-LOW transition of the C/$\overline{D}$ line takes on the function of an arm signal in preparation for the next LOW-to-HIGH transition of the PCLK.

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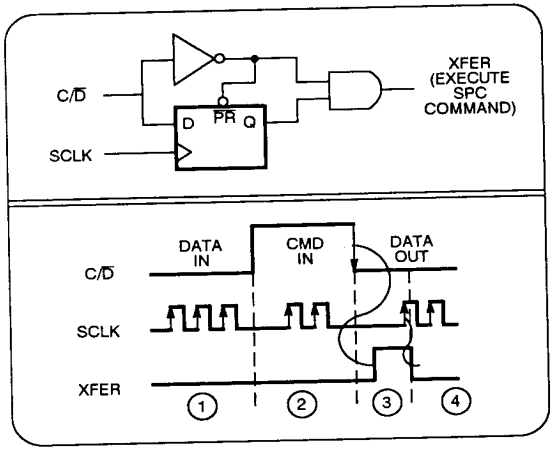


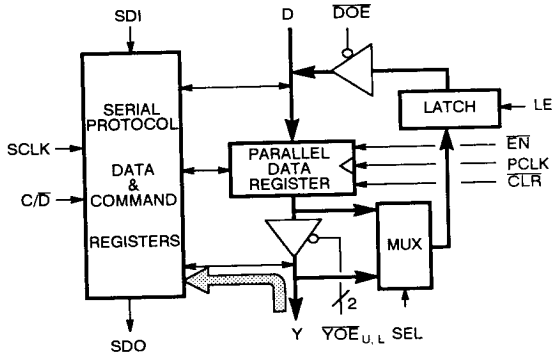
SPC COMMANDS

There are 16 possible SPC opcodes. Thirteen of these are utilized; the other three are reserved and perform NO-OP functions. The top eight opcodes, 0 through 7, are used for transferring data into the SPC data register for shifting out. The lower eight opcodes, 8 through 15, are used for transferring data from the SPC data register to other parts of the device. Two of the commands are also used for connecting the data in and out pins.

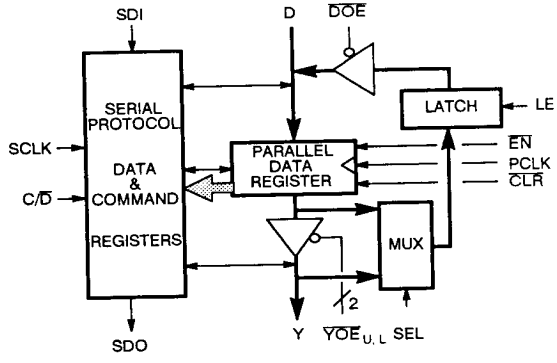
OPCODE	SPC COMMAND
0	Y to SPC Data Register
1	Parallel Data Register to SPC Data Register
2	D to SPC Data Register
3	Y to SPC Data Register Synchronous w/PCLK
4	Status ($\overline{YOE}_{U,L}$, PCLK, etc) to SPC Data Register
5-7	Reserved (NO-OP)
8	SPC Data to Y ($\overline{YOE}_{U,L}$ is overidden)
9	SPC Data to D ($\overline{DOE}$ is overidden)
10	SPC Data to Parallel Data Register
11	Select Serial Mode
12	Select Stub Mode
13	SPC Data to Y Synchronous w/PCLK
14	Connect D to Y ($\overline{YOE}_{U,L}$ is overidden)
15	NO-OP

Opcode 0 is used for transferring data from the Y output pins into the SPC data register. Opcode 1 transfers data from the output of the parallel data register into the SPC data register.

Y ⟶ SPC Data (Inst. 0)

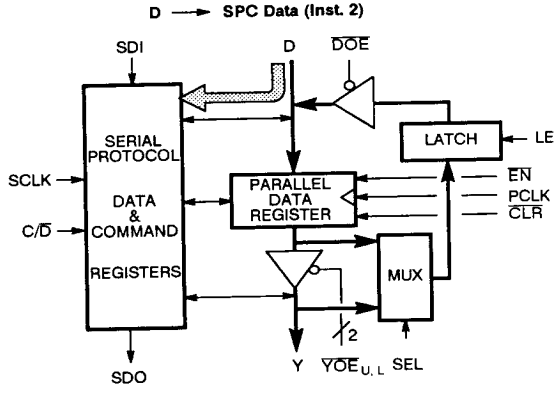


PARALLEL DATA REG ⟶ SPC Data (Inst. 1)



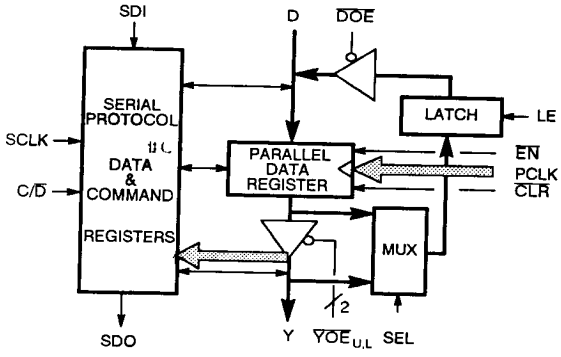
Opcode 2 transfers data which is on data input pin D into the SPC data register.

D ⟶ SPC Data (Inst. 2)



Opcode 3 transfers data on the Y pins to the SPC data register on the next PCLK, thus achieving a synchronous observation of the parallel data register in real time. This operation can be forced to repeat without shifting in a new command by pulsing C/$\overline{D}$ LOW-HIGH-LOW after each PCLK. As soon as data is shifted out using SCLK, the command is terminated and must be loaded in again.

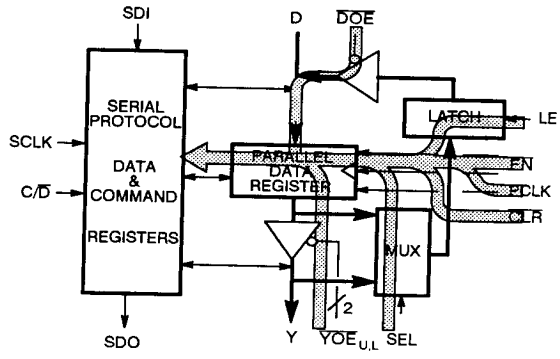
Y ⟶ SPC Data SYNCHRONOUS w/PCLK (Inst. 3)



Opcode 4 is used for loading status into the SPC data register. The format of bits is shown below.

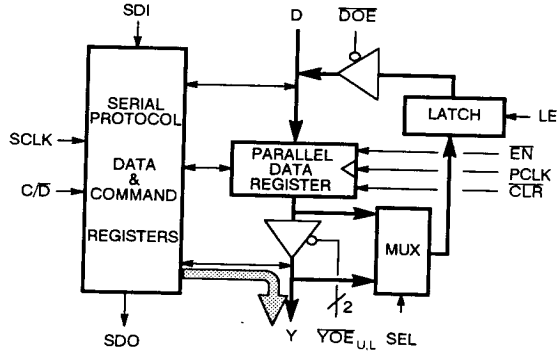
15	14	13	12	11	10	9	8	7	6	0
$\overline{DOE}$	PLCK	$\overline{YOE}_U$	LE	$\overline{EN}$	$\overline{CLR}$	$\overline{YOE}_L$		SEL		

STATUS ⟶ SPC Data (Inst. 4)



Opcodes 5 through 7 are reserved, hence designated NO-OP.

SPC Data ⟶ Y (Inst. 8)



Opcode 8 is used for transferring data directly to the Y pins. When executing opcode 8, the state of $\overline{YOE}_{U,L}$ is a don't care and data will be output even if $\overline{YOE}_{U,L}$ = HIGH. Opcode 9 is used for transferring SPC data to the D pins. Operations 8 and 9 can be temporarily suspended by raising the C/$\overline{D}$ input and resumed by lowering the C/$\overline{D}$. As soon as SCLK completes transition, the command is terminated.

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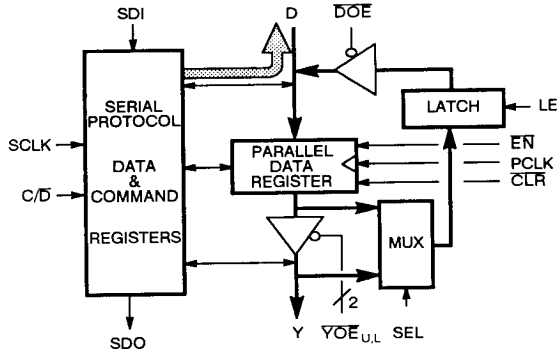
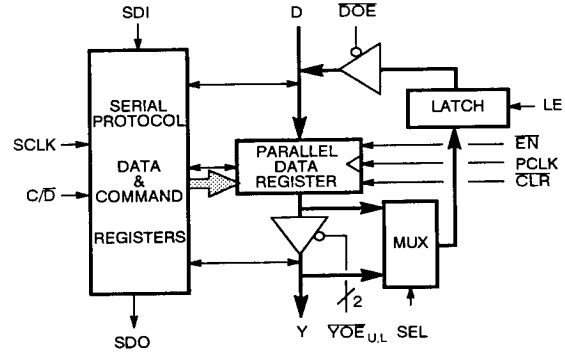
SPC Data ⟶ D (Inst. 9)



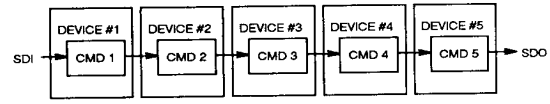
Opcode 10 is used for transferring data from the SPC Data register into the parallel data register, irrespective of the state of PCLK. However, PCLK must be static between C/D going HIGH-to-LOW and SCLK going LOW-to-HIGH.

SPC Data ⟶ PARALLEL DATA REGISTER (Inst. 10)



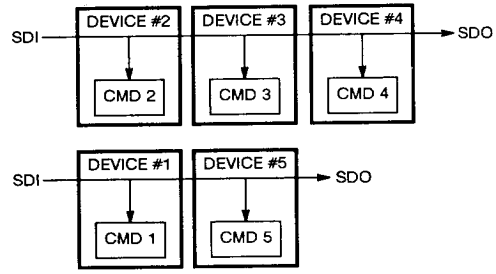
Opcodes 11 and 12 are used to set Serial and Stub mode, respectively. After executing one of these opcodes, the device remains in this mode through other Serial Protocol operations until reprogrammed using either command. The serial mode is the default mode that the IDT49FCT618 powers up in. In Serial mode, commands are shifted through the command register and then to the SDO pin. This is the typical mode used when several varieties of devices that utilize the SPC access method are employed on one serial ring.

SERIAL MODE



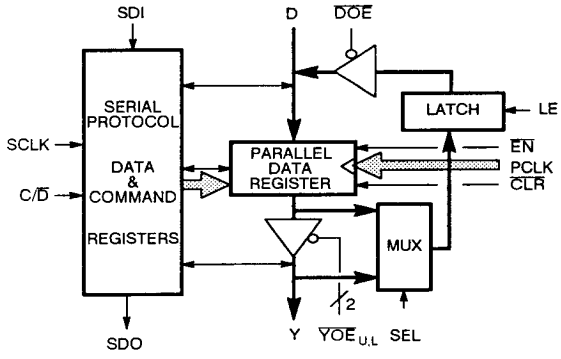
In Stub mode, SDI is connected directly to SDO. The serial input of the command register is connected to SDI. In this way, the same SPC command can be loaded into multiple devices of like type. For example, in four clock cycles the same command could be loaded into 8 IDT49FCT618s (128-bit pipeline register). Dissimilar devices must be segregated into serial scan loops of similar type as shown below (i.e., other devices from IDT that incorporate SPC). During the command phase, the serial shift clock must be slowed down to accommodate the delay from SDI to SDO through all of the devices. The slower clock is typically a small tradeoff compared to the reduced number of clock cycles.

STUB MODE

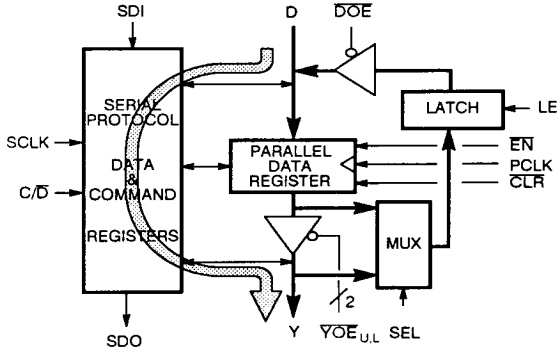


Opcode 13 transfers data from the SPC data register to the pipeline register on the next PCLK. Opcode 14 connects the D bus to the Y bus. Operation 14 can be temporarily suspended by raising the C/D input and resumed by lowering the C/D input again. The operation is terminated by SCLK.

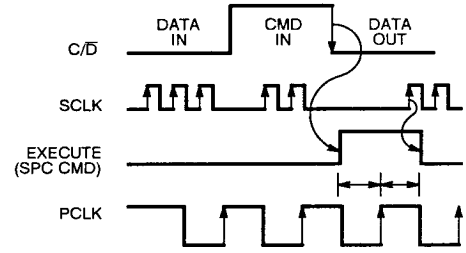
SPC Data → PARALLEL DATA REGISTER SYNCHRONOUS w/PCLK (Inst. 13)



CONNECT D TO Y (Inst. 14)



Opcodes 3 and 13 transfer data synchronous to the PCLK which means that the High-to-Low on the C/$\overline{D}$ input is an arm signal. The data and command can be shifted in while the PCLK is running. The C/$\overline{D}$ line is dropped prior to the desired PCLK edge and raised afterwards, before the next edge. Instruction 13 can be repeated many times by leaving the C/$\overline{D}$ line low during multiple transitions of the PCLK while not clocking SCLK. PCLK cycles can even be skipped by raising the C/$\overline{D}$ input during the desired clock periods. Instruction 3 can be repeated by pulsing the C/$\overline{D}$ high after each PCLK.



The ability to repeatedly execute a synchronous command can provide major benefits. For example, the synchronous read (Instruction 3, Y to SPC data) instruction could be clocked into the serial command register. Then, it could be continuously executed by pulsing the C/$\overline{D}$ line HIGH. When the whole system is stopped (PCLK quiescent), the serial data register will contain the next to the last state of the parallel data register. That value can be shifted out and the current state of the parallel data register can then be observed, allowing for the observation of two states of the parallel data register (the current and the previous).

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TYPICAL APPLICATION

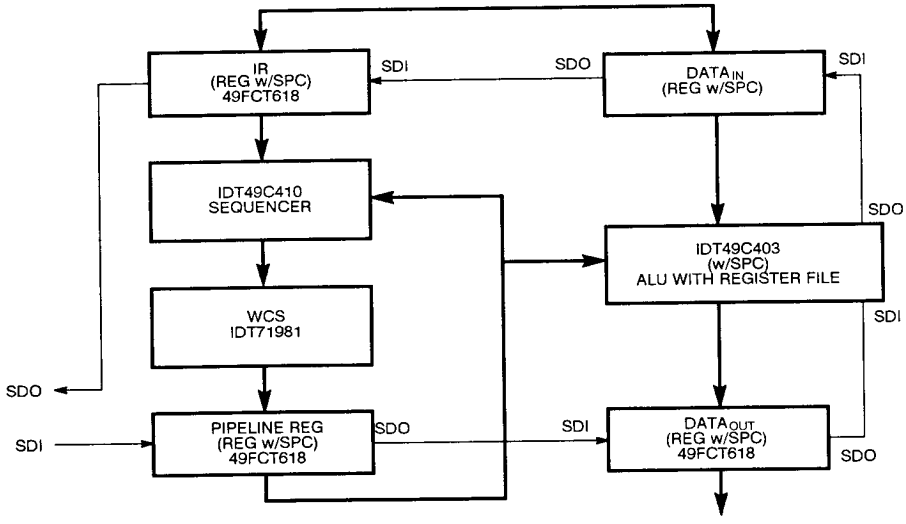
In the block diagram of the typical application, the register with SPC register is shown being used with a writable control store in a microprogrammed design. The control store can be initialized through the diagnostics path. The SPC data register with SPC is used for the instruction register going into the IDT49C410, as well as parallel data registers around the IDT49C403. In this way, the designer may use the SPC register to observe and modify the microcode coming out of the writable control store, as well as observing and being able to modify data and instructions in the overall machine. The IDT49C403 is a 16-bit version of the 2903A/203 which includes an SPC port for diagnostic and break point purposes.

The block diagram of the diagnostic ring shows how the devices with SPC Data are hooked together in a serial ring via the SDI and SDO signals. The SPC signals may be generated through registers which are hooked up to a microprocessor. This microprocessor could conceivably be an IBM PC.

As companies like IDT continue to integrate more onto each device and put each device into smaller packages such as surface mount devices, the board level testing becomes more complex for the designer and the manufacturing divisions of companies. To help this situation, SPC was invented. This allows for observation of critical signals deep within the system. During system test when an error is observed, these signals may be modified in order to zero in on the fault in the system.

SPC is primarily a scheme utilizing only a few pins (4) to examine and alter the internal state of a system for the purpose of monitoring and diagnosing system faults. It can be used at many points in the life of a product: design debug and verification, manufacturing test and field service. This document describes a serial diagnostic scheme which was developed at IDT and will be used in future VLSI logic devices designed by IDT.

TYPICAL MICROPROGRAM APPLICATION WITH SPC™



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