Integrated Device Technology, Inc.

HIGH-SPEED OCTAL REGISTER WITH SPC™

PRELIMINARY
IDT49FCT818
IDT49FCT818A

FEATURES:

- High-speed, non-inverting 8 bit parallel register for any data path, control path or pipelining application
- New, unique command capability which allows for multiplicity of diagnostic functions
- High-speed Serial Protocol Channel (SPC™) provides
  - Controllability:
    - Serially scan in new machine state
    - Load new machine state "on the fly"
    - Temporarily force Y output bus
    - Temporarily force data out the D input bus (as in loading WCS)
  - Observability:
    - Directly observe D and Y buses
    - Serially scan out current machine state
    - Capture machine state "on the fly"
- I_{OL} = 32mA (commercial) and 24mA (military)
- CMOS power levels (1mW typ. static)
- TTL input and output level compatible
- CMOS output level compatible
- Substantially lower input current levels than 29818 and 54/74AS818 (5µA max.)
- Available in plastic and sidebraze DIP, SOIC, LCC and CERPACK
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

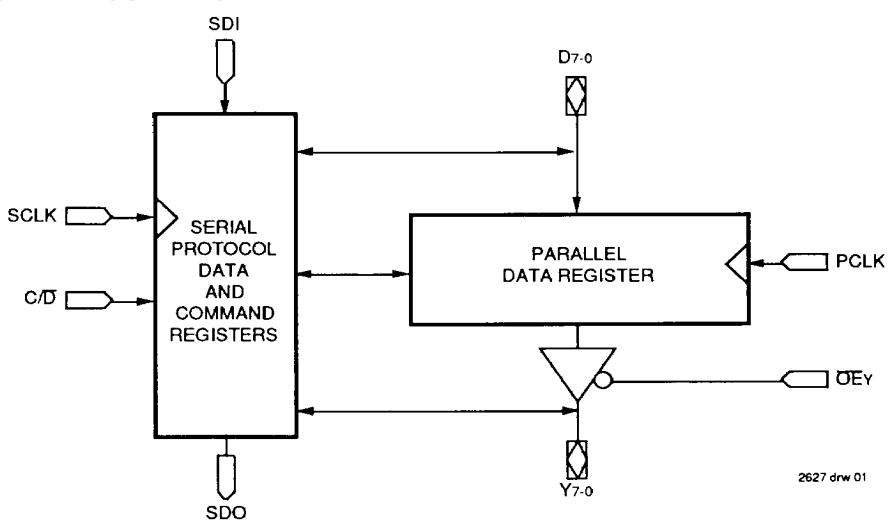
The IDT49FCT818 is a high-speed, general purpose octal register with Serial Protocol Channel (SPC). The D-to-Y path of the octal register provides a data path that is designed for normal system operation wherever a high-speed clocked register is required.

The SPC command and data registers are used to observe and control the octal data register for diagnostic purposes. The SPC command and data registers can be accessed while the system is performing normal system function. Diagnostic operations can then be performed "on the fly", synchronous with the system clock, or can be performed in the "single step" environment. The SPC port utilizes serial data in and out pins (a concept originated at IBM) which can participate in a serial scan loop throughout the system. Here normal data, address, status and control registers are replaced with the IDT49FCT818. The loop can be used to scan in a complete test routine starting point (data, address, etc). Then, after a specified number of clock cycles, the data can be clocked out and compared with expected results.

As well as diagnostic operations, SPC can be used for initializing at power-on time functions such as Writable Control Store (WCS).

6

FUNCTIONAL BLOCK DIAGRAM



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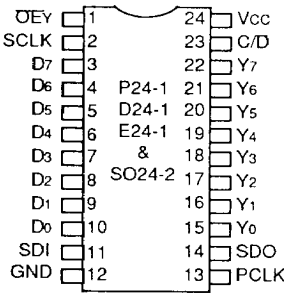
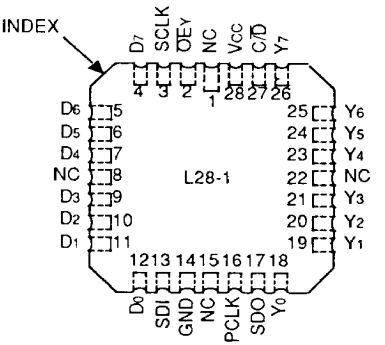
PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW

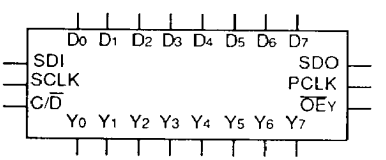
2627 drw 02



LCC
TOP VIEW

2627 drw 03

LOGIC SYMBOL



2627 drw 04

FUNCTION TABLE[1]

C/D	SCLK	PCLK	OEY	D	Y	Function
X	X	X	H	X	High Z	Tri-state Y
X	X	↓	L	H	H	Clock D to Y
X	X	↓	L	L	L	Clock D to Y
H	↓	X	X	X	X	Shift Bit into SPC Command Register
L	↓	X	X	X	X	Shift Bit into SPC Data Register
↘	↓	H or L (Static)	X	X	X	Excute SPC Command during time Between C/D & SCLK

2627 tbl 01

NOTES:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't care
   Z = High Impedance
   ↘ = Transition, High-to-Low or Low-to-High

PIN DESCRIPTION

Pin Names	I/O	Description
PCLK	I	Parallel Data Register Clock
D7-0	I/O	Parallel Data Register Input Pins (D0 = LSB, D7 = MSB)
Y7-0	I/O	Parallel Data Register Output Pins (Y0 = LSB, Y7 = MSB)
OEY	I	Output Enable for Y Bus (Overidden by SPC Inst. 8 and 14)
SDI	I	Serial Data In for SPC Operation, Data and Command Shifts in the Least Significant Bit First
SDO	O	Serial Data Out for SPC Operation, Data and Command Shifts Out the Least Significant Bit First
C/D	I	Mode Control for SPC
SCLK	I	Serial Shift Clock for SPC Operations

2627 tbl 02

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC}	–0.5 to V_{CC}	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	0.5	0.5	W
I_{OUT}	DC Output Current	120	120	mA

NOTES: 2627 tbl 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Input and Vcc terminals only.
3. Outputs and I/O terminals only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	8	12	pF

NOTE: 2627 tbl 04
1. This parameter is guaranteed by characterization and not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified: V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V
Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions(1)		Min.	Typ.(2)	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	—	—	5	µA
	(Except I/O pins)		V_I = 2.7V	—	—	5(4)	
I_{IL}	Input LOW Current		V_I = 0.5V	—	—	–5(4)	
	(Except I/O pins)		V_I = GND	—	—	–5	
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	—	—	15	µA
	(I/O pins only)		V_I = 2.7V	—	—	15(4)	
I_{IL}	Input LOW Current		V_I = 0.5V	—	—	–15(4)	
	(I/O pins only)		V_I = GND	—	—	–15	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_N = –18mA		—	–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.(3), V_O = GND		–60	–120	—	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = –32µA		V_{HC}	V_{CC}	—	V
		V_{CC} = Min.	I_{OH} = –300µA	V_{HC}	V_{CC}	—	
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –12mA MIL.	2.4	4.3	—	
			I_{OH} = –15mA COM'L.	2.4	4.3	—	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		—	GND	V_{LC}	V
		V_{CC} = Min.	I_{OL} = 300µA	—	GND	V_{LC}(4)	
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA MIL.	—	0.3	0.5	
			I_{OL} = 32mA COM'L.	—	0.3	0.5	

NOTES: 2627 tbl 05
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

V_{LC} = 0.2V; V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$		—	0.2	1.5	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open $\overline{OE}_Y$ = GND One Input Toggling 50% Duty Cycle	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[5]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}_Y$ = GND	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	1.7	4.0	mA
		One Bit Toggling at f_i = 5MHz 50% Duty Cycle SCLK = C/$\overline{D}$ = V_{CC} SDI = V_{CC}	V_{IN} = 3.4V V_{IN} = GND	—	2.2	6.0	
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle $\overline{OE}_Y$ = GND	$V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (FCT)	—	4.0	7.8[5]	
		Eight Bits Toggling at f_i = 2.5MHz 50% Duty Cycle SCLK = C/$\overline{D}$ = V_{CC} SDI = V_{CC}	V_{IN} = 3.4V V_{IN} = GND	—	6.2	16.8[5]	

2627 tbl 06

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

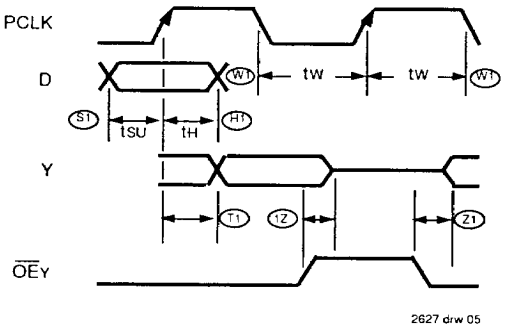
Symbol		Parameter	Condition[1]	IDT54/74FCT818				IDT54/74FCT818A				Unit
				Com'l.		Mil.		Com'l.		Mil.		
				Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
tPHL	T1	PCLK ≠ to Y	CL = 50pF	3.0	12.5	3.0	14.0	3.0	9.0	3.0	10.0	ns
tPLH	T2	SCLK ≠ to SDO	RL = 500Ω	3.0	20.0	3.0	22.0	3.0	14.0	3.0	15.0	
	T3	SDI to SDO (in stub mode)		3.0	20.0	3.0	22.0	3.0	14.0	3.0	15.0	
	T4	C/D Øto Y (OEY = Low Inst. 8 & 14)		3.0	16.0	3.0	18.0	3.0	13.0	3.0	14.0	
	T5	SCLK ≠ to Y (OEY = Low, Inst. 8 & 14)		3.0	20.0	3.0	22.0	3.0	13.0	3.0	14.0	
	T6	C/D to SDO (Inst. 0, 1, 2 & 4)		3.0	12.5	3.0	14.0	3.0	10.0	3.0	11.0	
tSU	S1	D to PCLK ≠		2.5	—	3.0	—	2.5	—	3.0	—	ns
	S2	C/D to SCLK ≠		12.0	—	14.0	—	12.0	—	14.0	—	
	S3	SDI to SCLK ≠		4.0	—	5.0	—	4.0	—	5.0	—	
	S4	Y or D to C/D Ø (Inst. 0, 2 & 4)		2.0	—	2.5	—	2.0	—	2.5	—	
	S5	C/D (Low) to PCLK ≠ (Inst. 3 & 13)		8.0	—	9.0	—	8.0	—	9.0	—	
	S6	Y to PCLK ≠ (Inst. 3)		1.0	—	1.5	—	1.0	—	1.5	—	
tH	H1	D to PCLK ≠		2.0	—	2.5	—	2.0	—	2.5	—	ns
	H2	C/D to SCLK Ø		12.0	—	14.0	—	12.0	—	14.0	—	
	H3	SDI to SCLK ≠		1.0	—	1.0	—	1.0	—	1.0	—	
	H4	Y or D to C/D Ø (Inst. 0, 2 & 4)		2.0	—	2.5	—	2.0	—	2.5	—	
	H5	SCLK (Low) to PCLK ≠ (Inst. 3 & 13)		2.0	—	2.5	—	2.0	—	2.5	—	
	H6	C/D (Low) to PCLK ≠ (Inst. 3 & 13)		2.0	—	2.5	—	2.0	—	2.5	—	
	H7	Y to PCLK ≠ (Inst. 3)		4.5	—	5.0	—	4.5	—	5.0	—	
tPHZ	1Z	OEY to Y		3.0	10.0	3.0	11.0	3.0	8.0	3.0	9.0	ns
tPLZ	2Z	SCLK ≠ to D (Inst. 5 & 9)		3.0	13.0	3.0	14.0	3.0	10.0	3.0	11.0	
	3Z	C/D ≠ to D (Inst. 5 & 9)		3.0	13.0	3.0	14.0	3.0	10.0	3.0	11.0	
	4Z	SCLK ≠ to Y (OEY = High Inst. 8 & 14)		3.0	13.0	3.0	14.0	3.0	10.0	3.0	11.0	
	5Z	C/D ≠ to Y (OEY = High Inst. 14)		3.0	13.0	3.0	14.0	3.0	10.0	3.0	11.0	
tPZH	Z1	OEY to Y		3.0	11.0	3.0	12.0	3.0	9.0	3.0	10.0	ns
tPZL	Z2	C/D Øto D (Inst. 5 & 9)		3.0	14.0	3.0	15.0	3.0	10.0	3.0	11.0	
	Z3	C/D Øto Y (OEY = High Inst. 14)		3.0	14.0	3.0	15.0	3.0	10.0	3.0	11.0	
tW	W1	PCLK (High & Low)		7.0	—	8.0	—	7.0	—	8.0	—	ns
	W2	SCLK (High & Low)		25.0	—	25.0	—	25.0	—	25.0	—	
	W3	C/D (High)		25.0	—	25.0	—	25.0	—	25.0	—	

NOTES:

2627 tbl 07

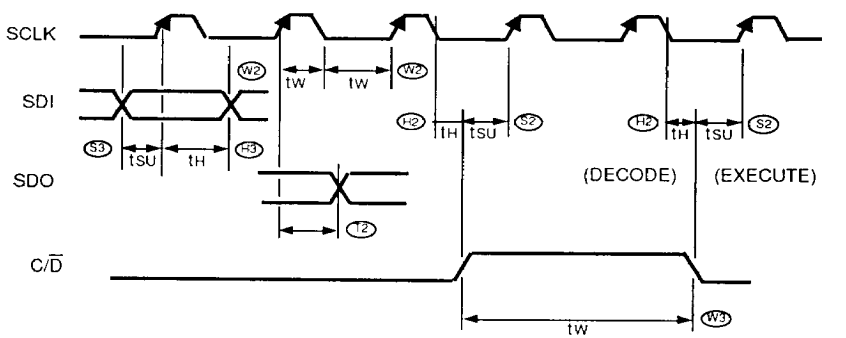
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

GENERAL AC WAVEFORMS FOR PARALLEL INPUTS AND OUTPUTS



2627 drw 05

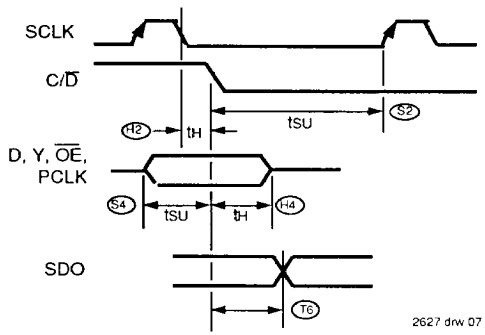
GENERAL AC WAVEFORMS FOR SERIAL PROTOCOL INPUTS AND OUTPUTS



2627 drw 06

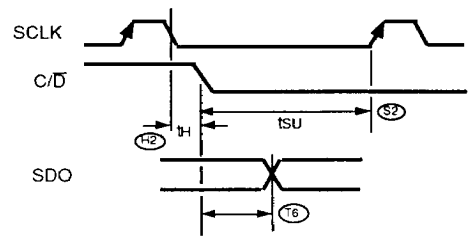
DETAILED WAVEFORMS FOR SERIAL PROTOCOL OPERATIONS

Y ⟶ SPC Data (Inst. 0)
D ⟶ SPC Data (Inst. 2)
Status ⟶ SPC Data (Inst. 4)



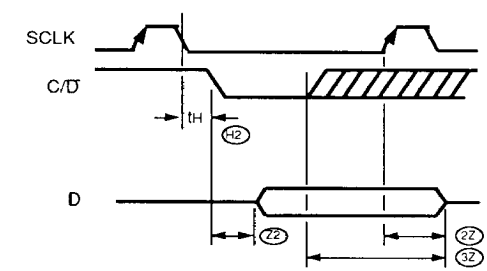
2627 drw 07

PARALLEL DATA REGISTER ⟶ SPC Data (Inst. 1)
SET SERIAL MODE (Inst. 11)
SET STUB MODE (Inst. 12)



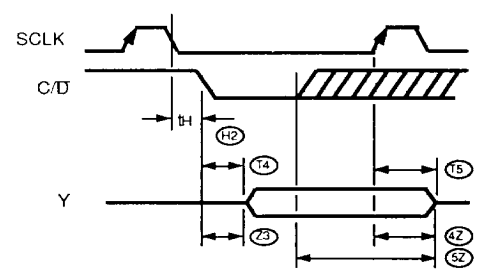
2627 drw 08

CONNECT Y TO D (Inst. 5)
SPC Data ⟶ D (Inst. 9)



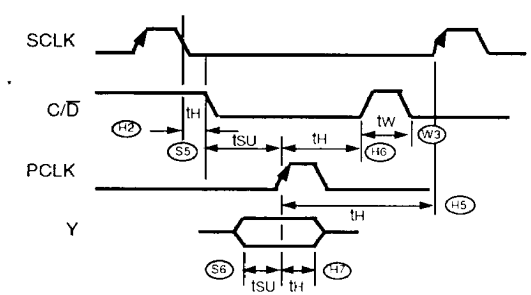
2627 drw 09

SPC Data ⟶ PARALLEL DATA REGISTER (Inst. 10)
SPC Data ⟶ Y (Inst. 8)
CONNECT D TO Y (Inst. 14)



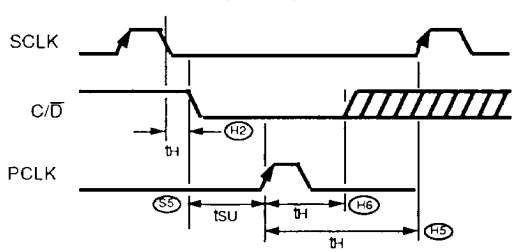
2627 drw 10

Y ⟶ SPC Data SYNCHRONOUS W/PCLK (Inst. 3)



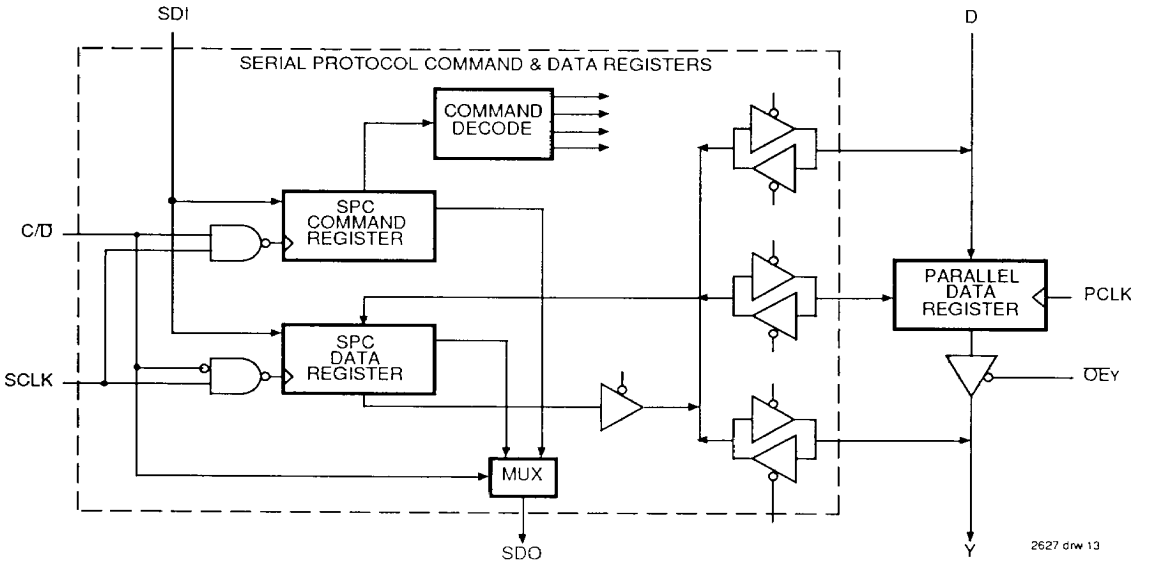
2627 drw 11

SPC Data ⟶ PARALLEL DATA REGISTER SYNCHRONOUS W/ PCLK (Inst. 13)

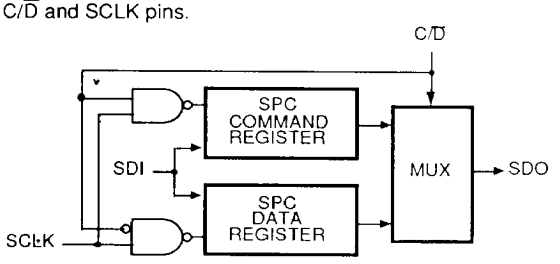


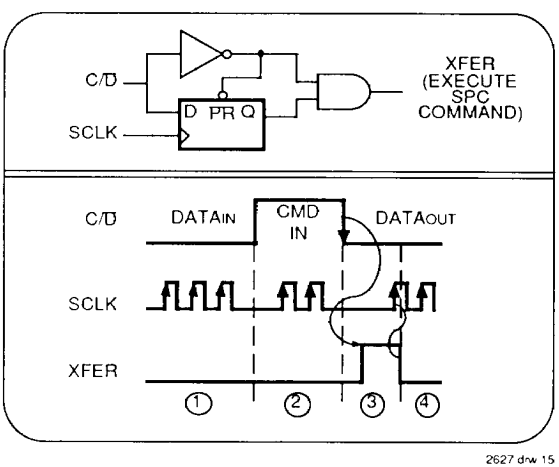
2627 drw 12

DETAILED FUNCTIONAL BLOCK DIAGRAM



The detailed block diagram consists of two main elements: the parallel data register and the SPC data /command registers. The main data path is from the D inputs down to the data register and through the Y outputs. This path is typically used during standard operations. For diagnostic or systems initialization, the internal SPC data path is used. This path allows access between the SPC data and command registers and the standard data path, pins and data register. The SPC data and command registers are accessed via the SDI, SDO, C/$\overline{D}$ and SCLK pins.





SPC FUNCTIONAL DESCRIPTION

The Serial Protocol Channel (SPC) has been optimized for the minimum number of pins and the maximum flexibility. The data is passed in on a Serial Data Input pin (SDI) and out on a Serial Data Output pin (SDO). The transfer of the data is controlled by a Serial Clock (SCLK) and a Command/Data mode input (C/$\overline{D}$). These four pins are the basic SPC pins. To the outside, the SPC appears as two serial shift registers in parallel – one for command and the other data. The serial clock shifts data and the Command/Data (C/$\overline{D}$) line selects which register is being shifted. The command register is used to control loading of data to and from the data register with other storage elements in the device.

With respect to executing an SPC command, there are four distinct phases: (1) data is shifted in, (2) followed by the command, (3) the command is executed, and (4) data is shifted out. During the data mode, data is simultaneously shifted into the serial data register while the data in the register is shifted out. During the command mode, opcode-type information is shifted through the serial ports. The command

is executed when the last bit is shifted in and the C/$\overline{D}$ line is brought LOW. The execution phase is ended with the next serial clock edge.

SPC data and commands are shifted in through the SDI pin, which is a serial input pin, and out through the SDO pin, which is a serial output pin. Data and commands are shifted in Least Significant Bit first; Most Significant Bit last (Y_0 = LSB, Y_7 = MSB). Execution of SPC commands is performed by stopping the shift clock, SCLK, and lowering the C/$\overline{D}$ line from HIGH-to-LOW. Later SCLK may then be transitioned from LOW-to-HIGH. SPC commands and data can be shifted anytime without regard for operation. During the execution phase, care must be taken that there is no conflict between the SPC operation and parallel operation. This means that if the SPC operation attempts to load the parallel data register (opcode 10) while PCLK is in transition, the results are undefined. In general, it is required that PCLK be static during SPC operations. The synchronous commands (opcode 3 and 13), however, allow PCLK to run. In these operations, the HIGH-to-LOW transition of the C/$\overline{D}$ line takes on the function of an arm signal in preparation for the next LOW-to-HIGH transition of PCLK.

SPC COMMANDS

There are 16 possible SPC opcodes. Fourteen of these are utilized, the other two are reserved and perform NO-OP functions. The top eight opcodes, 0 through 7, are reserved for transferring data into the SPC data register for shifting out. The lower eight opcodes, 8 through 15, are used for transferring data from the SPC data register to other parts of the device. Two of the commands are also used for connecting the data in and out pins.

Opcode	SPC Command
0	Y to SPC Data Register
1	Parallel Data Register to SPC Data Register
2	D to SPC Data Register
3	Y to SPC Data Register Synchronous w/PCLK
4	Status ($\overline{OE}_Y$, PCLK) to SPC Data Register
5	Connect Y to D
6-7	Reserved (NO-OP)
8	SPC Data to Y ($\overline{OE}_Y$ is Overidden)
9	SPC Data to D
10	SPC Data to Parallel Data Register
11	Select Serial Mode
12	Select Stub Mode
13	SPC Data to Parallel Data Register Synchronous w/PCLK
14	Connect D to Y ($\overline{OE}_Y$ is Overidden)
15	NO-OP

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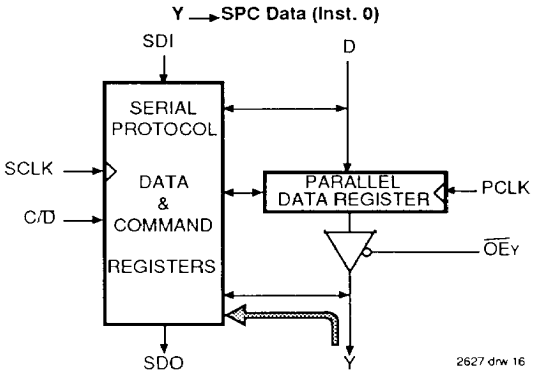
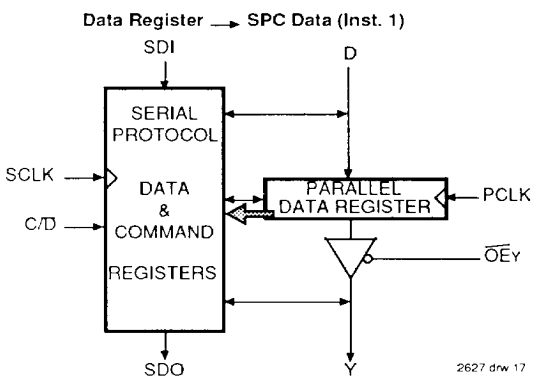
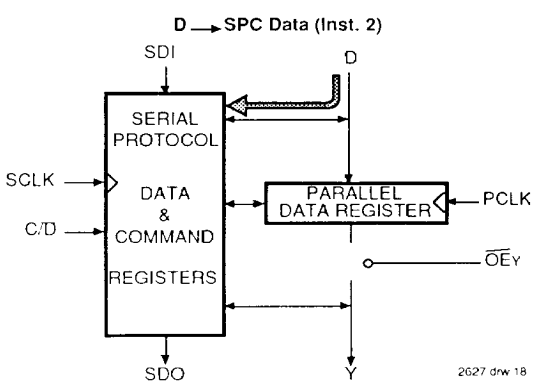
Opcode 0 is used for transferring data from the Y output pins into the SPC data register. Opcode 1 transfers data from the output of the parallel data register, before the tri-state gate, into the SPC data register. Opcode 2 transfers data from the D input pins into the SPC data register.

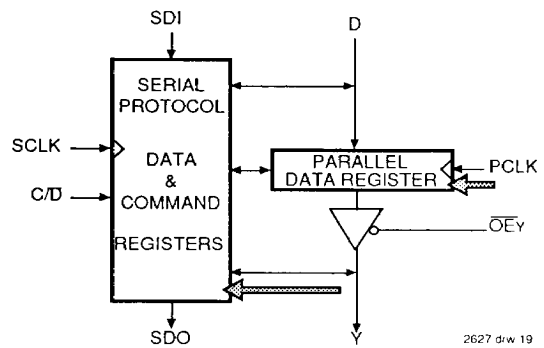




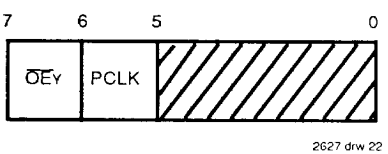


Opcode 3 transfers data on the Y pins to the SPC data register on the next PCLK, thus achieving a synchronous observation of the Y data pins in real time. This operation can be forced to repeat without shifting in a new command by pulsing C/$\overline{D}$ LOW-HIGH-LOW after each PCLK. As soon as data is shifted out using SCLK, the command is terminated and must be loaded in again.

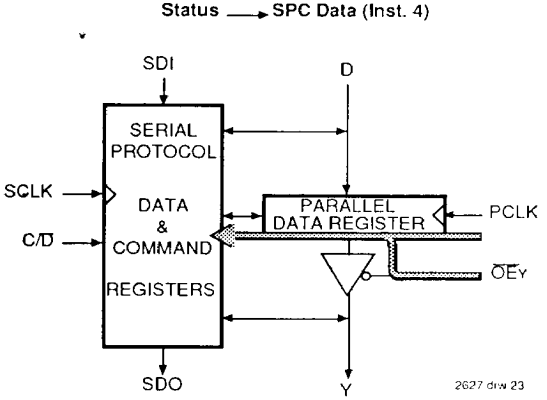
Y → SPC Data Synchronous w/PCLK (Inst. 3)



Opcode 4 is used for loading status into the SPC data register. The format of bits is shown below.

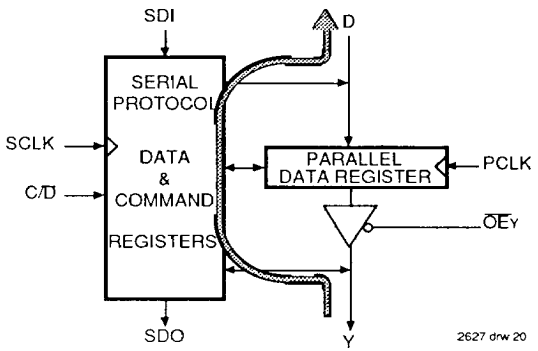


Status → SPC Data (Inst. 4)

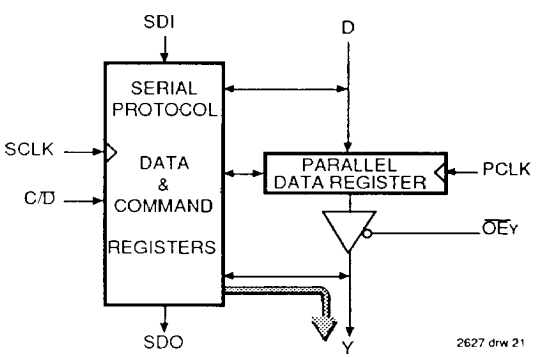


Opcode 5 connects Y to D. Opcodes 6 and 7 are reserved, hence designated NO-OP.

Connect Y to D (Inst. 5)

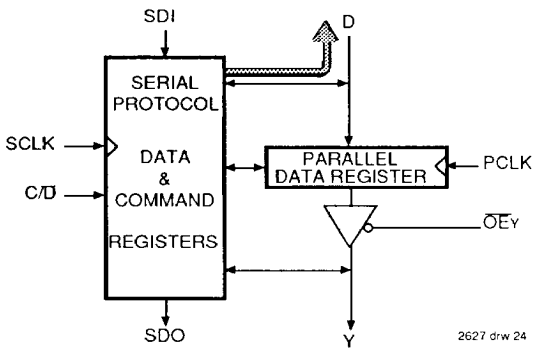


SPC Data → Y (Inst. 8)



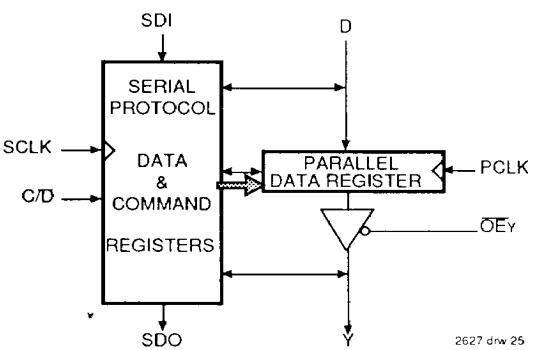
Opcode 8 is used for transferring SPC data directly to the Y pins. When executing opcode 8, the state of $\overline{OE}_Y$ is a "do not care"; that is, data will be output even if $\overline{OE}_Y$ = HIGH. Opcode 9 is used for transferring SPC data to the D pins. Operands 8 and 9 can be temporarily suspended by raising the C/$\overline{D}$ input and resumed by lowering C/$\overline{D}$. As soon as SCLK completes its LOW-to-HIGH transition, the command is terminated.

SPC Data ⟶ D (Inst. 9)



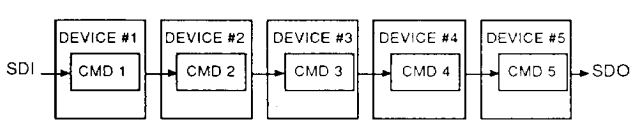
Opcode 10 is used for transferring data from the SPC data register into the parallel data register, irrespective of the state of PCLK. However, PCLK must be static between C/$\overline{D}$ going HIGH-to-LOW and SCLK going LOW-to-HIGH.

SPC Data ⟶ Parallel Data Register (Inst. 10)



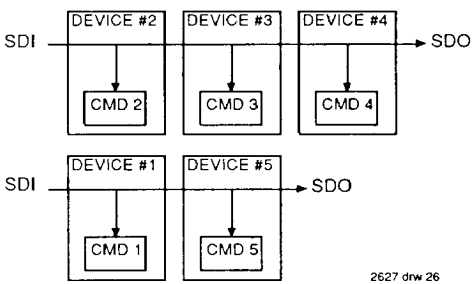
Opcodes 11 and 12 are used to set Serial and Stub Mode, respectively. After executing one of these opcodes, the device remains in this mode until programmed otherwise. The Serial mode is the default mode that the IDT49FCT818 powers up in. In Serial mode, commands are shifted through the SPC command register and then to the SDO pin. This is the typical mode used when several varieties of devices that utilize the SPC access method are employed on one serial ring.

SERIAL MODE



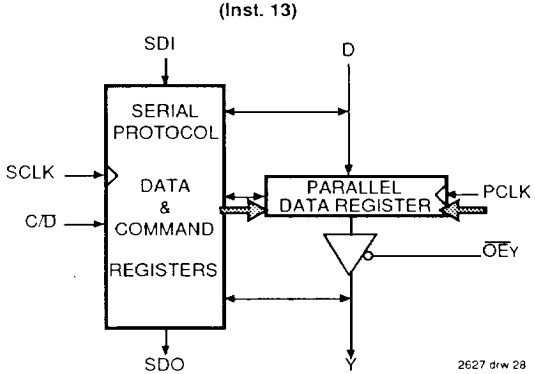
In Stub mode, SDI is connected directly to SDO. In this way, the same diagnostic command can be loaded into multiple devices of like type. For example, in four clock cycles the same command could be loaded into 8 IDT49FCT818s (64-bit pipeline register). Dissimilar devices must be segregated into serial scan loops of similar type, as shown below. During the command phase, the serial shift clock must be slowed down to accommodate the delay from SDI to SDO through all of the devices. The slower clock is typically a small tradeoff compared to the reduced number of clock cycles.

STUB MODE



Opcode 13 transfers data from the SPC data register to the parallel data register on the next PCLK. Opcode 14 connects the D bus to the Y. Operation 14 can be temporarily suspended by raising the C/$\overline{D}$ input and resumed by lowering the C/$\overline{D}$ input again. The operation is terminated by SCLK.

SPC Data ⟶ Parallel Data Register Synchronous w/PCLK (Inst. 13)



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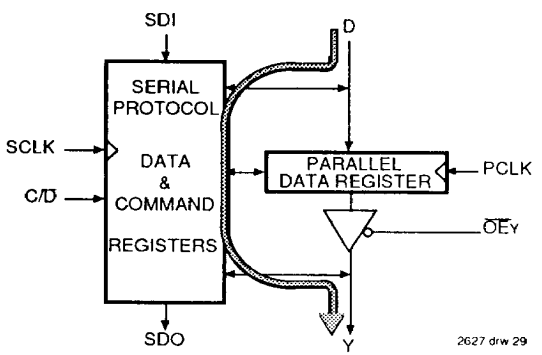
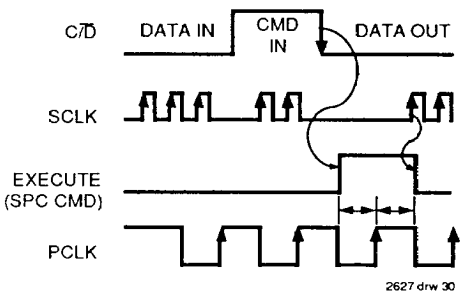
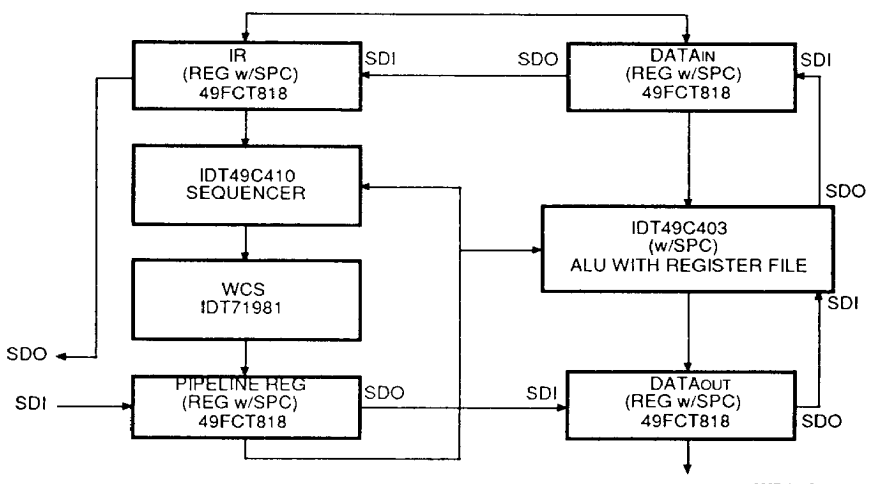
Opcodes 3 and 13 transfer data synchronous to PCLK which means that the HIGH-to-LOW on the C/$\overline{D}$ input is an arm signal. The data and command can be shifted in while PCLK is running. The C/$\overline{D}$ line is dropped prior to the desired PCLK edge and raised before the next edge. Instruction 13 can be repeated over many times by leaving the C/$\overline{D}$ line LOW during multiple transitions of PCLK while not clocking SCLK. PCLK cycles can even be skipped by raising the C/$\overline{D}$ input during the desired clock periods. Instruction 3 can be repeated by pulsing C/$\overline{D}$ high after each PCLK. The ability to continuously execute a synchronous command can provide major benefits. For example, the synchronous read (Instruction 3, Y to SPC data) instruction could be clocked into the SPC command register. Then, it could be continuously executed by pulsing the C/$\overline{D}$ line HIGH. When the whole system is stopped (PCLK quiescent), the serial data register will contain the next to the last state of the parallel data register. That value can be shifted out and the current state of the parallel register can then be observed, allowing for the observation of two states of the parallel register (the current and the previous).

Connect D to Y (Inst. 14)





TYPICAL MICROPROGRAM APPLICATION WITH SPC™



TYPICAL APPLICATION

In the block diagram of the typical application, the SPC data register is shown being used with a writable control store in a microprogrammed design. The control store can be initialized through the diagnostic path. The SPC data register is used for the instruction register going into the IDT49C410, as well as for data registers around the IDT49C403. In this way, the designer may use the SPC data register to observe and modify the microcode coming out of the writable control store, as well as observing and being able to modify data and instructions in the overall machine. The IDT49C403 is a 16-bit version of the 2903A/203 which includes an SPC port for diagnostic and break point purposes.

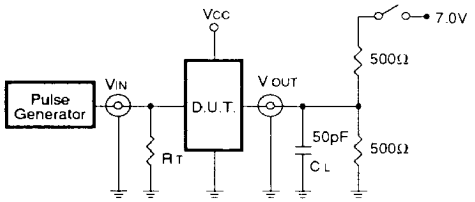
The block diagram of the diagnostics ring shows how devices with diagnostics are hooked together in a serial ring via the SDI and SDO signals. The diagnostics signals may be generated through registers which are hooked up to a microprocessor. This microprocessor could conceivably be an IBM PC.

As companies like IDT continue to integrate more onto each device and put each device into smaller packages such as surface mount devices, the board level testing becomes more complex for the designer and the manufacturing divisions of companies. To help this situation, serial diagnostics was invented. This allows for observation of critical signals deep within the system. During system test when an error is observed, these signals may be modified in order to zero in on the fault in the system.

Serial diagnostics is primarily a scheme utilizing only a few pins (4) to examine and alter the internal state of a system for the purpose of monitoring and diagnosing system faults. It can be used at many points in the life of a product: design debug and verification, manufacturing test and field service. This document describes a serial diagnostic scheme which was developed at IDT and will be used in future VLSI logic devices designed by IDT.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



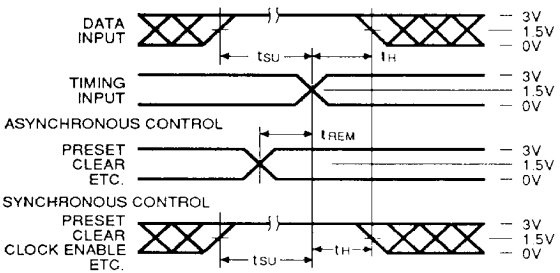
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

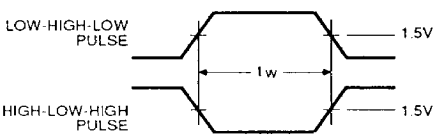
DEFINITIONS: 2627 tbl 08

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

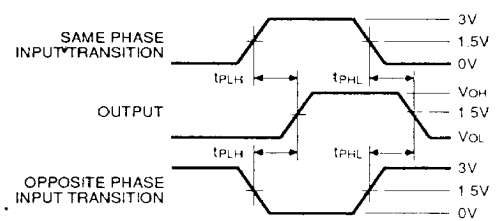
SET-UP, HOLD AND RELEASE TIMES



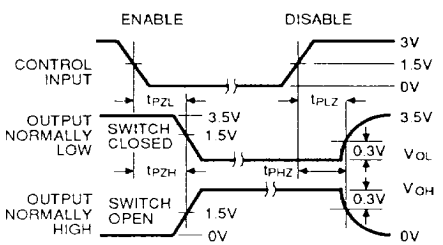
PULSE WIDTH



PROPAGATION DELAY



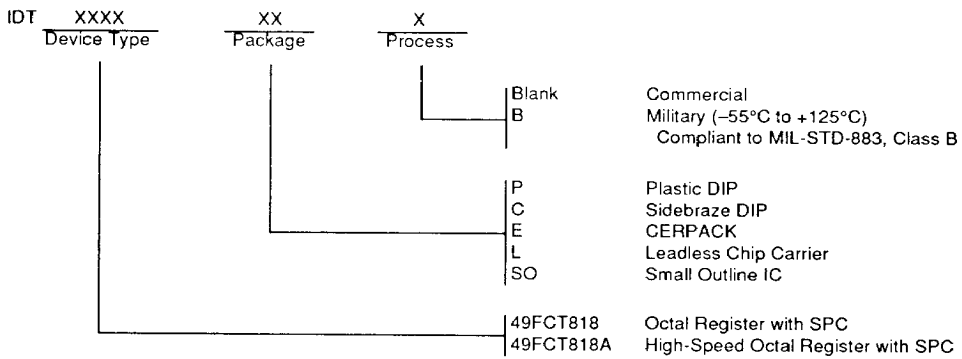
ENABLE AND DISABLE TIMES



NOTES 2627 drw 32

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0 MHz; Z_O ≤ 50Ω; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

ORDERING INFORMATION



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