Integrated Device Technology, Inc.

HIGH-SPEED CMOS SYNCHRONOUS PRESETTABLE BINARY COUNTERS

IDT54AHCT161/163

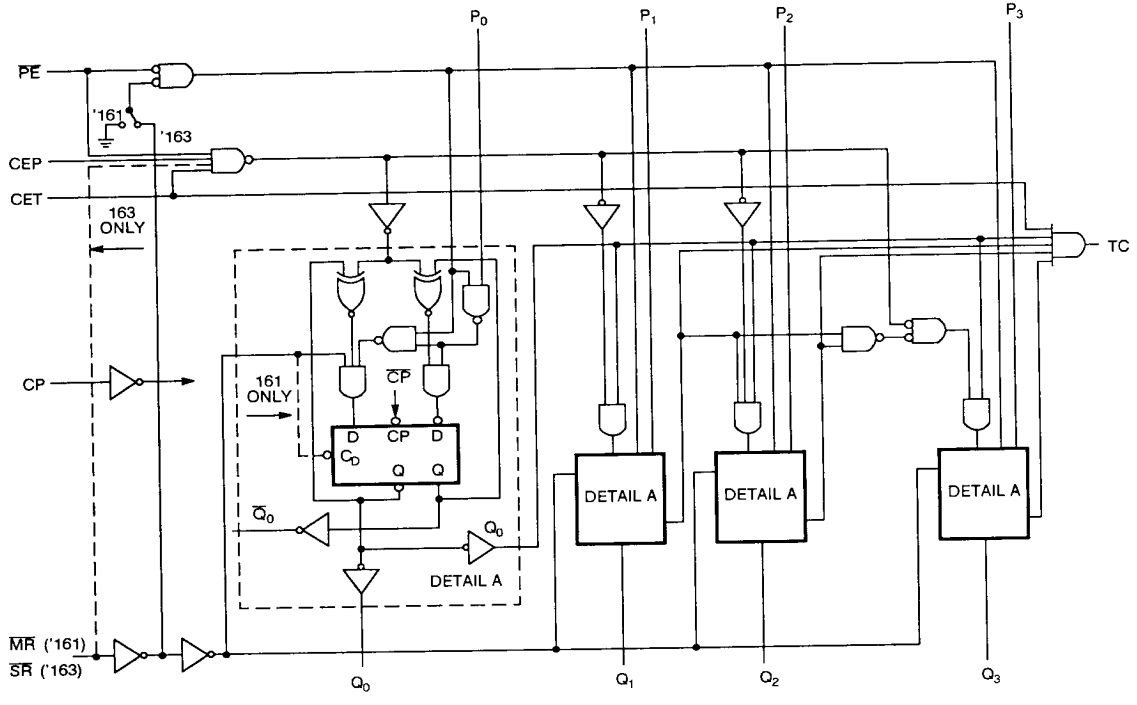
FEATURES:

- Equivalent to ALS speeds and output drive over full temperature and voltage supply extremes
- I_{OL} = 14mA over full military temperature range
- CMOS power levels (5μW typ. static)
- Both CMOS and TTL output compatible
- Substantially lower input current levels than ALS (5μA max.)
- JEDEC standard pinout for DIP and LCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT54AHCT161/163 are high-speed synchronous modulo-16 binary counters built using advanced CEMOS™, a dual metal CMOS technology. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multi-stage counters. The IDT54AHCT161 have asynchronous Master Reset inputs that override all other inputs and force the outputs LOW. The IDT54AHCT163 have synchronous Reset inputs that override counting and parallel loading and allow the outputs to be simultaneously reset on the rising edge of the clock.

FUNCTIONAL BLOCK DIAGRAM



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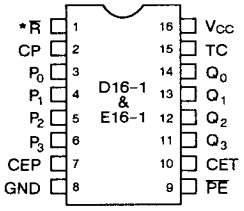
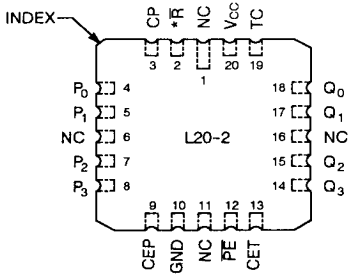
PIN CONFIGURATIONS



DIP/CERPACK
TOP VIEW



* $\overline{MR}$ for 161
* $\overline{SR}$ for 163

LCC/PLCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
T_A	Operating Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-65 to +135	°C
T_{STG}	Storage Temperature	-65 to +150	°C
P_T	Power Dissipation	0.5	W
I_{OUT}	DC Output Current	120	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER(1)	CONDITIONS	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

T_A = -55°C to +125°C
V_{CC} = 5.0V ± 10%
V_{LC} = 0.2V
V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS (1)		MIN.	TYP.(2)	MAX.	UNIT
V_{IH}	Input HIGH Level	Guaranteed Logic High Level		2.0	–	–	V
V_{IL}	Input LOW Level	Guaranteed Logic Low Level		–	–	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = V_{CC}		–	–	5	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = GND		–	–	-5	µA
I_{SC}	Short Circuit Current	V_{CC} = Max.(3)		-60	-100	–	mA
V_{OH}	Output HIGH Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OH} = -32µA		V_{HC}	V_{CC}	–	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = -150µA	V_{HC}	V_{CC}	–	
			I_{OH} = -1.0mA	2.4	4.3	–	
V_{OL}	Output LOW Voltage	V_{CC} = 3V, V_{IN} = V_{LC} or V_{HC}, I_{OL} = 300µA		–	GND	V_{LC}	V
		V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 300µA	–	GND	V_{LC}	
			I_{OL} = 14mA	–	–	0.4	

NOTES:

1. For conditions shown as max. or min. use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

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POWER SUPPLY CHARACTERISTICS (IDT54AHCT161) V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_i = 0$		–	0.001	1.5	mA
I_{CCT}	Power Supply Current per TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[4]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[5]	V_{CC} = Max. Outputs Open Count Mode CEP = CET = $\overline{MR}$ = $\overline{PE}$ = V_{HC} $P_{0-3} = V_{LC}$	CP $V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	–	0.2	0.3	mA/MHz
I_{CC}	Total Power Supply Current[4]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz, 50% Duty Cycle Count Mode CEP = CET = $\overline{MR}$ = $\overline{PE}$ = V_{HC} $P_{0-3} = V_{LC}$	CP $V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)[6]	–	1.0	3.0	mA
			CP V_{IN} = 3.4V or V_{IN} = GND[6]	–	1.3	4.0	

POWER SUPPLY CHARACTERISTICS (IDT54AHCT163) V_{LC} = 0.2V; V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS[1]		MIN.	TYP.[2]	MAX.	UNIT
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max. $V_{IN} \geq V_{HC}$; $V_{IN} \leq V_{LC}$ $f_{CP} = f_i = 0$		–	0.001	1.5	mA
I_{CCT}	Power Supply Current per TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[4]		–	0.5	2.0	mA
I_{CCD}	Dynamic Power Supply Current[5]	V_{CC} = Max. Outputs Open Count Mode CEP = CET = $\overline{SR}$ = $\overline{PE}$ = V_{HC} $P_{0-3} = V_{LC}$	CP $V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)	–	0.2	0.3	mA/MHz
I_{CC}	Total Power Supply Current[4]	V_{CC} = Max. Outputs Open f_{CP} = 1.0MHz, 50% Duty Cycle Count Mode CEP = CET = $\overline{SR}$ = $\overline{PE}$ = V_{HC} $P_{0-3} = V_{LC}$	CP $V_{IN} \geq V_{HC}$ $V_{IN} \leq V_{LC}$ (AHCT)[6]	–	1.0	3.0	mA
			CP V_{IN} = 3.4V or[6] V_{IN} = GND	–	1.3	4.0	

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. $I_{CC} = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_{CC} = I_{CCQ} + I_{CCT} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CCQ} = Quiescent Current
   I_{CCT} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = ClockFrequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.
5. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
6. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

DEFINITION OF FUNCTIONAL TERMS

PIN NAMES	DESCRIPTION
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input (Active Rising Edge)
$\overline{MR}$ ('161)	Asynchronous Master Reset Input (Active LOW)
$\overline{SR}$ ('163)	Synchronous Reset Input (Active LOW)
P_{0-3}	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Input (Active LOW)
Q_{0-3}	Flip-Flop Outputs
TC	Terminal Count Output

TRUTH TABLE

$\overline{SR}$ (1)	$\overline{PE}$	CET	CEP	ACTION ON THE RISING CLOCK EDGE (⌐)
L	X	X	X	Reset (Clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

NOTES:
1. For AHCT163 only
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

SYMBOL	PARAMETER	CONDITION (1)	TYP.	MIN. (2)	MAX.	UNIT
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input HIGH)	C_L = 50pF R_L = 500Ω	12.0	2.0	20.0	ns
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n ($\overline{PE}$ Input LOW)		12.0	2.0	20.0	ns
t_{PLH} t_{PHL}	Propagation Delay CP to TC		18.0	2.0	30.0	ns
t_{PHL} t_{PHL}	Propagation Delay CET to TC		10.0	1.5	16.0	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n (161)		10.0	2.0	27.0	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to TC		10.0	2.0	31.0	ns
t_S (H) t_S (L)	Set-up Time, HIGH or LOW P_n to CP		–	20.0	–	ns
t_H (H) t_H (L)	Hold Time, HIGH or LOW P_n to CP		–	0	–	ns
t_S (H) t_S (L)	Set-up Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP		–	20.0	–	ns
t_H (H) t_H (L)	Set-up Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP		–	0	–	ns
t_S (H) t_S (L)	Set-up Time, HIGH or LOW CEP or CET to CP		–	25.0	–	ns
t_H (H) t_H (L)	Set-up Time, HIGH or LOW CEP to CET to CP		–	0	–	ns
t_W(H) t_W(L)	Clock Pulse Width (Load) HIGH or LOW		–	20.0	–	ns
t_W(H) t_W(L)	Clock Pulse Width (Count) HIGH or LOW		–	20.0	–	ns
t_W(L)	$\overline{MR}$ Pulse Width, LOW (161)		–	20.0	–	ns
t_{REC}	Recovery Time $\overline{MR}$ to CP (161)		–	20.0	–	ns

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

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ORDERING INFORMATION