Integrated Device Technology, Inc.

# FAST CMOS UP/DOWN BINARY COUNTERS

**IDT54/74FCT193T/AT**

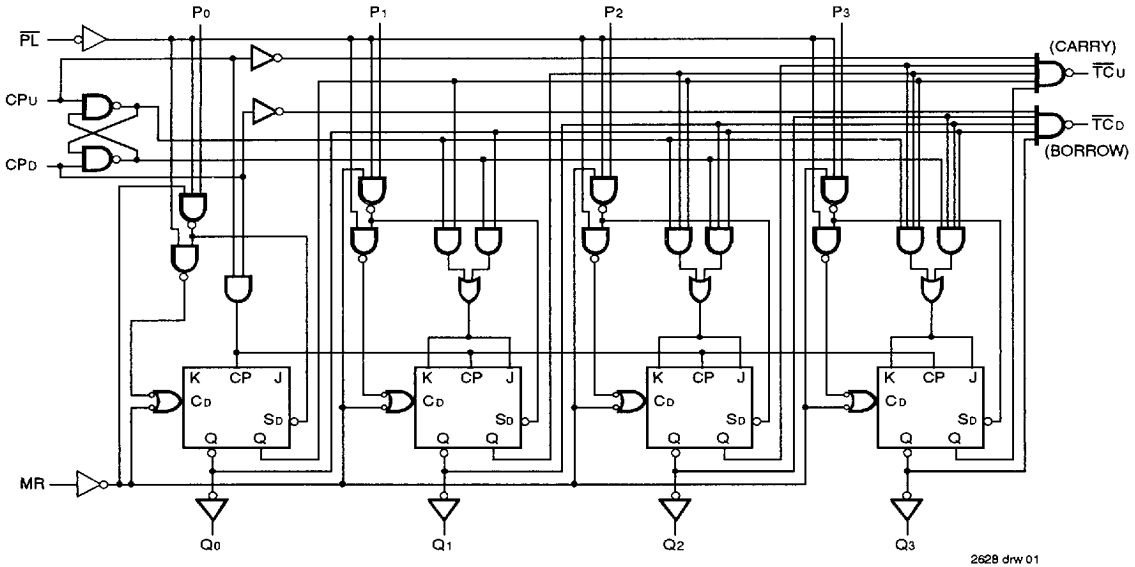
## FEATURES:

- Std. and A speed grades
- Low input and output leakage ≤1μA (max.)
- CMOS power levels
- True TTL input and output compatibility
  - $V_{OH}$ = 3.3V (typ.)
  - $V_{OL}$ = 0.3V (typ.)
- High drive outputs (-15mA $I_{OH}$, 48mA $I_{OL}$)
- Meets or exceeds JEDEC standard 18 specifications
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
- Available in DIP, SOIC, CERPACK and LCC packages

## DESCRIPTION:

The IDT54/74FCT193T and IDT54/74FCT193AT are up/down modulo-16 binary counters built using an advanced dual metal CMOS technology. Separate count-up and count-down clocks are used and, in either counting mode, the circuits operate synchronously. The outputs change state synchronously with the LOW-to-HIGH transitions on the clock inputs. Separate terminal count-up and terminal count-down outputs are provided that are used as the clocks for subsequent stages without extra logic, thus simplifying multistage counter designs. Individual preset inputs allow the circuit to be used as a programmable counter. Both the Parallel Load ($\overline{PL}$) and the Master Reset (MR) inputs asynchronously override the clocks.

## FUNCTIONAL BLOCK DIAGRAM

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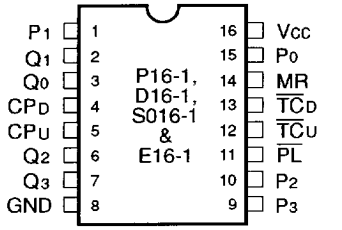
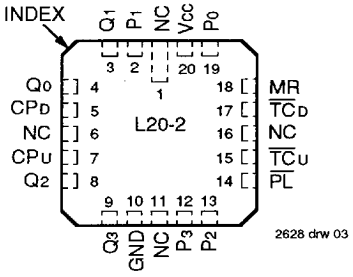
## PIN CONFIGURATIONS




DIP/SOIC/CERPACK
TOP VIEW




LCC
TOP VIEW

## DEFINITION OF FUNCTIONAL TERMS

| Pin Names | Description |
|---|---|
| $CP_U$ | Count Up Clock Input (Active Rising Edge) |
| $CP_D$ | Count Down Clock Input (Active Rising Edge) |
| MR | Asynchronous Master Reset (Active HIGH) |
| $\overline{PL}$ | Asynchronous Parallel Load Input (Active LOW) |
| $P_n$ | Parallel Data Inputs |
| $Q_n$ | Flip-flop Outputs |
| $\overline{TC}_D$ | Terminal Count Down (Borrow) Output (Active LOW) |
| $\overline{TC}_U$ | Terminal Count Up (Carry) Output (Active LOW) |

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## FUNCTION TABLE[1]

| MR | $\overline{PL}$ | $CP_U$ | $CP_D$ | Mode |
|---|---|---|---|---|
| H | X | X | X | Reset (Asyn.) |
| L | L | X | X | Preset (Asyn.) |
| L | H | H | H | No Change |
| L | H | ↑ | H | Count Up |
| L | H | H | ↑ | Count Down |

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**NOTE:**
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   ↑ = LOW-to-HIGH Clock Transition.

## ABSOLUTE MAXIMUM RATINGS[1]

| Symbol | Rating | Commercial | Military | Unit |
|---|---|---|---|---|
| $V_{TERM}$[2] | Terminal Voltage with Respect to GND | –0.5 to +7.0 | –0.5 to +7.0 | V |
| $V_{TERM}$[3] | Terminal Voltage with Respect to GND | –0.5 to $V_{CC}$ +0.5 | –0.5 to $V_{CC}$ +0.5 | V |
| $T_A$ | Operating Temperature | 0 to +70 | –55 to +125 | °C |
| $T_{BIAS}$ | Temperature Under Bias | –55 to +125 | –65 to +135 | °C |
| $T_{STG}$ | Storage Temperature | –55 to +125 | –65 to +150 | °C |
| $P_T$ | Power Dissipation | 0.5 | 0.5 | W |
| $I_{OUT}$ | DC Output Current | –60 to +120 | –60 to +120 | mA |

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**NOTES:**
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed $V_{CC}$ by +0.5V unless otherwise noted.
2. Input and $V_{CC}$ terminals only.
3. Outputs and I/O terminals only.

## CAPACITANCE ($T_A$ = +25°C, f = 1.0MHz)

| Symbol | Parameter[1] | Conditions | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | 6 | 10 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0V | 8 | 12 | pF |

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**NOTE:**
1. This parameter is measured at characterization but not tested.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: $T_A$ = 0°C to +70°C, $V_{CC}$ = 5.0V ± 5%; Military: $T_A$ = −55°C to +125°C, $V_{CC}$ = 5.0V ± 10%

| Symbol | Parameter | Test Conditions[1] | | Min. | Typ.[2] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Level | Guaranteed Logic | COM'L.[5] | 2.0 | — | — | V |
| | | HIGH Level | MIL. | 2.7 | — | — | V |
| $V_{IL}$ | Input LOW Level | Guaranteed Logic LOW Level | | — | — | 0.8 | V |
| $I_{IH}$ | Input HIGH Current[4] | $V_{CC}$ = Max. | $V_I$ = 2.7V | — | — | ±1 | µA |
| $I_{IL}$ | Input LOW Current[4] | | $V_I$ = 0.5V | — | — | ±1 | |
| $I_{OZH}$ | High Impedance Output Current | $V_{CC}$ = Max. | $V_O$ = 2.7V | — | — | ±1 | µA |
| $I_{OZL}$ | (3-State Output pins)[4] | | $V_O$ = 0.5V | — | — | ±1 | |
| $I_I$ | Input HIGH Current[4] | $V_{CC}$ = Max., $V_I$ = $V_{CC}$ (Max.) | | — | — | ±1 | µA |
| $V_{IK}$ | Clamp Diode Voltage | $V_{CC}$ = Min., $I_{IN}$ = −18mA | | — | −0.7 | −1.2 | V |
| $I_{OS}$ | Short Circuit Current | $V_{CC}$ = Max., $V_O$ = GND[3] | | −60 | −120 | −225 | mA |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min. $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = −6mA MIL. $I_{OH}$ = −8mA COM'L. | 2.4 | 3.3 | — | V |
| | | | $I_{OH}$ = −12mA MIL. $I_{OH}$ = −15mA COM'L. | 2.0 | 3.0 | — | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min. $V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 32mA MIL. $I_{OL}$ = 48mA COM'L. | — | 0.3 | 0.5 | V |
| $V_H$ | Input Hysteresis | — | | — | 200 | — | mV |
| $I_{CC}$ | Quiescent Power Supply Current | $V_{CC}$ = Max., $V_{IN}$ = GND or $V_{CC}$ | | — | 0.01 | 1 | mA |

**NOTES:**

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1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC}$ = 5.0V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
4. The test limit for this parameter is ±5µA at $T_A$ = −55°C.
5. Clock pin requires a minimum $V_{IH}$ of 2.5V.

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## POWER SUPPLY CHARACTERISTICS

| Symbol | Parameter | Test Conditions[1] | | Min. | Typ.[2] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $\Delta I_{CC}$ | Quiescent Power Supply Current<br>TTL Inputs HIGH | $V_{CC}$ = Max.<br>$V_{IN}$ = 3.4V[3] | | — | 0.5 | 2.0 | mA |
| $I_{CCD}$ | Dynamic Power Supply Current[4] | $V_{CC}$ = Max., Outputs Open<br>Preset Mode<br>$\overline{PL}$ = $\overline{CE}$ = $\overline{U}$/D = CP = GND<br>One Bit Toggling<br>50% Duty Cycle | $V_{IN}$ = $V_{CC}$<br>$V_{IN}$ = GND | — | 0.15 | 0.25 | mA/<br>MHz |
| $I_C$ | Total Power Supply Current[6] | $V_{CC}$ = Max., Outputs Open<br>Preset Mode<br>$\overline{PL}$ = $\overline{CE}$ = $\overline{U}$/D = CP = GND | $V_{IN}$ = $V_{CC}$<br>$V_{IN}$ = GND | — | 1.5 | 3.5 | mA |
| | | One Bit Toggling<br>at fi = 10MHz<br>50% Duty Cycle | $V_{IN}$ = 3.4V<br>$V_{IN}$ = GND | — | 1.8 | 4.5 | |
| | | $V_{CC}$ = Max., Outputs Open<br>Preset Mode<br>$\overline{PL}$ = $\overline{CE}$ = $\overline{U}$/D = CP = GND | $V_{IN}$ = $V_{CC}$<br>$V_{IN}$ = GND | — | 3.0 | 6.0[5] | |
| | | Four Bits Toggling<br>at fi = 5MHz<br>50% Duty Cycle | $V_{IN}$ = 3.4V<br>$V_{IN}$ = GND | — | 4.0 | 10.0[5] | |

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**NOTES:**

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC}$ = 5.0V, +25°C ambient.
3. Per TTL driven input ($V_{IN}$ = 3.4V). All other inputs at $V_{CC}$ or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the $I_{CC}$ formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   $I_{CC}$ = Quiescent Current
   $\Delta I_{CC}$ = Power Supply Current for a TTL High Input ($V_{IN}$ = 3.4V)
   $D_H$ = Duty Cycle for TTL Inputs High
   $N_T$ = Number of TTL Inputs at $D_H$
   $I_{CCD}$ = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   $f_{CP}$ = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   $f_i$ = Input Frequency
   $N_i$ = Number of Inputs at $f_i$
   All currents are in milliamps and all frequencies are in megahertz.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

| Symbol | Parameter | Condition[1] | FCT193T | | | | FCT193AT | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Com'l. | | Mil. | | Com'l. | | Mil. | | |
| | | | Min.[2] | Max. | Min.[2] | Max. | Min.[2] | Max. | Min.[2] | Max. | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>$CP_U$ or $CP_D$ to $\overline{TC}_U$ or $\overline{TC}_D$ | $C_L$ = 50pF<br>$R_L$ = 500Ω | 2.0 | 10.0 | 2.0 | 10.5 | 2.0 | 6.5 | 2.0 | 6.9 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>$CP_U$ or $CP_D$ to $Q_n$ | | 2.0 | 13.5 | 2.0 | 14.0 | 2.0 | 8.8 | 2.0 | 9.1 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>$P_n$ to $Q_n$ | | 2.0 | 15.5 | 2.0 | 16.5 | 2.0 | 10.1 | 2.0 | 10.8 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>$\overline{PL}$ to $Q_n$ | | 2.0 | 14.0 | 2.0 | 13.5 | 2.0 | 8.8 | 2.0 | 9.1 | ns |
| $t_{PHL}$ | Propagation Delay<br>MR to $Q_n$ | | 3.0 | 15.5 | 3.0 | 16.0 | 3.0 | 10.1 | 3.0 | 10.4 | ns |
| $t_{PLH}$ | Propagation Delay<br>MR to $\overline{TC}_U$ | | 3.0 | 14.5 | 3.0 | 15.0 | 3.0 | 9.4 | 3.0 | 9.8 | ns |
| $t_{PHL}$ | Propagation Delay<br>MR to $\overline{TC}_D$ | | 3.0 | 15.5 | 3.0 | 16.0 | 3.0 | 10.1 | 3.0 | 10.4 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>$\overline{PL}$ to $\overline{TC}_U$ or $\overline{TC}_D$ | | 3.0 | 16.5 | 3.0 | 18.5 | 3.0 | 10.8 | 3.0 | 12.0 | ns |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>$P_n$ to $\overline{TC}_U$ or $\overline{TC}_D$ | | 3.0 | 15.5 | 3.0 | 16.5 | 3.0 | 10.1 | 3.0 | 10.8 | ns |
| $t_{SU}$ | Set-up Time, HIGH or LOW<br>$P_n$ to $\overline{PL}$ | | 5.0 | — | 6.0 | — | 4.0 | — | 5.0 | — | ns |
| $t_H$ | Hold Time, HIGH or LOW<br>$P_n$ to $\overline{PL}$ | | 2.0 | — | 2.0 | — | 1.5 | — | 1.5 | — | ns |
| $t_W$ | $\overline{PL}$ Pulse Width LOW | | 6.0 | — | 7.5 | — | 5.0 | — | 6.5 | — | ns |
| $t_W$ | $CP_U$ or $CP_D$ Pulse Width<br>HIGH or LOW | | 5.0 | — | 7.0 | — | 4.0[3] | — | 6.0 | — | ns |
| $t_W$ | $CP_U$ or $CP_D$ Pulse Width LOW<br>(Change of Direction) | | 10.0 | — | 12.0 | — | 8.0 | — | 10.0 | — | ns |
| $t_W$ | MR Pulse Width HIGH | | 6.0 | — | 6.0 | — | 5.0 | — | 5.0 | — | ns |
| $t_{REM}$ | Recovery Time<br>$\overline{PL}$ to $CP_U$ or $CP_D$ | | 6.0 | — | 8.0 | — | 5.0 | — | 7.0 | — | ns |
| $t_{REM}$ | Recovery Time<br>MR to $CP_U$ or $CP_D$ | | 4.0 | — | 4.5 | — | 3.0 | — | 3.5 | — | ns |

**NOTES:**
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

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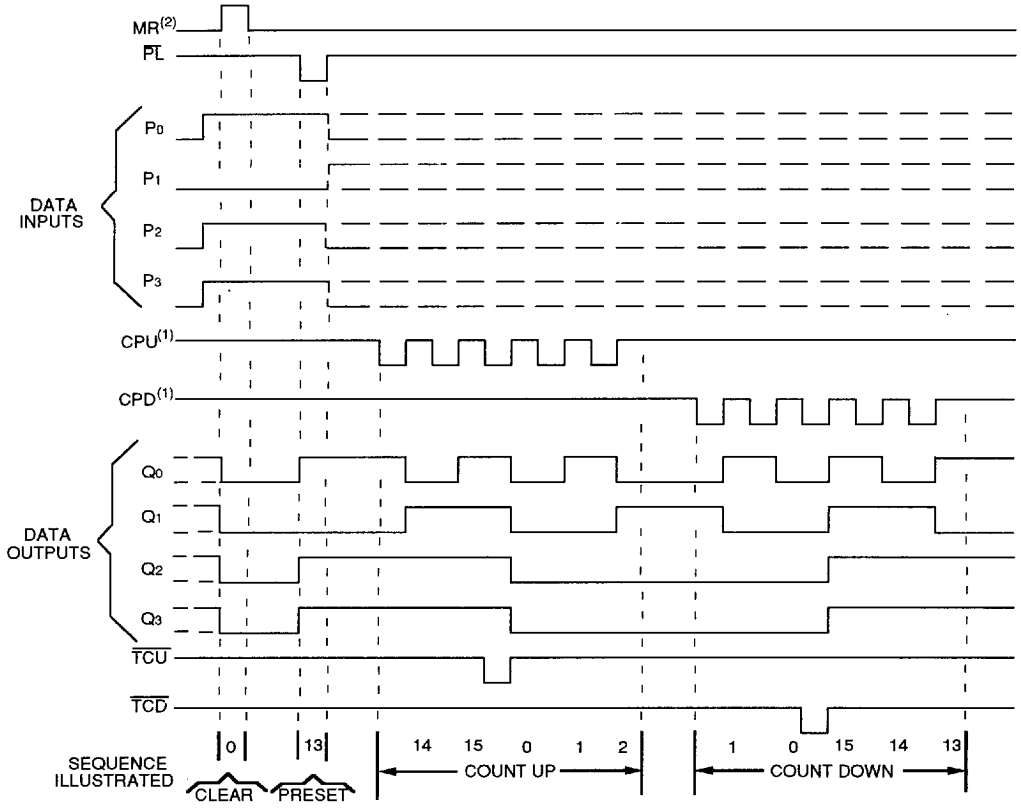
## TIMING WAVEFORMS

**Typical clear, load and count sequences**

Illustrated below is the following sequence:

- Clear outputs to zero.
- Load (preset) to binary thirteen.
- Count up to fourteen, fifteen, carry zero, one and two.
- Count down to one, zero, borrow, fifteen, fourteen and thirteen.



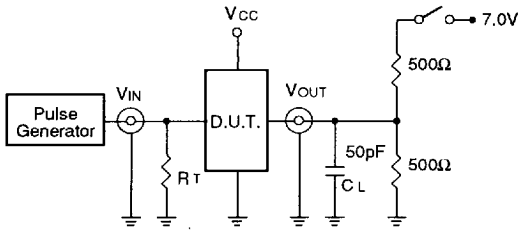

2628 drw 04

**NOTES:**

1. MR overrrides load, data, and count inputs.
2. When counting up, CPD input must be HIGH; when counting down, CPU input must be HIGH.

# TEST CIRCUITS AND WAVEFORMS

## TEST CIRCUITS FOR ALL OUTPUTS




## SWITCH POSITION

| Test | Switch |
|---|---|
| Open Drain<br>Disable Low<br>Enable Low | Closed |
| All Other Tests | Open |

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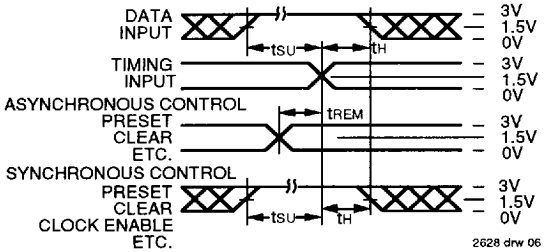
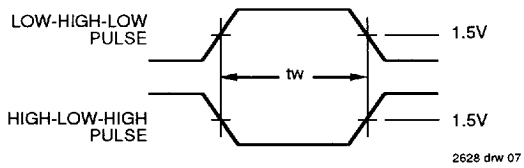
**DEFINITIONS:**

$C_L$ = Load capacitance: includes jig and probe capacitance.
$R_T$ = Termination resistance: should be equal to $Z_{OUT}$ of the Pulse Generator.

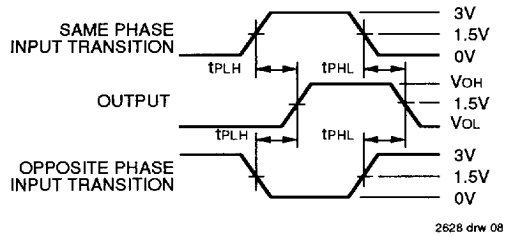
## SET-UP, HOLD AND RELEASE TIMES



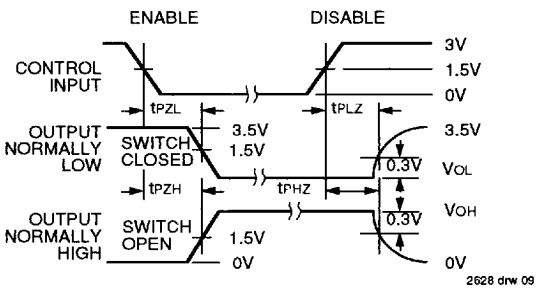

## PULSE WIDTH




## PROPAGATION DELAY




## ENABLE AND DISABLE TIMES




**NOTES:**

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $t_F$ ≤ 2.5ns; $t_R$ ≤ 2.5ns

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## ORDERING INFORMATION