Integrated Device Technology, Inc.

3.3V CMOS OCTAL TRANSCEIVER/ REGISTERS (3-STATE)

IDT54/74FCT3646/A
IDT54/74FCT3648/A
IDT54/74FCT3651/A
IDT54/74FCT3652/A
PRODUCT PREVIEW

FEATURES:

- 0.5 MICRON CMOS Technology
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- 25 mil Center SSOP Packages
- Extended commercial range of –40°C to +85°C
- Vcc = 3.3V ±0.3V, Normal Range or Vcc = 2.7V to 3.6V, Extended Range
- CMOS power levels (10μW typ. static)
- Rail-to-Rail output swing for increased noise margin
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT54/74FCT3646/A, IDT54/74FCT3648/A, IDT54/74FCT3651/A and IDT54/74FCT3652/A consist of a bus transceiver with 3-state D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers.

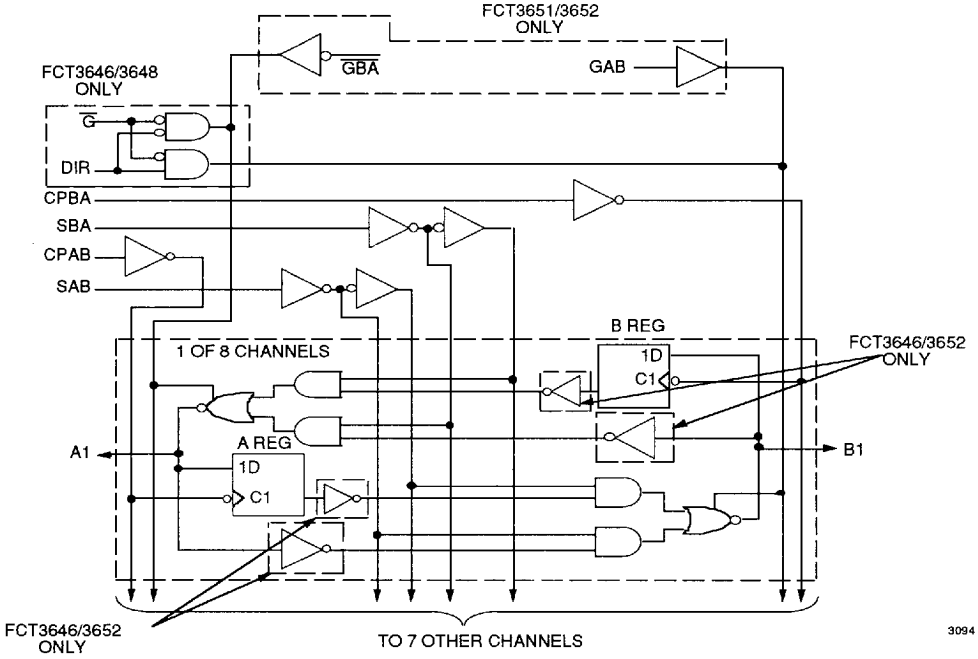
The FCT3651/3652 utilize GAB and $\overline{GBA}$ signals to control the transceiver functions. The FCT3646/3648 utilize the enable control ($\overline{G}$) and direction (DIR) pins to control the transceiver functions.

SAB and SBA control pins are provided to select either real-time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A LOW input level selects real-time data and a HIGH selects stored data.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by LOW-to-HIGH transitions at the appropriate clock pins (CPAB or CPBA), regardless of the select or enable control pins.

The IDT54/74FCT3xxx/A have series current limiting resistors. These offer low ground bounce, minimal undershoot, and controlled output fall times-reducing the need for external series terminating resistors.

FUNCTIONAL BLOCK DIAGRAM



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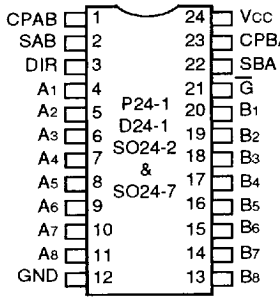
PIN CONFIGURATIONS

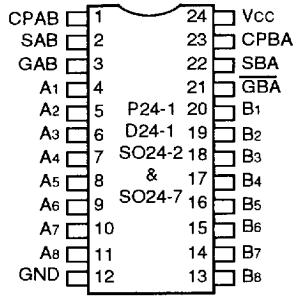
FCT3646/3648



3094 drw 02

DIP/SOIC/SSOP
TOP VIEW

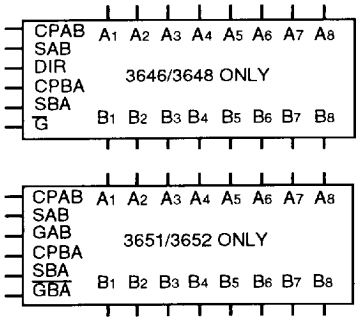
FCT3651/3652



3094 drw 03

DIP/SOIC/SSOP
TOP VIEW

LOGIC SYMBOLS



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PIN DESCRIPTION

Pin Names	Description
A1 - A8	Data Register A Inputs Data Register B Outputs
B1 - B8	Data Register B Inputs Data Register A Outputs
CPAB, CPBA	Clock Pulse Inputs
SAB, SBA	Output Data Source Select Inputs
DIR, $\overline{G}$	Output Enable Inputs (3646/3648)
GAB, $\overline{GBA}$	Output Enable Inputs (3651/3652)

3094 tbl 01

FUNCTION TABLE (3646/3648)

Inputs						Data I/O[1]		Operation or Function	
$\overline{G}$	DIR	CPAB	CPBA	SAB	SBA	A_1 - A_8	B_1 - B_8	FCT3646	FCT3648
H	X	H or L	H or L	X	X	Input	Input	Isolation	Isolation
H	X	↑	↑	X	X			Store A and B Data	Store A and B Data
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus	Real-Time $\overline{B}$ Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus	Stored $\overline{B}$ Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus	Real-Time $\overline{A}$ Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus	Stored $\overline{A}$ Data to B Bus

3094 tbl 02

FUNCTION TABLE (3651/3652)

Inputs						Data I/O		Operation or Function	
GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA	A_1 - A_8	B_1 - B_8	FCT3651	FCT3652
L	H	H or L	H or L	X	X	Input	Input	Isolation	Isolation
L	H	↑	↑	X	X			Store A and B Data	Store A and B Data
X	H	↑	H or L	X	X	Input	Unspecified[1]	Store A, Hold B	Store A, Hold B
H	H	↑	↑	X[2]	X	Input	Output	Store A in Both Registers[3]	Store A in Both Registers
L	X	H or L	↑	X	X	Unspecified[1]	Input	Hold A, Store B	Hold A, Store B
L	L	↑	↑	X	X[2]	Output	Input	Store B in Both Registers[4]	Store B in Both Registers
L	L	X	X	X	L	Output	Input	Real-Time $\overline{B}$ Data to A Bus	Real-Time B Data to A Bus
L	L	X	H or L	X	H			Stored $\overline{B}$ Data to A Bus	Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time $\overline{A}$ Data to B Bus	Real-Time A Data to B Bus
H	H	H or L	X	H	X			Stored $\overline{A}$ Data to B Bus	Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ Data to B Bus and Stored $\overline{B}$ Data to A Bus	Stored A Data to B Bus and Stored B Data to A Bus

3094 tbl 03

NOTES:
1. The data output functions may be enabled or disabled by various signals at the GAB or $\overline{GBA}$ inputs. Data input functions are always enabled, i.e. data at the bus pins will be stored on every LOW-to-HIGH transition on the clock inputs.
2. Select control = L: clocks can occur simultaneously.
   Select control = H: clocks must be staggered in order to load both registers.
   H = HIGH, L = LOW, X = Don't Care, ≠ = LOW-to-HIGH transition.
3. $\overline{A}$ in B Register.
4. $\overline{B}$ in A Register.

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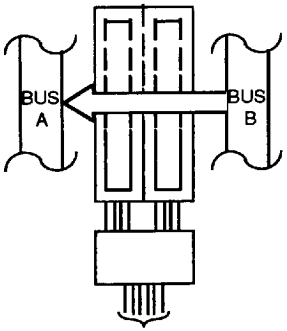
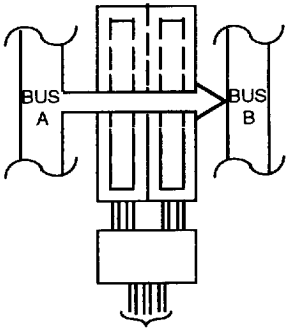


3651/3652	GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
	L	L	X	X	X	L
3646/3648	DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
	L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO A

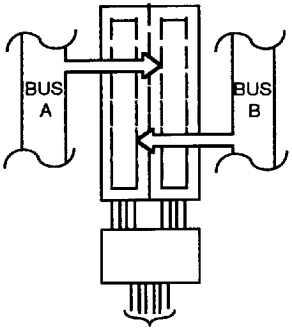
3094 drw 05



3651/3652	GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
	H	H	X	X	L	X
3646/3648	DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
	H	L	X	X	L	X

REAL-TIME TRANSFER
BUS A TO B

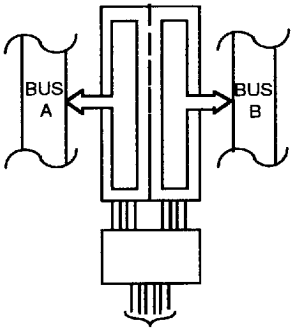
3094 drw 06



3651/3652	GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
	X	H	↑	X	X	X
	L	X	X	↑	X	X
	L	H	↑	↑	X	X
3646/3648	DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
	H	L	↑	X	X	X
	L	L	X	↑	X	X
	X	H	↑	↑	X	X

STORAGE FROM
A AND/OR B

3094 drw 07



3651/3652	GAB	$\overline{GBA}$	CPAB	CPBA	SAB	SBA
	H	L	H or	H or	H	H
3646/3648[1]	DIR	$\overline{G}$	CPAB	CPBA	SAB	SBA
	L	L	X	H or	X	H
	H	L	H or	X	H	X

TRANSFER STORES
DATA TO A AND/OR B

3094 drw 08

NOTE:
1. FCT3646/3648 cannot transfer data to A bus and B bus simultaneously.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +4.6	–0.5 to +4.6	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
V_{TERM}(4)	Terminal Voltage with Respect to GND	–0.5 to V_{CC} + 0.5	–0.5 to V_{CC} + 0.5	V
T_A	Operating Temperature	–40 to +85	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	–60 to +60	–60 to +60	mA

3094 lnk 04

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Vcc terminals.
3. Input terminals.
4. Output and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	3.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	4.0	8.0	pF

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NOTE:
1. This parameter is measured at characterization but not tested.

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DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: T_A = –40°C to +85°C, V_{CC} = 2.7V to 3.6V; Military: T_A = –55°C to +125°C, V_{CC} = 2.7V to 3.6V

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2.0	—	5.5	V
	Input HIGH Level (I/O pins)			2.0	—	V_{CC}+0.5	
V_{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		–0.5	—	0.8	V
I_{IH}	Input HIGH Current (Input pins)[6]	V_{CC} = Max.	V_I = 5.5V	—	—	±1	µA
	Input HIGH Current (I/O pins)[6]		V_I = V_{CC}	—	—	±1	
I_{IL}	Input LOW Current (Input pins)[6]		V_I = GND	—	—	±1	
	Input LOW Current (I/O pins)[6]		V_I = GND	—	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = V_{CC}	—	—	±1	µA
I_{OZL}	(3-State Output pins)[6]		V_O = GND	—	—	±1	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	V
I_{ODH}	Output HIGH Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		–36	–60	–110	mA
I_{ODL}	Output LOW Current	V_{CC} = 3.3V, V_{IN} = V_{IH} or V_{IL}, V_O = 1.5V[3]		50	90	200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min.	I_{OH} = –0.1mA	V_{CC}–0.2	—	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –3mA	2.4	3.0	—	
		V_{CC} = 3.0V V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4[5]	3.0	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min.	I_{OL} = 0.1mA	—	—	0.2	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA	—	0.2	0.4	
			I_{OL} = 24mA	—	0.3	0.5	
I_{OS}	Short Circuit Current[4]	V_{CC} = Max., V_O = GND[3]		–60	–135	–240	mA
V_H	Input Hysteresis	—		—	150	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}	COM'L.	—	0.1	10	µA
			MIL.	—	0.1	100	

3094 lnk 06

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. V_{OH} = V_{CC} –0.6V at rated current.
6. The test limits for this parameter is ± 5µA at T_A = –55°C.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current	V_{CC} = Max.	V_{IN} = V_{CC} −0.6V[3]				µA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Open GAB = $\overline{GBA}$ = GND or $\overline{G}$ = DIR = GND One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND				µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle GAB = $\overline{GBA}$ = GND or	V_{IN} = V_{CC} V_{IN} = GND				mA
		$\overline{G}$ = DIR = GND One Bit Toggling at fi = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} −0.6V V_{IN} = GND				
		V_{CC} = Max. Outputs Open f_{CP} = 10MHz 50% Duty Cycle GAB = $\overline{GBA}$ = GND or	V_{IN} = V_{CC} V_{IN} = GND				
		$\overline{G}$ = DIR = GND Eight Bits Toggling at fi = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} −0.6V V_{IN} = GND				

3094 tbl 07

NOTES:

1. For conditions shown as max. or min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Per TTL driven input; all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   N_{CP} = Number of Clock Inputs at f_{CP}
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

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SWITCHING CHARACTERISTICS OVER OPERATING RANGE[3]

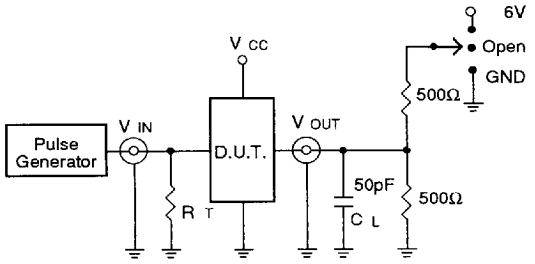
Symbol	Parameter	Condition[1]	FCT3646/3648/3651/3652				FCT3646A/3648A/3651A/3652A				Unit
			Com'l.		Mil.		Com'l.		Mil.		
			Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay Bus to Bus	C_L = 50pF R_L = 500Ω	2.0	9.0	2.0	11.0	2.0	6.3	2.0	7.7	ns
t_{PZH} t_{PZL}	Output Enable Time, $\overline{G}$, DIR to Bus (646, 648 only)		2.0	14.0	2.0	15.0	2.0	9.8	2.0	10.5	ns
t_{PZH} t_{PZL}	Output Enable Time, GAB, $\overline{GBA}$ to Bus (651, 652 only)		2.0	14.0	2.0	15.0	2.0	9.8	2.0	10.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time, $\overline{G}$, DIR to Bus (646, 648 only)		2.0	9.0	2.0	11.0	2.0	6.3	2.0	7.7	ns
t_{PHZ} t_{PLZ}	Output Disable Time, GAB, $\overline{GBA}$ to Bus (651, 652 only)		2.0	9.0	2.0	11.0	2.0	6.3	2.0	7.7	ns
t_{PLH} t_{PHL}	Propagation Delay Clock to Bus		2.0	9.0	2.0	10.0	2.0	6.3	2.0	7.0	ns
t_{PLH} t_{PHL}	Propagation Delay SBA or SAB to Bus		2.0	11.0	2.0	12.0	2.0	7.7	2.0	8.4	ns
t_{SU}	Set-up Time HIGH or LOW Bus to Clock		4.0	—	4.5	—	2.0	—	2.0	—	ns
t_H	Hold Time HIGH or LOW Bus to Clock		2.0	—	2.0	—	1.5	—	1.5	—	ns
t_W	Clock Pulse Width, HIGH or LOW		6.0	—	6.0	—	5.0	—	5.0	—	ns

3094 tbl 08

NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, Normal Range. For V_{CC} = 2.7V to 3.6V, Extended Range, all Propagation Delays and Enable/Disable times should be degraded by 20%.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



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SWITCH POSITION

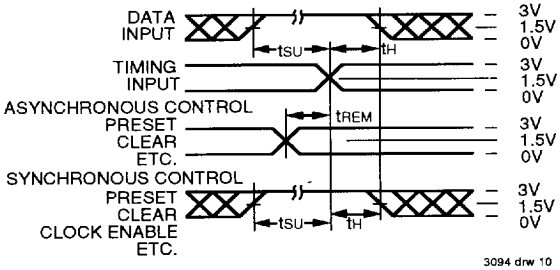
Test	Switch
Open Drain Disable Low Enable Low	6V
Disable High Enable High	GND
All Other tests	Open

3094 lnk 09

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



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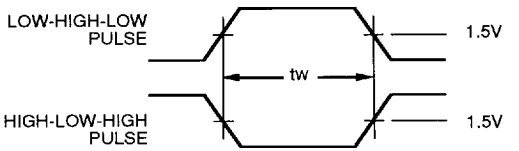
PULSE WIDTH



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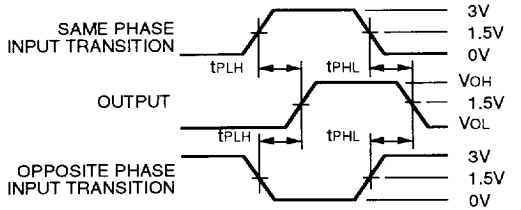
PROPAGATION DELAY



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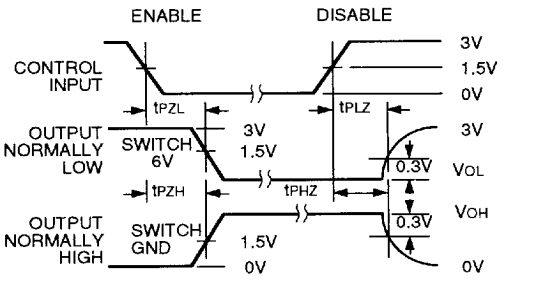
ENABLE AND DISABLE TIMES



3094 drw 13

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
3. If V_{CC} is below 3V, input voltage swings should be adjusted not to exceed V_{CC}.

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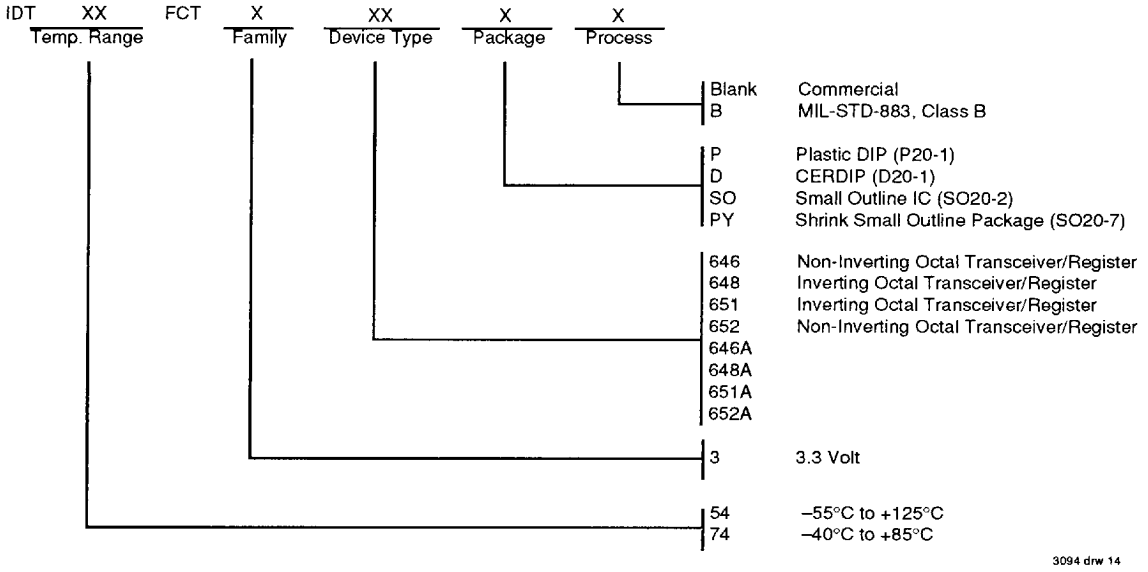
ORDERING INFORMATION



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