T-46-23-10

NOTICE
SEE ORDER OF DATA FOR ERRATA INFORMATION

Integrated Device Technology, Inc.

CMOS STATIC RAM 256K (64K x 4-BIT)

ADVANCED INFORMATION
IDT61298

FEATURES:

- Fast Output Enable ($\overline{OE}$) pin available for added system flexibility
- High speed (equal access and cycle times)
  - — Military: 25/35/45/55 (max.)
  - — Commercial: 20/25/35/45ns (max.)
- Low power consumption
  - — IDT61298S
    Active: 400mW (typ.)
    Standby: 400µw (typ.)
  - — IDT61298L
    Active: 350mW (typ.)
    Standby: 100µw (typ.)
- Battery back-up operation
  - — 2V data retention (L version only)
- JEDEC standard pinout
- 300 Mil 28-pin DIP, 300 Mil28-pin SOJ, and 300 Mil 28-pin LCC
- Produced with advanced CEMOS™ technology
- Bidirectional data inputs and outputs
- Inputs/Outputs TTL-compatible
- Three-state outputs
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT61298 is a 262,144-bit high-speed static RAM organized as 64K x 4. It is fabricated using IDT's high-performance, high-reliability technology – CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective approach for memory intensive applications.

The IDT61298 features two memory control functions: Chip Select ($\overline{CS}$) and Output Enable ($\overline{OE}$). These two functions greatly enhance the IDT61298's overall flexibility in high-speed memory applications.

Access times as fast as 20ns are available with typical power consumption of only 350mW. The IDT61298 offers a reduced power standby mode, I_{SB1}, which enables the designer to considerably reduce device power requirements. This capability significantly decreases system power and cooling levels, while greatly enhancing system reliability. The low-power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 100µW when operating from a 2V battery.

All inputs and outputs are TTL-compatible and the device operates from a single 5 volt supply. Fully static asynchronous

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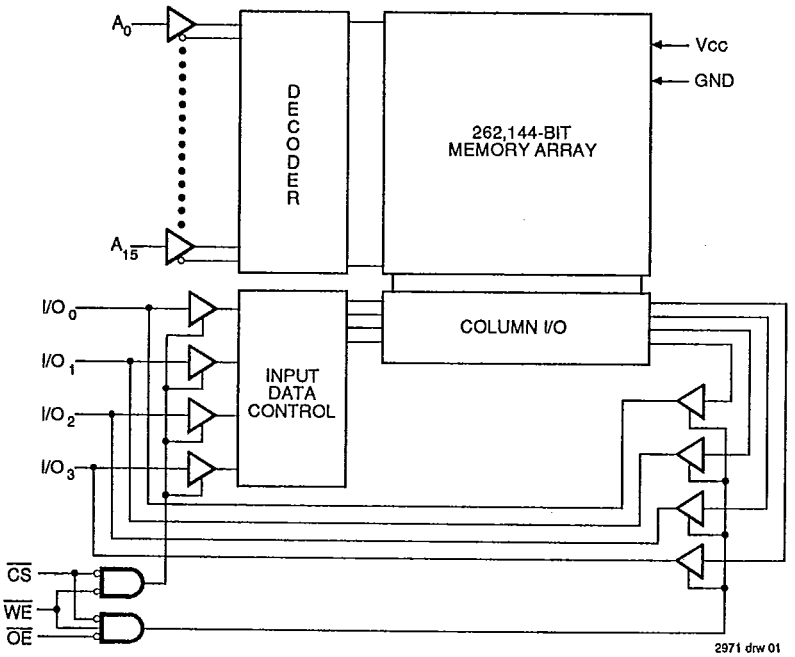
FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

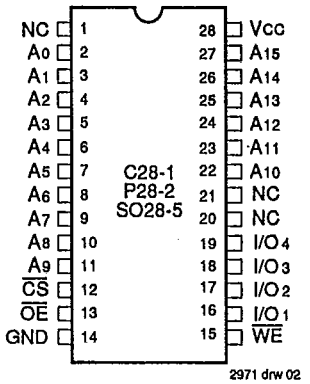
DESCRIPTION (Continued)

circuitry, along with matching access and cycle times, favor the simplified system design approach.

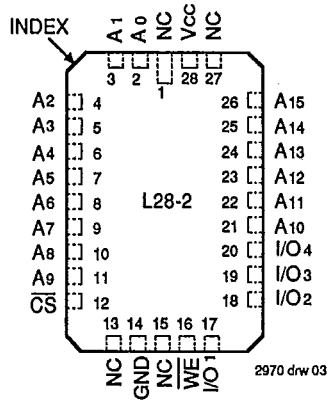
The IDT61298 is packaged in a 28-pin sidebraze or plastic 300mil DIP, an SOJ, plus an LCC, providing improved board-level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

PIN CONFIGURATION



DIP/SOJ
TOP VIEW



LCC
TOP VIEW

PIN DESCRIPTIONS

Name	Description
A_0–A_{15}	Address Inputs
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
I/O_{1-4}	Data Input/Output
V_{CC}	Power
GND	Ground

2971 tbl 01

TRUTH TABLE[1]

Mode	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O	Power
Standby	H	X	X	High Z	Standby
Read	L	H	L	D_{OUT}	Active
Write	L	L	X	D_{IN}	Active
Read	L	H	H	High Z	Active

NOTE: 2971 tbl 02
1. H = V_{IH}, L = V_{IL}, X = Don't Care

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2971 tbl 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	11	pF

NOTE: 2975 tbl 04
1. This parameter is determined by device characterization, but is not production tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2971 tbl 05

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE:
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

2971 tbl 06

DC ELECTRICAL CHARACTERISTICS[1]

(Vcc = 5V ± 10%, V_{LC} = 0.2V, V_{HC} = Vcc - 0.2V)

Symbol	Parameter	Power	61298S20 61298L20		61298S25 61298L25		61298S35 61298L35		61298S45 61298L45		61298S55 61298L55		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open Vcc = Max., f = 0[2]	S	110	—	100	110	100	110	100	110	—	110	mA
		L	100	—	90	100	90	100	90	100	—	100	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open Vcc = Max., f = f_{MAX}[2]	S	160	—	150	160	150	160	150	160	—	160	mA
		L	140	—	130	140	130	140	130	140	—	140	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, Vcc = Max., Outputs Open, f = f_{MAX}[2]	S	35	—	35	35	35	35	35	35	—	35	mA
		L	20	—	20	20	20	20	20	20	—	20	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, Vcc = Max., f = 0[2]	S	30	—	30	35	30	35	30	35	—	35	mA
		L	1.5	—	1.5	4.5	1.5	4.5	1.5	4.5	—	4.5	

NOTES:
1. All values are maximum guaranteed values.
2. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of 1/t_{RC}. f = 0 means no input lines change.

2971 tbl 07

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AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2971 tbl 08

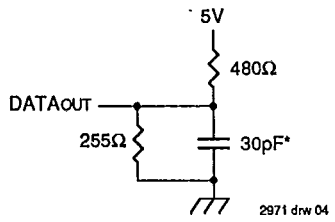


Figure 1. Output Load

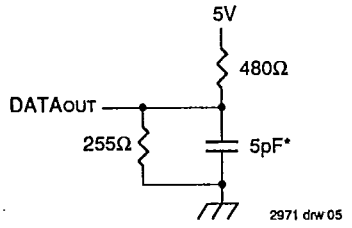


Figure 2. Output Load
(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, t_{WHZ})

*Includes scope and jig capacitances

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition		IDT61298S Min.	IDT61298S Typ.	IDT61298S Max.	IDT61298L Min.	IDT61298L Typ.	IDT61298L Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL COM'L	— —	— —	10 5	— —	— —	5 2	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL COM'L	— —	— —	10 5	— —	— —	5 2	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min. I_{OL} = 10mA, V_{CC} = Min.		— —	— —	0.4 0.5	— —	— —	0.4 0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	—	—	2.4	—	—	V

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

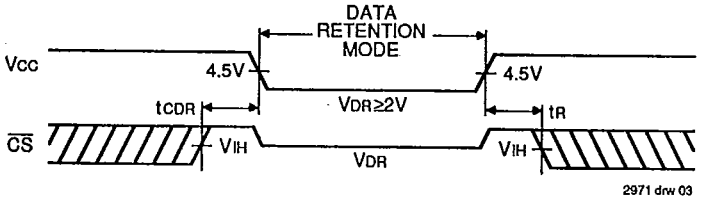
(L Version Only) V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Condition		Min.	Typ.(1) Vcc @ 2.0v	Typ.(1) Vcc @ 3.0V	Max. Vcc @ 2.0V	Max. Vcc @ 3.0V	Unit
V_{DR}	Vcc for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current		MIL. COM'L.	— —	50 50	75 75	2000 500	3000 750	µA
t_{CDR}(3)	Chip Deselect to Data Retention Time	$\overline{CS}$ ≥ V_{HC}		0	—	—	—	—	ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	—	—	—	—	ns
$\|I_{LI}\|$(3)	Input Leakage Current			—	—	—	2	2	µA

2971 tbl 10

NOTES:
1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed, but not tested.

LOW Vcc DATA RETENTION WAVEFORM



2971 drw 03

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	61298S20(1) 61298L20(1) Min.	61298S20(1) 61298L20(1) Max.	61298S25(2) 61298L25(2) Min.	61298S25(2) 61298L25(2) Max.	61298S35 61298L35 Min.	61298S35 61298L35 Max.	61298S45 61298L45 Min.	61298S45 61298L45 Max.	61298S55(2) 61298L55(2) Min.	61298S55(2) 61298L55(2) Max.	Unit
Read Cycle												
tRC	Read Cycle Time	20	—	25	—	35	—	45	—	55	—	ns
tAA	Address Access Time	—	20	—	25	—	35	—	45	—	55	ns
tACS	Chip Select Access Time	—	20	—	25	—	35	—	45	—	55	ns
tCLZ(3)	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
tOE	Output Enable to Output Valid	—	13	—	15	—	25	—	30	—	35	ns
tOLZ(3)	Output Enable to Output in Low Z	2	—	3	—	5	—	5	—	5	—	ns
tCHZ(3)	Chip Select to Output in High Z	—	10	—	13	—	15	—	20	—	25	ns
tOHZ(3)	Output Disable to Output in High Z	—	10	—	13	—	15	—	15	—	20	ns
tOH	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns
tPU(3)	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	0	—	ns
tPD(3)	Chip Deselect to Power Down Time	—	20	—	25	—	35	—	45	—	55	ns
Write Cycle												
tWC	Write Cycle Time	20	—	20	—	30	—	40	—	50	—	ns
tCW	Chip Select to End of Write	15	—	20	—	30	—	40	—	50	—	ns
tAW	Address Valid to End of Write	15	—	20	—	30	—	40	—	50	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	15	—	20	—	30	—	40	—	50	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tWHZ(3)	Write Enable to Output in High Z	—	10	—	11	—	15	—	20	—	25	ns
tDW	Data Valid to End of Write	11	—	15	—	20	—	25	—	30	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
tOW(3)	Output Active from End of Write	5	—	5	—	5	—	5	—	5	—	ns

NOTES:
1. 0° to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.
4. Preliminary data for militatry devices only.

2971 tbl 11

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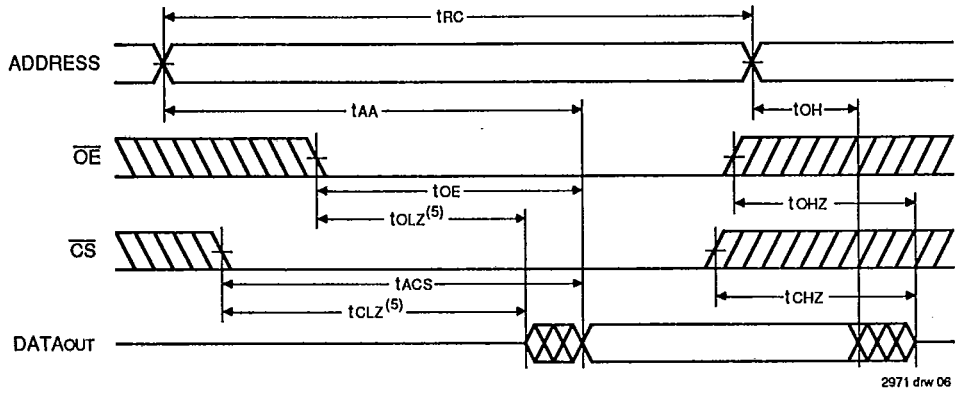
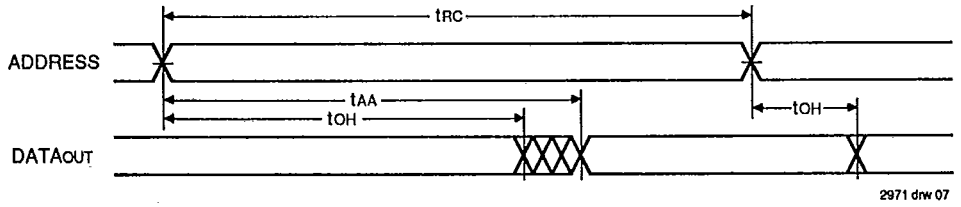
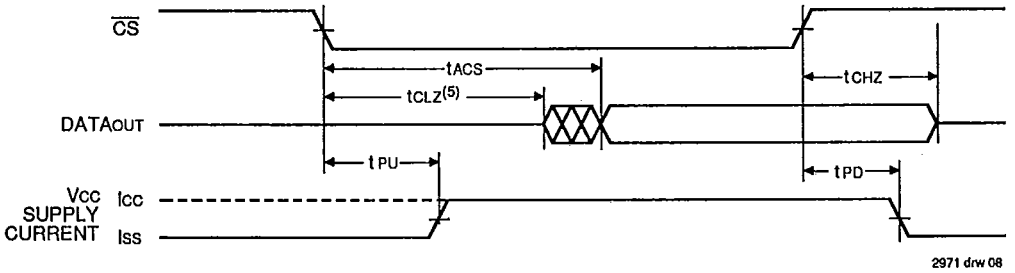
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



TIMING WAVEFORM OF READ CYCLE NO. 2(1,2,4)

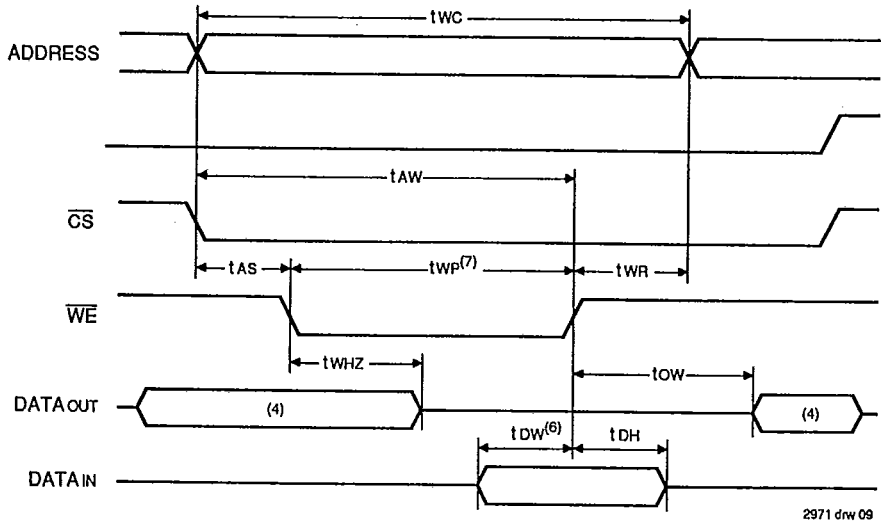


TIMING WAVEFORM OF READ CYCLE NO. 3(1,3,4)

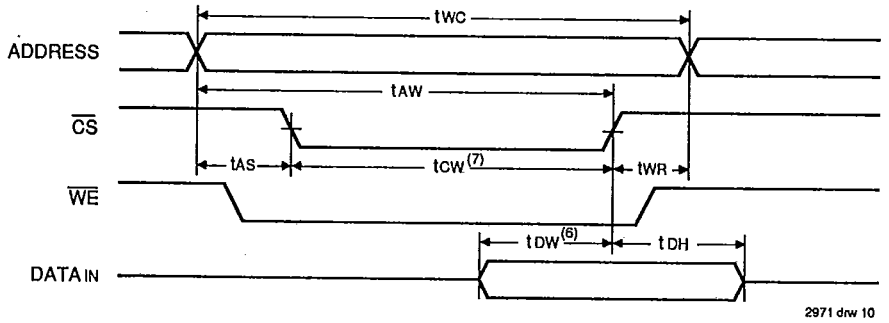


NOTES:
1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CS}$ = VIL.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = VIL.
5. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1,2,3,7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1,2,3,5)



NOTES:
1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (tCW or tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig).
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

ORDERING INFORMATION