Integrated Device Technology, Inc.

CMOS STATIC RAM 16K (16K x 1-BIT)

IDT6167SA
IDT6167LA

FEATURES:

- High-speed (equal access and cycle time)
  - — Military: 15/20/25/35/45/55/70/85/100ns (max.)
  - — Commercial: 12/15/20/25/35ns (max.)
- Low power consumption
  - — IDT6167SA
    Active: 200mW (typ.)
    Standby: 100µW (typ.)
  - — IDT6167LA
    Active: 150mW (typ.)
    Standby: 10µW (typ.)
- Battery backup operation — 2V data retention voltage (IDT6167LA only)
- Available in 20-pin CERDIP and plastic DIP, 20-pin CERPACK, 20-pin SOIC and 20-pin leadless chip carrier
- Produced with advanced CEMOS™ high-performance technology
- CEMOS process virtually eliminates alpha particle soft-error rates
- Separate data input and output
- Single 5V (+10%) power supply
- Input and output directly TTL-compatible
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-84132 is listed on this function. Refer to Section 2/page 2-4

DESCRIPTION:

The IDT6167 is a 16,384-bit high-speed static RAM organized as 16K x 1. The part is fabricated using IDT's high-performance, high reliability technology — CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective alternative to bipolar and fast NMOS memories.

Access times as fast as 12ns are available with maximum power consumption of only 660mW. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, a standby mode as long as $\overline{CS}$ remains high. In the standby mode, the device consumes less than 10µW, typically. This capability provides significant system-level power and cooling savings. The low-power (LA) version also offers a battery backup data retention capability where the circuit typically consumes only 1µW operating off a 2V battery.

All inputs and the output of the IDT6167 are TTL-compatible and operate from a single 5V supply, thus simplifying system designs.

The IDT6167 is packaged in a space-saving 20-pin, 300 mil Plastic DIP or CERDIP, plastic 20-pin SOIC or SOJ, 20-pin CERPACK and 20-pin leadless chip carrier, providing high board-level packing densities.

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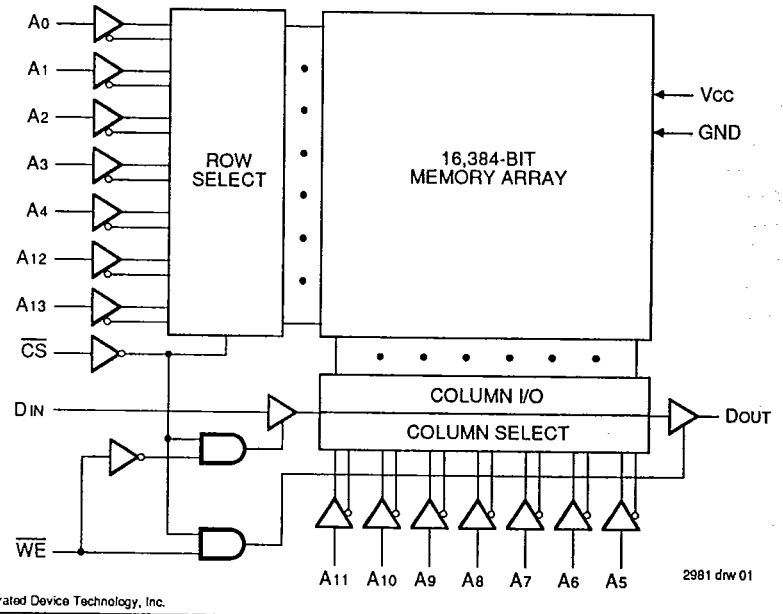
FUNCTIONAL BLOCK DIAGRAM



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DESCRIPTION (Continued)

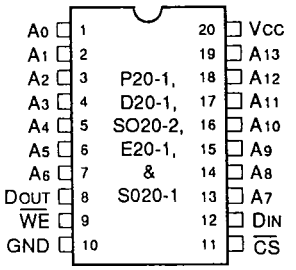
Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

TRUTH TABLE (1)

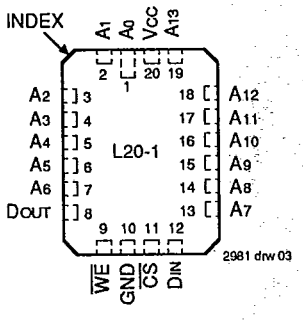
Mode	$\overline{CS}$	$\overline{WE}$	Output	Power
Standby	H	X	High Z	Standby
Read	L	H	DATAOUT	Active
Write	L	L	High Z	Active

NOTE: 2981 tbl 02
1. H = VIH, L = VIL, X = Don't Care.

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



LCC
TOP VIEW

PIN NAMES

A0–A13	Address Inputs
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
VCC	Power
DIN	DATAIN
DOUT	DATAOUT
GND	Ground

2981 tbl 01

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	-0.5(1)	—	0.8	V

NOTE: 2981 tbl 05
1. VIL (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	VCC
Military	-55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2981 tbl 06

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
PT	Power Dissipation	1.0	1.0	W
IOUT	DC Output Current	50	50	mA

NOTE: 2981 tbl 03
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	7	pF
COUT	Output Capacitance	VOUT = 0V	7	pF

NOTE: 2981 tbl 04
1. This parameter is determined by device characterization, but is not production tested.

DC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	6167SA12		6167SA/LA15		6167SA/LA25		6167SA/LA35		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = 0[3]	SA	90	—	90	90	90	90	90	90	mA
		LA	—	—	55	60	55	60	55	60	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}[3]	SA	140	—	120	130	100	110/100	100	100	mA
		LA	—	—	100	110	80/70	85/75	65	70	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, Outputs Open, V_{CC} = Max., f = f_{MAX}[3]	SA	50	—	50	50	35	35	35	35	mA
		LA	—	—	35	35	30/25	30/25	20	20	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max. V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC}, f = 0[3]	SA	10	—	5	10	5	10	5	10	mA
		LA	—	—	0.9	2	0.05	2/0.9	0.05	0.9	

DC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	6167SA/LA45		6167SA/LA55		6167SA/LA70		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = 0[3]	SA	—	90	—	90	—	90	mA
		LA	—	60	—	60	—	60	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}[3]	SA	—	100	—	100	—	100	mA
		LA	—	65	—	60	—	60	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, Outputs Open, V_{CC} = Max., f = f_{MAX}[3]	SA	—	35	—	35	—	35	mA
		LA	—	20	—	20	—	15	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max. V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC}, f = 0[3]	SA	—	10	—	10	—	10	mA
		LA	—	0.9	—	0.9	—	0.9	

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NOTES:
1. All values are maximum guaranteed values.
2. Also available: 85ns and 100ns Military devices.
3. f = f_{MAX} (All Inputs cycling at f = 1/t_{RC}). f = 0 means no address control lines change.

2980 tbl 07

DC ELECTRICAL CHARACTERISTICS

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V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition		IDT6167SA Min.	IDT6167SA Max.	IDT6167LA Min.	IDT6167LA Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max.,	MIL	—	10	—	5	µA
		V_{IN} = GND to V_{CC}	COM'L	—	5	—	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH},	MIL	—	10	—	5	µA
		V_{OUT} = GND to V_{CC}	COM'L	—	5	—	2	
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.		—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OL} = -4mA, V_{CC} = Min.		2.4	—	2.4	—	V

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

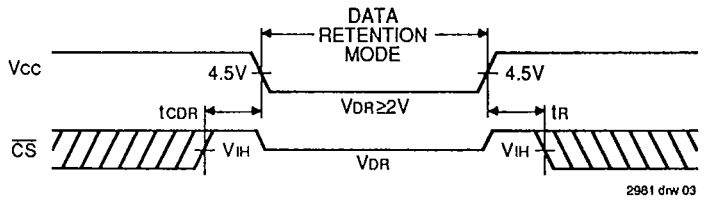
(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Condition		Min.	Typ.[1] Vcc @ 2.0v	Typ.[1] Vcc @ 3.0V	Max. Vcc @ 2.0V	Max. Vcc @ 3.0V	Unit
V_{DR}	Vcc for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current		MIL.	—	0.5	1.0	200	300	µA
			COM'L.	—	0.5	1.0	20	30	
t_{CDR}	Chip Deselect to Data Retention Time	$\overline{CS}$ ≥ V_{HC} VIN ≥ V_{HC} or ≤ V_{LC}		0	—	—	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	—	—	ns
$\|I_{LI}\|$[3]	Input Leakage Current			—	—	—	2	2	µA

2981 tbl 09

NOTES:
1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed, but not tested.

LOW Vcc DATA RETENTION WAVEFORM



2981 drw 03

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AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2979 tbl 09

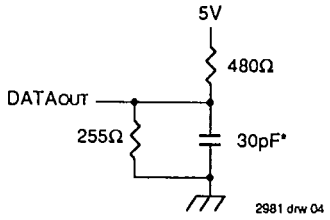

Figure 1. Output Load

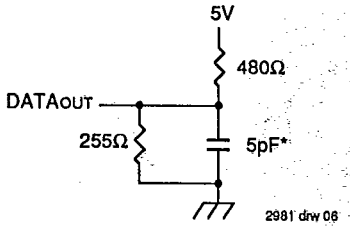

Figure 2. Output Load
(for tHZ, tLZ, twz and tow)

*Includes scope and jig.

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	6167SA12[1] Min.	6167SA12[1] Max.	6167SA15 6167LA15 Min.	6167SA15 6167LA15 Max.	6167SA20/25 6167LA20/25 Min.	6167SA20/25 6167LA20/25 Max.	6167SA35/45[2] 6167LA35/45[2] Min.	6167SA35/45[2] 6167LA35/45[2] Max.	6167SA55[2]/70[2] 6167LA55[2]/70[2] Min.	6167SA55[2]/70[2] 6167LA55[2]/70[2] Max.	Unit
Read Cycle												
tRC	Read Cycle Time	12	—	15	—	20/25	—	35/45	—	55/70	—	ns
tAA	Address Access Time	—	12	—	15	—	20/25	—	35/45	—	55/70	ns
tACS	Chip Select Access Time	—	12	—	15	—	20/25	—	35/45	—	55/70	ns
tOH	Output Hold from Address Change	3	—	3	—	5/5	—	5/5	—	5/5	—	ns
tLZ	Chip Deselct to Output in Low Z[3]	3	—	3	—	5/5	—	5/5	—	5/5	—	ns
tHZ	Chip Select to Output in High Z[3]	—	8	—	10	—	10/10	—	15/30	—	40/40	ns
tPU	Chip Select to Power Up Time[3]	0	—	0	—	0/0	—	0/0	—	0/0	—	ns
tPD	Chip Deselect to Power Down Time[3]	—	12	—	15	—	20/25	—	35/45	—	55/70	ns
Write Cycle												
tWC	Write Cycle Time	12	—	15	—	20/20	—	30/45	—	55/70	—	ns
tCW	Chip Select to End of Write	12	—	15	—	15/20	—	30/40	—	45/55	—	ns
tAW	Address Valid to End of Write	12	—	15	—	15/20	—	30/40	—	45/55	—	ns
tAS	Address Set-up Time	0	—	0	—	0/0	—	0/0	—	0/0	—	ns
tWP	Write Pulse Width	12	—	13	—	15/20	—	30/30	—	35/40	—	ns
tWR	Write Recovery Time	0	—	0	—	0/0	—	0/0	—	0/0	—	ns
tDW	Data Valid to End of Write	10	—	10	—	12/15	—	17/20	—	25/30	—	ns
tDH	Data Hold Time	0	—	0	—	0/0	—	0/0	—	0/0	—	ns
tWZ	Write Enable to Output in High Z[3]	—	6	—	7	—	8/8	—	15/30	—	40/40	ns
tOW	Output Active from End of Write[3]	0	—	0	—	0/0	—	0/0	—	0/0	—	ns

NOTES:
1. 0° to +70°C temperature range only.
2. -55°C to +125°C temperature range only. Also available: 85ns and 100ns Military devices.
3. This parameter is guaranteed, but not tested.

2981 tbl 11

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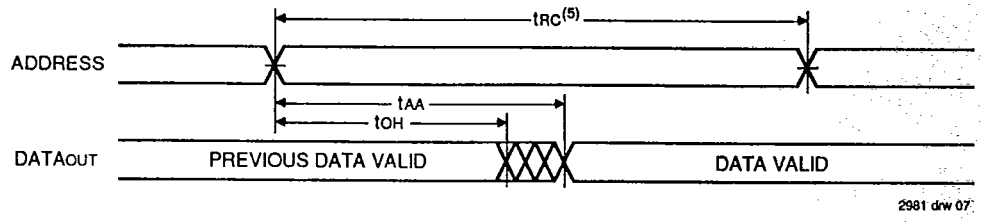
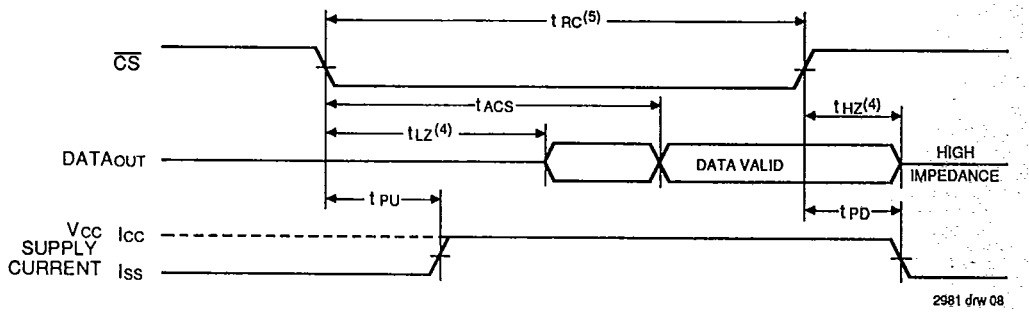
TIMING WAVEFORM OF READ CYCLE NO. 1(1, 2)



TIMING WAVEFORM OF READ CYCLE NO. 2(1, 3)



NOTES:
1. $\overline{WE}$ is High for READ cycle.
2. $\overline{CS}$ is low for READ cycle.
3. Address valid prior to or coincedent with $\overline{CS}$ transition low.
4. Transition is measured ±200mV from steady state with specified loadingiin Figure 2.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.

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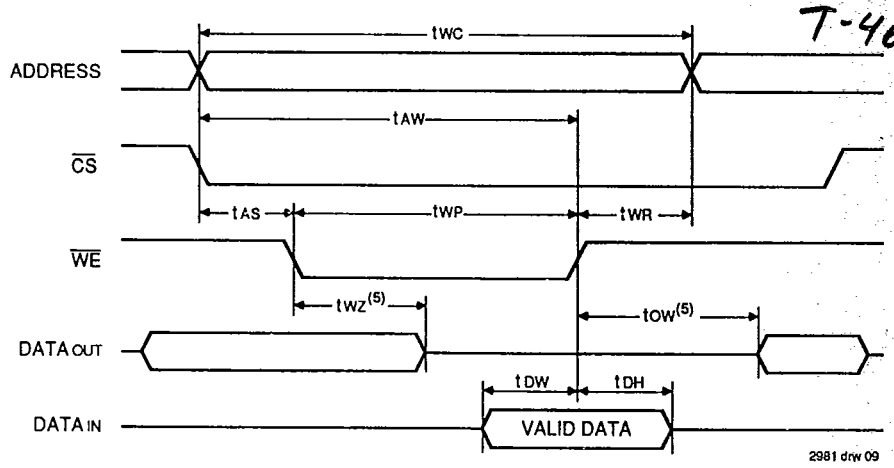
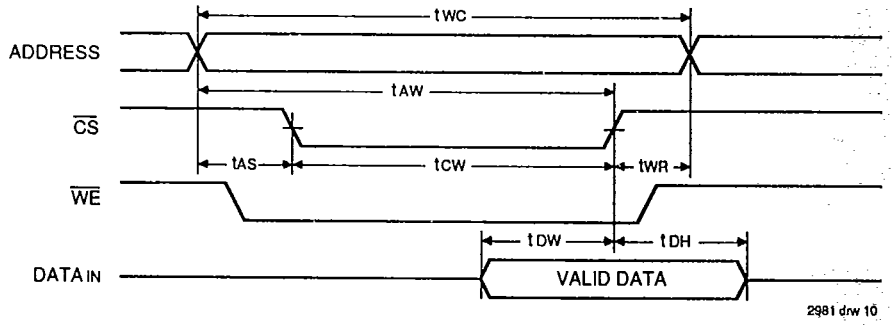
TIMING WAVEFORM OF WRITE CYCLE NO. 1, ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3)



TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3)



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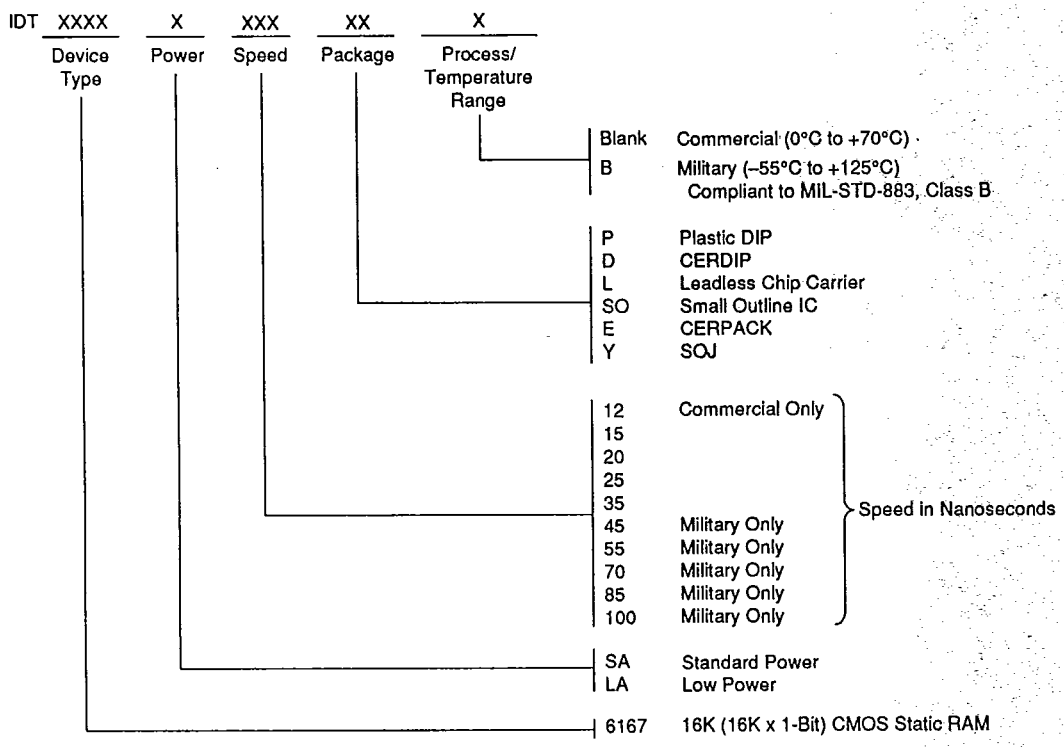
NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be inactive during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the wnd of the write cycle.
4. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
5. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig).

ORDERING INFORMATION



2981 drw 11