Integrated Device Technology, Inc.

CMOS STATIC RAM WITH OUTPUT ENABLE 16K (4K x 4-BIT)

IDT61970S
IDT61970L

FEATURES:

- High Speed (equal Access and Cycle Times)
  - Military: 12/15/20/25/35/45/55
  - Commercial: 10/12/15/20/25/35/45
- Fast Output Enable
- Low power consumption
- Battery backup operation—2V data retention (IDT61970L only)
- Available in 22-pin ceramic or plastic DIP and 24-pin SOJ
- Produced with advanced CMOS high-performance technology
- Separate Output Enable control
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT61970 is a 16,384-bit high-speed static RAM organized as 4096 x 4 bits. It is fabricated using IDT's high-performance, high-reliability CMOS technology.

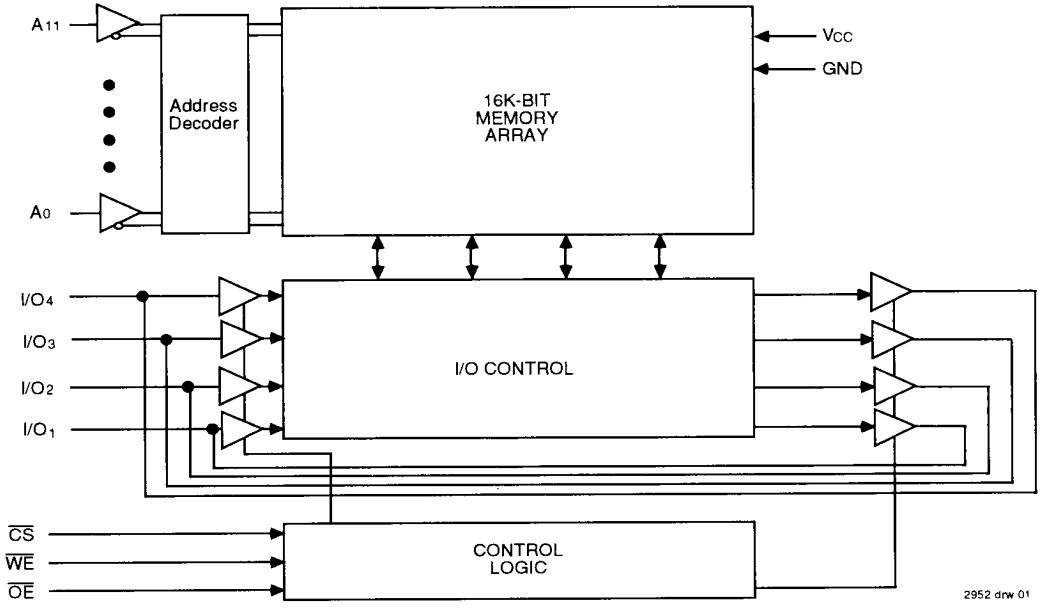
The IDT61970 features two memory control functions: Chip Select ($\overline{CS}$) and Output Enable ($\overline{OE}$). These two functions greatly enhance the IDT61970s overall flexibility in high-speed memory applications. This feature makes the IDT61970 ideal for use in cache memory applications.

Access times as fast as 10ns and t_{OE} as fast as 5ns are available. The IDT61970 offers a reduced power standby mode which enables the designer to considerably reduce device power requirements. This capability significantly decreases system power and cooling levels, while greatly enhancing system reliability. The low power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 10μW when operating from a 2V battery. All inputs and output are TTL-compatible and operate from a single 5V supply.

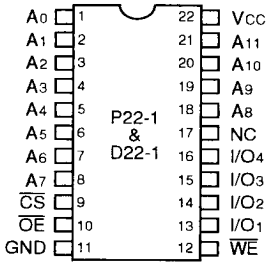
The IDT61970 is packaged in either a space saving 22-pin, 300-mil ceramic or plastic DIP, or a 24-pin SOJ, providing high board level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM

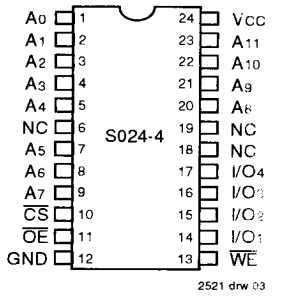


PIN CONFIGURATIONS



2521 drw 02

DIP
TOP VIEW



2521 drw 03

SOJ
TOP VIEW

2952 drw 03

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Value	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
TA	Operating Temperature	–55 to +125	°C
TBIAS	Temperature Under Bias	–65 to +135	°C
TSTG	Storage Temperature	–65 to +150	°C
PT	Power Dissipation	1.0	W
IOUT	DC Output Current	50	mA

2952 tbl 02

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.

PIN NAMES

A0 – A11	Address	$\overline{WE}$	Write Enable
I/O1 – I/O4	Data Input/Output	$\overline{OE}$	Output Enable
VCC	Power	$\overline{CS}$	Chip Select
GND	Ground	NC	No Connection

2952 tbl 01

5

TRUTH TABLE(1)

Mode	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O	Power
Standby	H	X	X	High-Z	Standby
Read	L	H	L	DATAOUT	Active
Write	L	L	X	DATAIN	Active
Read	L	H	H	High-Z	Active

2952 tbl 08

NOTE:
1. H = VIH, L = VIL, X = Don't Care.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition		61970S Min.	61970S Max.	61970L Min.	61970L Max.	Unit
|ILI|	Input Leakage Current	VCC = Max.	Mil.	—	10	—	5	µA
		VIN = GND to VCC	Com'l.	—	2	—	2	
|ILO|	Output Leakage Current	VCC = Max., $\overline{CS}$ = VIH,	Mil.	—	10	—	5	µA
		VCC = GND to VCC	Com'l.	—	2	—	2	
VOL	Output Low Voltage	IOL = 10mA, VCC = Min.		—	0.5	—	0.5	V
		IOL = 8mA, VCC = Min.		—	0.4	—	0.4	V
VOH	Output High Voltage	IOH = –4mA, VCC = Min.		2.4	—	2.4	—	V

2952 tbl 03

CAPACITANCE (TA = +25°C, f = 1MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	8	pF
COUT	Output Capacitance	VOUT = 0V	8	pF

NOTE:
1. This parameter is determined by device characterization, but is not production tested

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	–	6.0	V
VIL	Input Low Voltage	–0.5(1)	–	0.8	V

2952 tbl 05

NOTE:
1. VIL (min.) = –3.0V for pulse width less than 20ns, once per cycle.

DC ELECTRICAL CHARACTERISTICS[1] $V_{CC} = 5.0V \pm 10\%$, $V_{LC} = 0.2V$, $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	Power	61970S10		61970S12[4]		61970S15		61970S20 61970L20		61970S25 61970L25		61970S35 61970L35		61970S45/55[3] 61970L45/55[3]		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC1}	Operating Power Supply Current $\overline{CS} = V_{IL}$, Outputs Open, V_{CC} = Max., f = 0[2]	S	120	—	110	120	110	120	90	100	90	100	90	100	—	100	mA
		L	—	—	—	—	—	—	70	80	70	80	70	80	—	80	
I_{CC2}	Dynamic Operating Current, $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	S	175	—	165	175	145	165	120	120	110	120	100	110	—	110	mA
		L	—	—	—	—	—	—	100	110	90	100	80	90/80	—	80	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \geq V_{IH}$, V_{CC} = Max., Outputs Open, f = f_{MAX}[2]	S	65	—	65	65	55	60	45	45	35	45	30	35	—	35	mA
		L	—	—	—	—	—	—	30	35	25	30	20	25	—	20	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \geq V_{HC}$, V_{CC} = Max., $V_{IN} \geq V_{HC}$ or $V_{IN} \leq V_{LC}$, f = 0[2]	S	20	—	20	20	20	20	20	20	3	10	3	10	—	10	mA
		L	—	—	—	—	—	—	0.5	5	0.5	0.3	0.5	0.3	—	0.3	

2952 tbl 04

NOTES:
1. All values are maximum guaranteed values.
2. $f_{MAX} = 1/t_{RC}$, only address inputs are cycling at f_{MAX}. f = 0 means no address inputs are changing.
3. –55°C to +125°C temperature range only.
4. Military values are preliminary only.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	–55° to +125°C	0V	5.0V ±10%
Commercial	0°C to +70°C	0V	5.0V ±10%

2952 tbl 09

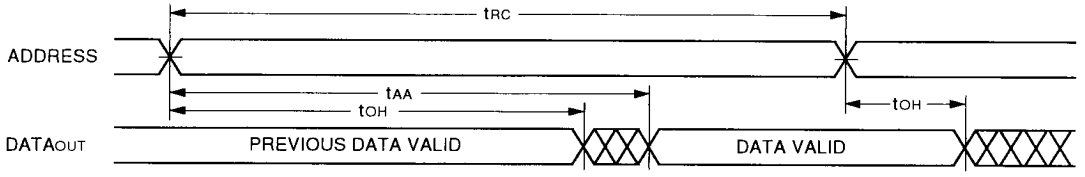
AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	61970S10		61970S12[2]		61970S15		61970S20/25 61970L20/25		61970S35/45 61970L35/45		61970S55 61970L55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle														
t_{RC}	Read Cycle Time	10	—	12	—	15	—	20/25	—	35/45	—	55	—	ns
t_{AA}	Address Access Time	—	10	—	12	—	15	—	20/25	—	35/45	—	55	ns
t_{OE}	Output Enable Access Time	—	5	—	5	—	6	—	8/10	—	12/15	—	20	ns
t_{OLZ}	Output Low-Z Time[1]	2	—	2	—	2	—	2	—	2	—	2	—	ns
t_{OHZ}	Output High-Z Time[1]	—	6	—	7	—	9	—	12	—	15	—	15	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	3	—	3	—	ns
t_{ACS}	Chip Select Access Time	10	—	12	—	15	—	20/25	—	35/45	—	55	—	ns
t_{CLZ}	Chip Select to Output in Low-Z[1]	3	—	3	—	3	—	3	—	3	—	3	—	ns
t_{CHZ}	Chip Deselect to Output in High-Z[1]	—	6	—	7	—	8	—	10	—	15	—	25	ns
t_{PU}	Chip Select to Power-up Time[1]	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{PD}	Chip Deselect Power-down Time[1]	—	10	—	12	—	15	—	20/25	—	35/45	—	55	ns

2952 tbl 06

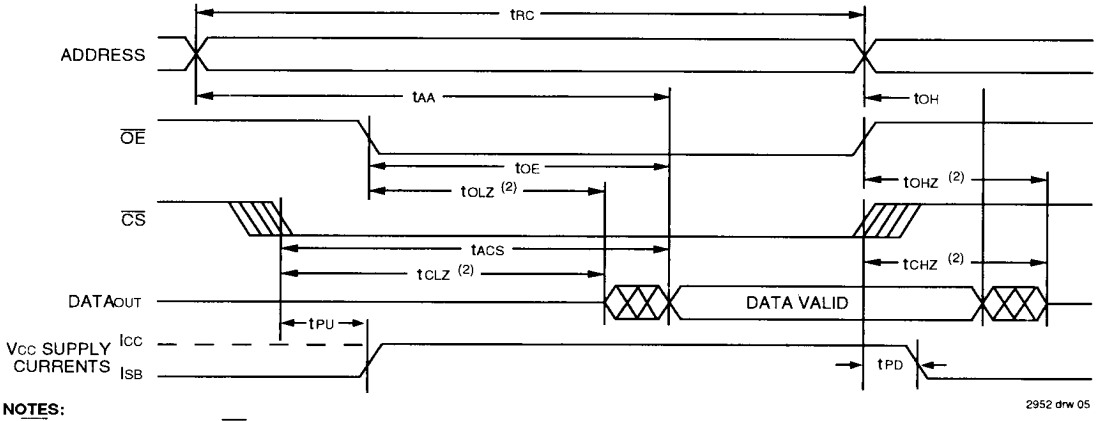
NOTE:
1. This parameter is guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.
2. Military values are preliminary only.

TIMING WAVEFORM OF READ CYCLE NO. 1[1,4]



2952 drw 04

TIMING WAVEFORM OF READ CYCLE NO. 2[1,3]



2952 drw 05

NOTES:
1. $\overline{WE}$ is HIGH for read cycle, $\overline{WE} \geq V_{IH}$.
2. Transition is measured ±200mV from steady state.
3. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
4. Device is continuously selected, $\overline{CS} \leq V_{IL}$.

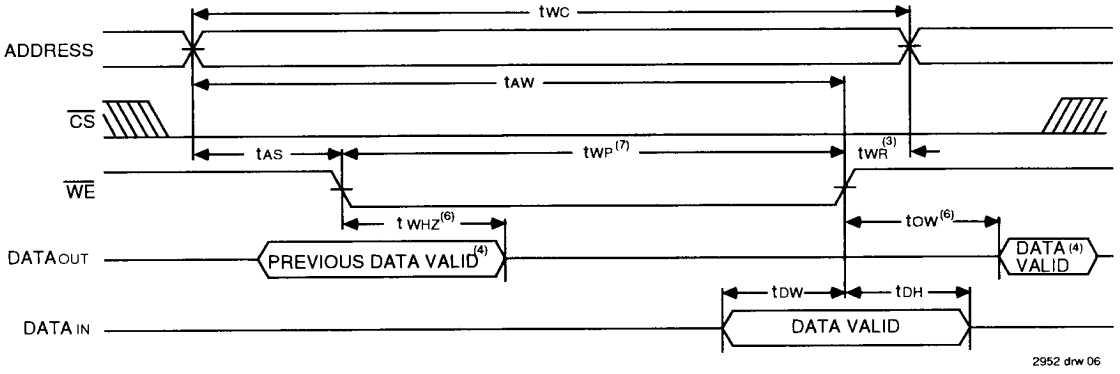
AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	61970S10 Min.	61970S10 Max.	61970S12[3] Min.	61970S12[3] Max.	61970S15 Min.	61970S15 Max.	61970S20/25 61970L20/25 Min.	61970S20/25 61970L20/25 Max.	61970S35/45 61970L35/45 Min.	61970S35/45 61970L35/45 Max.	61970S55 61970L55 Min.	61970S55 61970L55 Max.	Unit
Write Cycle														
tWC	Write Cycle Time	10	—	12	—	15	—	20/25	—	35/45	—	55	—	ns
tAW	Address Valid to End of Write	8	—	10	—	12	—	15/20	—	25/30	—	35	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	8	—	8	—	10	—	12/15	—	20/25	—	30	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	7	—	8	—	9	—	10/13	—	17/20	—	20	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tWHZ	Write Enable to Output in High-Z[1,2]	—	5	—	6	—	7	—	9	—	13/20	—	25	ns
tOW	Output Active From End of Write[1,2]	0	—	0	—	0	—	0	—	0	—	0	—	ns
tCW	Chip Select to End of Write	8	—	10	—	12	—	15/20	—	25/30	—	35	—	ns

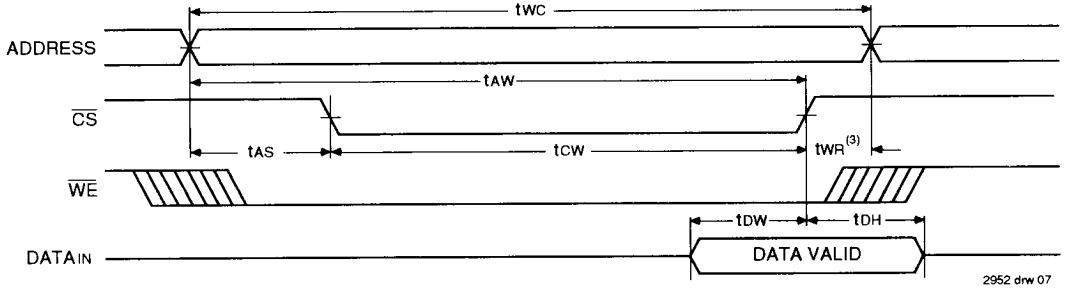
NOTES:
1. Transition is measured ±200mV from steady state.
2. This parameter is guaranteed with the AC load (Figure 2) by device characterization, but is not production tested.
3. Military values are preliminary only.

2952 tbl 07

TIMING WAVEFORM OF WRITE CYCLE NO. 1, ($\overline{WE}$ Controlled Timing)(1, 2, 5, 7)



TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CS}$ Controlled Timing)(1, 2, 5, 7)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and input signals should not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in the high-impedance state.
6. Transition is measured ±200mV from steady state.
7. $\overline{OE}$ is continuously HIGH. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP. For a $\overline{CS}$ controlled write cycle, $\overline{OE}$ may be LOW with no degradation to tCW.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

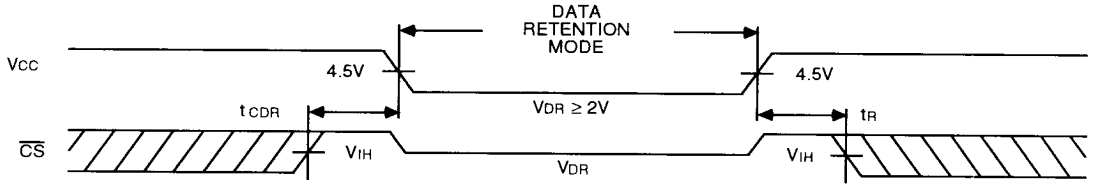
(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Condition		Min.	Typ.[1]	Max.	Unit
V_{DR}	V_{CC} for Data Retention	$\overline{CS} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$		2.0	—	—	V
I_{CCDR}	Data Retention Current		MIL.	— —	0.5[2] 1.0[3]	100[2] 150[3]	µA
			COM'L.	— —	0.5[2] 1.0[3]	20[2] 30[3]	µA
t_{CDR}[4]	Chip Deselect to Data Retention Time			0	—	—	ns
t_R[4]	Operation Recovery Time			t_{RC}[2]	—	—	ns

2952 tbl 10

NOTES:
1. T_A = +25°C.
2. at V_{CC} = 2V
3. at V_{CC} = 3V
4. This parameter is guaranteed by device characterization, but is not production tested.

LOW V_{CC} DATA RETENTION WAVEFORM

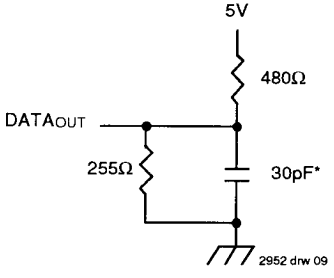


2952 drw 08

AC TEST CONDITIONS

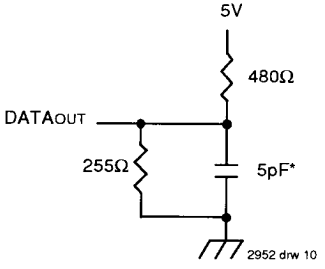
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2952 tbl 11



2952 drw 09

Figure 1. AC Test Load



2952 drw 10

Figure 2. AC Test Load
(for t_{OLZ}, t_{CLZ}, t_{OHZ}, t_{CHZ}, t_{OW} & t_{WZ})

* Including scope and jig.

ORDERING INFORMATION