



Integrated Device Technology, Inc.

CMOS STATIC RAM
64K (16K x 4-BIT)
IDT6198S
IDT6198L
FEATURES:

- Optimized for fast RISC processors including the IDT79R3000
- Output Enable ($\overline{OE}$) pin available for added system flexibility
- High-speed (equal access and cycle times)
 - Military: 20/25/35/45/55/70/85ns (max.)
 - Commercial: 15/20/25/35ns (max.)
- Low-power consumption
 - IDT6198S
 - Active: 350mW (typ.)
 - Standby: 100 μ W (typ.)
 - IDT6198L
 - Active: 300mW (typ.)
 - Standby: 30 μ W (typ.)
- JEDEC compatible pinout
- Battery back-up operation—2V data retention (L version only)
- 24-pin Cerdip, 24-pin plastic DIP, high-density 28-pin leadless chip carrier and 24-pin SOIC (gull-wing and J-bend)

- Produced with advanced CEMOS™ technology

- Bidirectional data inputs and outputs

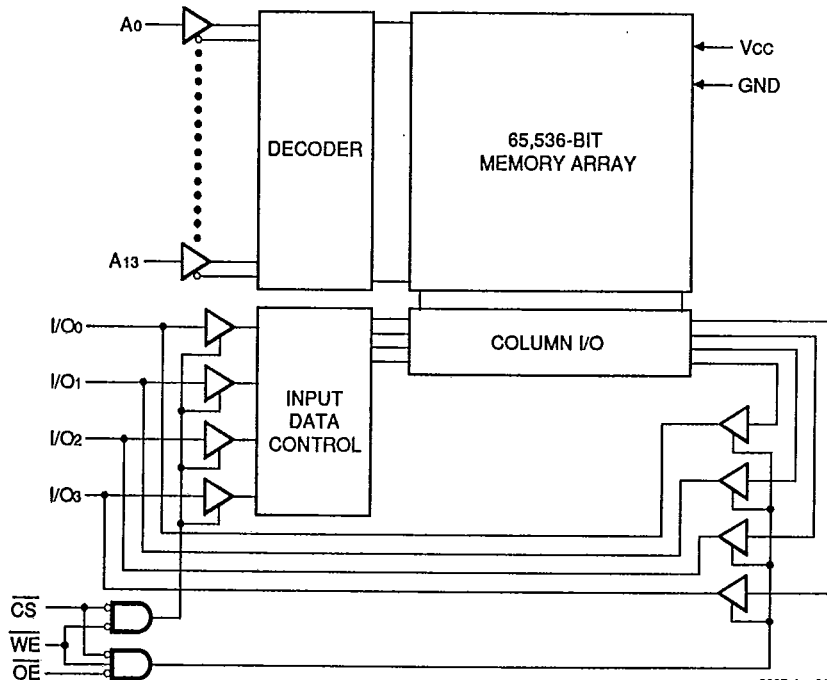
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT6198 is a 65,536-bit high-speed static RAM organized as 16K x 4. It is fabricated using IDT's high-performance, high-reliability technology—CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective approach for memory intensive applications. Timing parameters have been specified to meet the speed demands of the IDT79R3000 RISC processors.

The IDT6198 features two memory control functions: chip select ($\overline{CS}$) and output enable ($\overline{OE}$). These two functions greatly enhance the IDT6198's overall flexibility in high-speed memory applications.

Access times as fast as 15ns are available, with typical power consumption of only 300mW. The IDT6198 offers a reduced power standby mode, ISB_1 , which enables the designer to considerably reduce device power requirements. This capability significantly decreases system power and

FUNCTIONAL BLOCK DIAGRAM

CEMOS is a trademark of Integrated Device Technology, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES**DECEMBER 1990**

IDT6198S/L
CMOS STATIC RAM 64K (16K x 4-BIT)

MILITARY AND COMMERCIAL TEMPERATURE RANGES

DESCRIPTION (Continued)

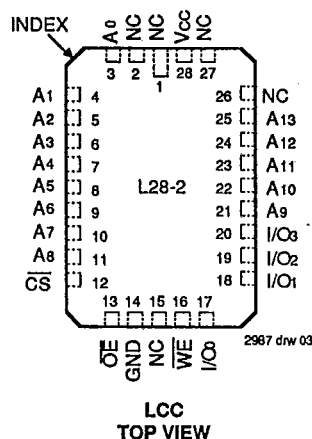
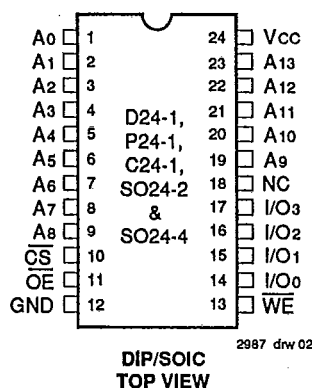
cooling levels, while greatly enhancing system reliability. The low-power version (L) also offers a battery backup data retention capability where the circuit typically consumes only 30μW when operating from a 2 volt battery.

All inputs and outputs are TTL-compatible and operate from a single 5 volt supply.

The IDT6198 is packaged in either a 24-pin 300 mil Cerdip or plastic DIP, 28-pin leadless chip carrier or 24-pin gull-wing or J-bend small outline IC.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

PIN CONFIGURATIONS



PIN DESCRIPTIONS

Name	Description
A0-A13	Address Inputs
CS	Chip Select
WE	Write Enable
OE	Output Enable
I/O0-I/O3	Data Input/Output
Vcc	Power
GND	Ground

2987 tbi 01

TRUTH TABLE⁽¹⁾

Mode	CS	WE	OE	I/O	Power
Standby	H	X	X	High Z	Standby
Read	L	H	L	DOUT	Active
Write	L	L	X	DIN	Active
Read	L	H	H	High Z	Active

NOTE:

1. H = VIH, L = VIL, X = Don't Care

2987 tbi 02

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
Pr	Power Dissipation	1.0	1.0	W
IOUT	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2987 tbi 03

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	7	pF
COUT	Output Capacitance	VOUT = 0V	7	pF

NOTE:

1. This parameter is determined by device characterization, but is not production tested.

2987 tbi 04

IDT6198S/L
CMOS STATIC RAM 64K (16K x 4-BIT)

MILITARY AND COMMERCIAL TEMPERATURE RANGES

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V _{IH}	Input High Voltage	2.2	—	6.0	V
V _{IL}	Input Low Voltage	-0.5 ⁽¹⁾	—	0.8	V

NOTE:

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

2987 tbl 05

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	V _{CC}
Military	-55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2987 tbl 06

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT6198S		IDT6198L		Unit
			Min.	Max.	Min.	Max.	
I _{LI}	Input Leakage Current	V _{CC} = Max., V _{IN} = GND to V _{CC}	MIL. COM'L.	— 10 5	— — —	5 2	μA
I _{LO}	Output Leakage Current	V _{CC} = Max., $\overline{CS}$ = V _{IH} , V _{OUT} = GND to V _{CC}	MIL. COM'L.	— 10 5	— — —	5 2	μA
V _{OL}	Output Low Voltage	I _{OL} = 10mA, V _{CC} = Min. I _{OL} = 8mA, V _{CC} = Min.	— —	0.5 0.4	— —	0.5 0.4	V
V _{OH}	Output High Voltage	I _{OL} = -4mA, V _{CC} = Min.	2.4	—	2.4	—	V

2987 tbl 07

DC ELECTRICAL CHARACTERISTICS⁽¹⁾

(V_{CC} = 5V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	6198S15 6198L15		6198S20 6198L20		6198S25 6198L25		6198S35 6198L35		6198S45 6198L45		6198S55/70/85 6198L55/70/85		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
ICC1	Operating Power Supply Current $\overline{CS}$ = V _{IL} , Outputs Open V _{CC} = Max., f = 0 ⁽²⁾	S	110	—	100	110	100	110	100	110	—	110	—	110	mA
		L	75	—	70	80	70	80	85	95	—	95	—	95	
ICC2	Dynamic Operating Current $\overline{CS}$ = V _{IL} , Outputs Open V _{CC} = Max., f = f _{MAX} ⁽²⁾	S	135	—	130	160	135	155	125	140	—	140	—	140	mA
		L	125	—	115	130	105	120	105	115	—	110	—	110	
ISB	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V _{IH} , V _{CC} = Max., Outputs Open, f = f _{MAX} ⁽²⁾	S	60	—	55	70	55	60	45	500	—	50	—	50	mA
		L	45	—	40	50	35	40	35	40	—	35	—	35	
ISB1	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V _{HC} , V _{CC} = Max., V _{IN} ≥ V _{HC} or V _{IN} ≤ V _{LC} , f = 0 ⁽²⁾	S	20	—	15	25	15	20	15	20	—	20	—	20	mA
		L	1.5	—	0.5	1.5	0.5	1.5	0.5	1.5	—	1.5	—	1.5	

NOTES:

1. All values are maximum guaranteed values.

2. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of 1/TRC. f = 0 means no input lines change.

2987 tbl 06

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

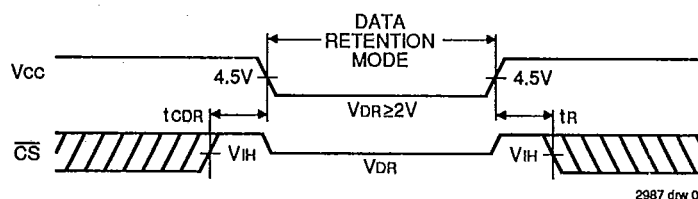
(L Version Only) $V_{LC} = 0.2V$, $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	Test Condition	Min.	Typ. ⁽¹⁾ V _{CC} @		Max. V _{CC} @		Unit
				2.0V	3.0V	2.0V	3.0V	
V _{DR}	V _{CC} for Data Retention	—	2.0	—	—	—	—	V
I _{CCDR}	Data Retention Current	MIL. COM'L.	—	10	15	600	900	μA
t _{CDR} ⁽³⁾	Chip Deselect to Data Retention Time	$\overline{CS} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	0	—	—	—	—	ns
t _R ⁽³⁾	Operation Recovery Time	t _{RC} ⁽²⁾	—	—	—	—	—	ns
I _{LI} ⁽³⁾	Input Leakage Current	—	—	—	—	2	2	μA

NOTES:

1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed, but not tested.

2967 tbl 09

LOW V_{CC} DATA RETENTION WAVEFORM

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2987 tbl 10

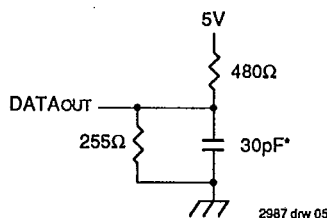
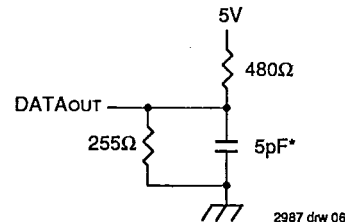


Figure 1. Output Load

Figure 2. Output Load
(for tOLZ, tCLZ, tOHZ, tWHZ, tCHZ and tOW)

*Includes scope and jig capacitances

IDT6198S/L
CMOS STATIC RAM 64K (16K x 4-BIT)

MILITARY AND COMMERCIAL TEMPERATURE RANGES

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%, All Temperature Ranges)

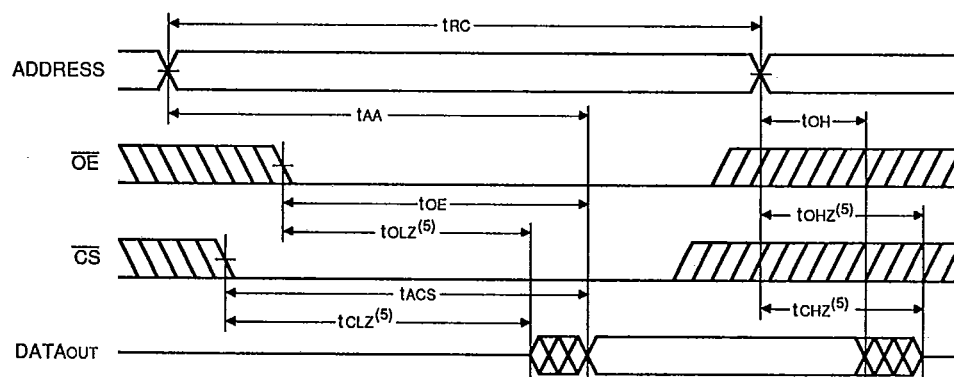
T-46-23-10

Symbol	Parameter	6198S15 ⁽¹⁾ 6198L15 ⁽¹⁾		6198S20 6198L20		6198S25 6198L25		6198S35 6198L35		6198S45/55 ⁽²⁾ 6198L45/55 ⁽²⁾		6198S70/85 ⁽²⁾ 6198L70/85 ⁽²⁾		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
		Read Cycle												
tRC	Read Cycle Time	15	—	20	—	25	—	35	—	45/55	—	70/85	—	ns
tAA	Address Access Time	—	15	—	19	—	25	—	35	—	45/55	—	70/85	ns
tACS	Chip Select Access Time	—	15	—	20	—	25	—	35	—	45/55	—	70/85	ns
tCLZ	Chip Select to Output in Low Z ⁽³⁾	5	—	5	—	5	—	5	—	5	—	5	—	ns
tOE	Output Enable to Output Valid	—	8	—	9	—	11	—	18	—	25/35	—	45/55	ns
tOLZ	Output Enable to Output in Low Z ⁽³⁾	5	—	5	—	5	—	5	—	5	—	5	—	ns
tCHZ	Chip Select to Output in High Z ⁽³⁾	2	7	2	8	2	10	2	14	—	15/20	—	25/30	ns
tOHZ	Output Disable to Output in High Z ⁽³⁾	2	7	2	8	2	9	2	15	—	15/20	—	25/30	ns
tOH	Output Hold from Address Change	5	—	5	—	2	—	5	—	5	—	5	—	ns
tPU	Chip Select to Power Up Time ⁽³⁾	0	—	0	—	0	—	0	—	0	—	0	—	ns
tPD	Chip Deselect to Power Down Time ⁽³⁾	—	15	—	20	—	25	—	35	—	45/55	—	70/85	ns

NOTES:

- 0° to +70°C temperature range only.
- 55°C to +125°C temperature range only.
- This parameter guaranteed but not tested.

2987 tbl 11

TIMING WAVEFORM OF READ CYCLE NO. 1⁽¹⁾

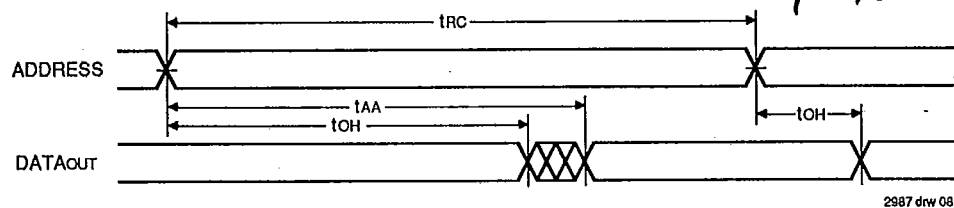
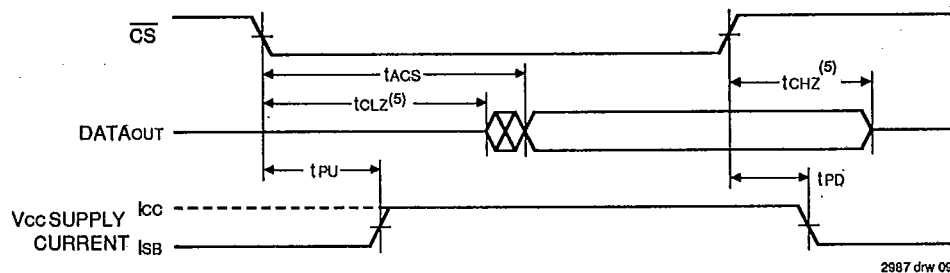
2987 drw 07

NOTES:

- WE is high for Read cycle.
- Device is continuously selected, $\overline{CS} = V_{IL}$.
- Address valid prior to or coincident with $\overline{CS}$ transition low.
- $\overline{OE} = V_{IL}$.
- Transition is measured ±200mV from steady state voltage.

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CMOS STATIC RAM 64K (16K x 4-BIT)

MILITARY AND COMMERCIAL TEMPERATURE RANGES

TIMING WAVEFORM OF READ CYCLE NO. 2^(1, 2, 4)TIMING WAVEFORM OF READ CYCLE NO. 3^(1, 3, 4)

NOTES:

1. WE is high for Read cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE} = V_{IL}$.
5. Transition is measured $\pm 200\text{mV}$ from steady state voltage.



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IDT6198S/L

CMOS STATIC RAM 64K (16K x 4-BIT)

MILITARY AND COMMERCIAL TEMPERATURE RANGES

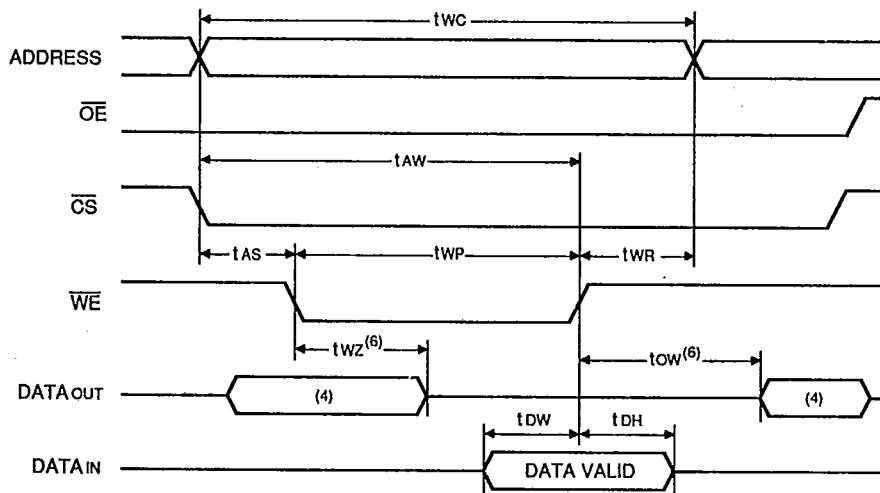
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	6198S15 ⁽¹⁾ 6198L15 ⁽¹⁾		6198S20 6198L20		6198S25 6198L25		6198S35 6198L35		6198S45/55 ⁽²⁾ 6198L45/55 ⁽²⁾		6198S70/85 ⁽²⁾ 6198L70/85 ⁽²⁾		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle														
tWC	Write Cycle Time	14	—	17	—	20	—	30	—	40/50	—	60/75	—	ns
tCW	Chip Select to End of Write	14	—	17	—	20	—	25	—	35/50	—	60/75	—	ns
tAW	Address Valid to End of Write	14	—	17	—	20	—	25	—	35/50	—	60/75	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	14	—	17	—	20	—	25	—	35/50	—	60/75	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tWHZ	Write Enable to Output in High Z ⁽³⁾	—	5	—	6	—	7	—	10	—	15/25	—	30/40	ns
tDW	Data Valid to End of Write	10	—	10	—	13	—	15	—	20/25	—	30/35	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tOW	Output Active from End of Write ⁽³⁾	5	—	5	—	5	—	5	—	5	—	5	—	ns

NOTES:

1. 0° to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.

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TIMING WAVEFORM OF WRITE CYCLE NO. 1 (WE CONTROLLED TIMING)^(1, 2, 3, 7)

2987 drw 10

NOTES:

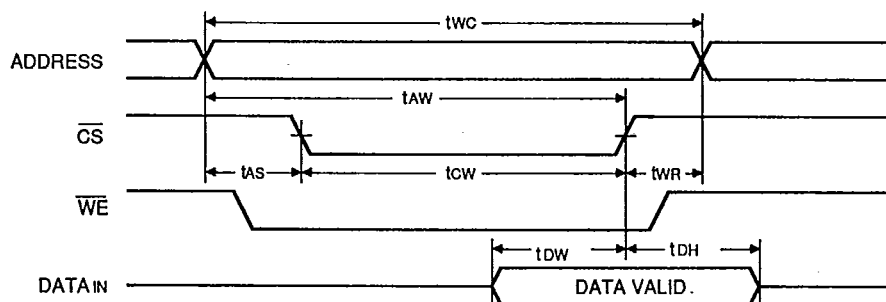
1. WE or CS must be high during all address transitions.
2. A write occurs during the overlap (t_{CW} t_{WP}) of a low CS and a low WE.
3. t_{WR} is measured from the earlier of CS or WE going high to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals must not be applied.
5. If the CS low transition occurs simultaneously with or after the WE low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state.
7. If OE is low during a WE controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ} + t_{OW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{OW}. If OE is high an WE controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.
8. OE = V_{IH}.

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CMOS STATIC RAM 64K (16K x 4-BIT)

MILITARY AND COMMERCIAL TEMPERATURE RANGES

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)^(1, 2, 3, 5, 8)



2987 drw 11

NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{CW}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ± 200 mV from steady state.
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or ($t_{WHZ} + t_{DW}$) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW} . If $\overline{OE}$ is high in a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP} .
8. $\overline{OE} = V_{IH}$.

ORDERING INFORMATION

IDT	XXXX	X	XX	XX	X	
	Device Type	Power	Speed	Package	Process/ Temperature Range	
					Blank	Commercial (0°C to +70°C)
					B	Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B
					C	Sidebrazed DIP (300 mil)
					D	CERDIP (300 mil)
					P	Plastic DIP (300 mil)
					L	Leadless Chip Carrier
					SO	Small Outline IC (Gull Wing)
					Y	Small Outline IC (J-Bend)
					15	Commercial Only
					20	
					25	
					35	
					45	Military Only
					55	Military Only
					70	Military Only
					85	Military Only
					S	Standard Power
					L	Low Power
					6198	16K x 4-Bit Static RAM

2987 drw 12

