



Integrated Device Technology, Inc.

HIGH-SPEED 2K x 9 DUAL-PORT STATIC RAM

PRELIMINARY
IDT7012

FEATURES:

- High-speed access
 - Military: 35/45/55/70ns (max.)
 - Commercial: 25/35/45/55ns (max.)
- Low-power operation
 - IDT7012S
 - Active: 400mW (typ.)
 - Standby: 7mW (typ.)
 - IDT7012L
 - Active: 400mW (typ.)
 - Standby: 2mW (typ.)
- Fully asynchronous operation from either port
- Each port has a 9-bit wide data path. The 9th bit could be used as the parity bit
- Battery backup operation — 2V data retention
- TTL compatible, single 5V ($\pm 10\%$) power supply
- Available in popular hermetic and plastic packages
- Military product compliant to MIL-STD-883, Class B
- Industrial temperature range (-40°C to $+85^{\circ}\text{C}$) is available, tested to military electrical specifications

DESCRIPTION:

The IDT7012 is a high-speed 2K x 9 dual-port static RAM designed to be used in systems where on-chip hardware port arbitration is not needed. This part lends itself to those systems which cannot tolerate wait states or are designed to be able to externally arbitrate or withstand contention when both sides simultaneously access the same dual-port location.

The IDT7012 provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. It is the user's responsibility to ensure data integrity when simultaneously accessing the same memory location from both ports. An automatic power-down feature, controlled by $\overline{\text{CE}}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

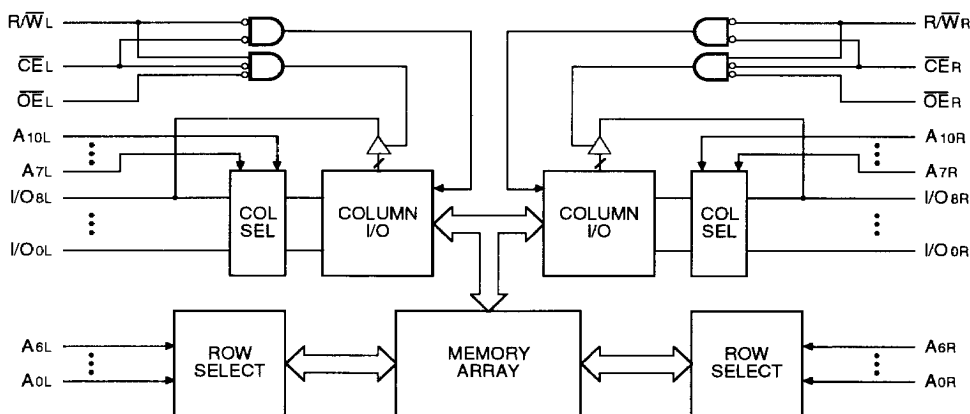
The IDT7012 utilizes a 9-bit wide data path to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only 400mW of power at maximum access times as fast as 25ns. Low-power (L) versions offer battery backup data retention capability, with each port typically consuming 200 μW from a 2V battery.

The IDT7012 is packaged in 48-pin sidebraced or plastic DIPs, 48-pin LCCs and 48-pin flatpacks. The military devices are processed 100% in compliance to the test methods of MIL-STD-883, Method 5004.

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FUNCTIONAL BLOCK DIAGRAM



CEMOS is a trademark of Integrated Device Technology, Inc.

2653 drw 01

MILITARY AND COMMERCIAL TEMPERATURE RANGES

APRIL 1992

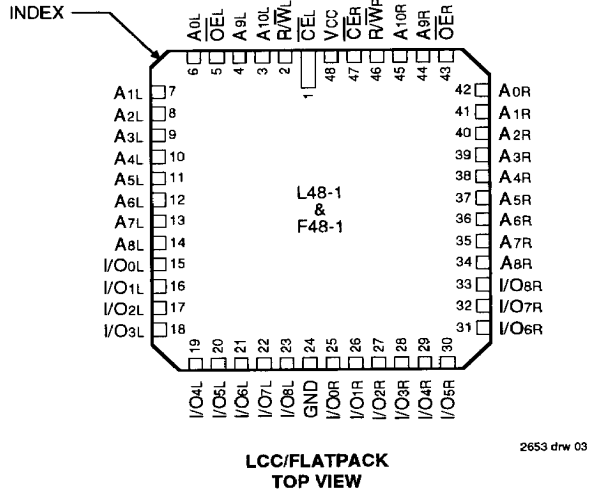
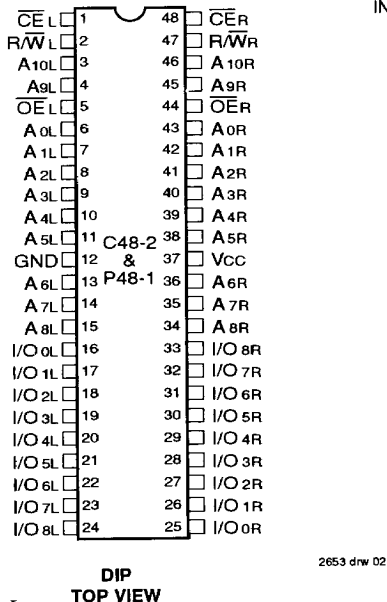
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DSC-1049/2

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PIN CONFIGURATIONS

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T _A	Operating Temperature	0 to +70	-55 to +125	°C
T _{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T _{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I _{OUT}	DC Output Current	50	50	mA

NOTE:

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- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{TERM} must not exceed V_{CC} + 0.5V.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Condition	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	11	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	11	pF

NOTE:

2653 tbl 13

- This parameter is sampled and not 100% tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	V _{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2653 tbl 02

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{CC}	Supply Voltage	4.5	5	5.5	V
GND	Supply Voltage	0	0	0.0	V
V _{IH}	Input High Voltage	2.2	—	6.0 ⁽²⁾	V
V _{IL}	Input Low Voltage	-0.5 ⁽¹⁾	—	0.8	V

NOTE:

2653 tbl 03

- V_{IL} = -3.0V for pulse width less than 20ns.
- V_{TERM} must not exceed V_{CC} + 0.5V.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE ($V_{CC} = 5.0V \pm 10\%$)

Symbol	Parameter	Test Condition	7012S		7012L		Unit
			Min.	Max.	Min.	Max.	
$ I_{LQ} $	Input Leakage Current ⁽⁷⁾	$V_{CC} = 5.5V$, $V_{IN} = 0V$ to V_{CC}	—	10	—	5	μA
$ I_{LO} $	Output Leakage Current	$\overline{CE} = V_{IH}$, $V_{OUT} = 0V$ to V_{CC}	—	10	—	5	μA
V_{OL}	Output Low Voltage	$I_{OL} = 4mA$	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	$I_{OH} = -4mA$	2.4	—	2.4	—	V

2653 tbi 04

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE^(1,6) ($V_{CC} = 5.0V \pm 10\%$)

Symbol	Parameter	Test Condition	Version	7012 x 25 ⁽²⁾		7012 x 35		7012 x 45		7012 x 55		7012 x 70 ⁽³⁾		Unit	
				Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.		
I _{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE} \leq V_{IL}$ Outputs Open $f = f_{MAX}^{(4)}$	Mil.	S	—	—	125	290	125	285	125	280	125	275	mA
				L	—	—	125	230	125	225	125	220	125	215	
I _{SB1}	Standby Current (Both Ports—TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$ $f = f_{MAX}^{(4)}$	Mil.	S	—	—	30	80	30	80	30	80	30	80	mA
				L	—	—	30	60	30	60	30	60	30	60	
			Com'l.	S	125	260	125	250	125	245	125	240	—	—	
				L	125	220	125	210	125	205	125	200	—	—	
I _{SB2}	Standby Current (One Port—TTL Level Inputs)	$\overline{CE}_L$ or $\overline{CE}_R \geq V_{IH}$ Active Port Outputs Open, $f = f_{MAX}^{(4)}$	Mil.	S	—	—	80	185	80	180	80	175	80	170	mA
				L	—	—	80	150	80	145	80	140	80	135	
			Com'l.	S	80	175	80	165	80	160	80	155	—	—	
				L	80	145	80	135	80	130	80	125	—	—	
I _{SB3}	Full Standby Current (Both Ports—All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, $f = 0^{(5)}$	Mil.	S	—	—	1.0	30	1.0	30	1.0	30	1.0	30	mA
				L	—	—	0.2	10	0.2	10	0.2	10	0.2	10	
			Com'l.	S	1.0	15	1.0	15	1.0	15	1.0	15	—	—	
				L	0.2	5	0.2	5	0.2	5	0.2	5	—	—	
I _{SB4}	Full Standby Current (One Port—All CMOS Level Inputs)	One Port $\overline{CE}_L$ or $\overline{CE}_R \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ Active Port Outputs Open, $f = f_{MAX}^{(4)}$	Mil.	S	—	—	70	175	70	170	70	165	70	160	mA
				L	—	—	70	140	70	135	70	130	70	125	
			Com'l.	S	70	170	70	160	70	155	70	150	—	—	
				L	70	140	70	130	70	125	70	120	—	—	

NOTES:

- "x" in part numbers indicates power rating (S or L).
- 0°C to +70°C temperature range only.
- 55°C to +125°C temperature range only.
- At $f = f_{MAX}$, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of $1/f_{IC}$, and using "AC TEST CONDITIONS" of input levels of GND to 3V.
- $f = 0$ means no address or control lines change. Applies only to inputs at CMOS level standby.
- $V_{CC} = 5V$, $T_A = +25^\circ C$ for Typ.
- At $V_{CC} \leq 2.0V$ input leakages are undefined.

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DATA RETENTION CHARACTERISTICS (L Version Only)

Symbol	Parameter	Test Condition	7012L			Unit
			Min.	Typ. ⁽¹⁾	Max.	
V _{DR}	V _{CC} for Data Retention	V _{CC} = 2.0V, $\overline{CE} \geq V_{CC} - 0.2V$	2	—	—	V
I _{CCDR}	Data Retention Current		Mil. —	100	4000	μA
t _{CDR} ⁽³⁾	Chip Deselect to Data Retention Time	V _{IN} ≥ V _{CC} - 0.2V or V _{IN} ≤ 0.2V	Com'l. —	100	1500	μA
t _{tr} ⁽³⁾	Operation Recovery Time		0	—	—	ns
			t _{RC} ⁽²⁾	—	—	ns

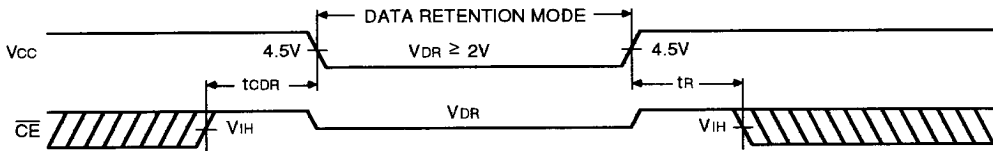
NOTES:

1. V_{CC} = 2V, T_A = +25°C.2. t_{RC} = Read Cycle Time.

3. This parameter is guaranteed but not tested.

2653 tbl 06

DATA RETENTION WAVEFORM

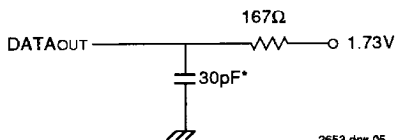


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AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

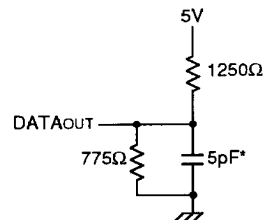
2653 tbl 07



2653 drw 05

* Including scope and jig.

Figure 1. Equivalent Output Load



2653 drw 06

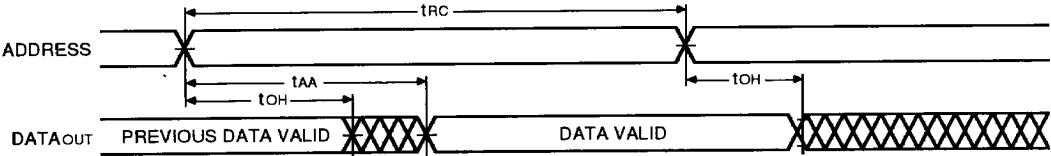
Figure 2. Output Load
(for t_{HZ}, t_{LZ}, t_{WZ} and t_{OW})

AC ELECTRICAL CHARACTERISTICS OVER THE
OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE⁽⁵⁾

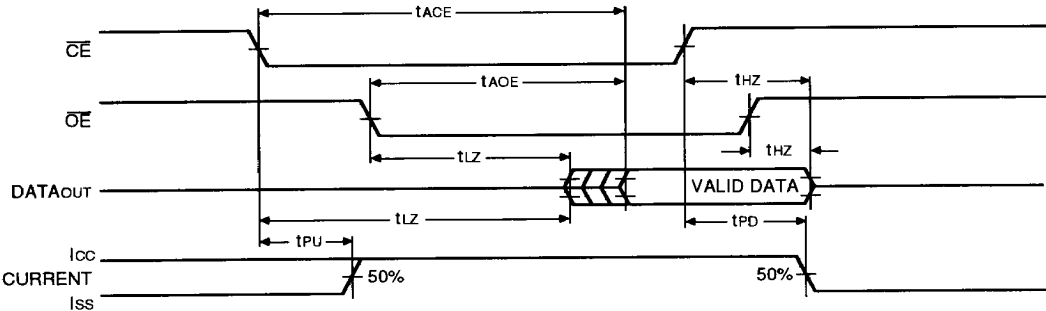
Symbol	Parameter	7012 x 25 ⁽²⁾		7012 x 35		7012 x 45		7012 x 55		7012 x 70 ⁽³⁾		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
t _{RC}	Read Cycle Time	25	—	35	—	45	—	55	—	70	—	ns
t _{AA}	Address Access Time	—	25	—	35	—	45	—	55	—	70	ns
t _{ACE}	Chip Enable Access Time	—	25	—	35	—	45	—	55	—	70	ns
t _{AOE}	Output Enable Access Time	—	12	—	25	—	30	—	35	—	40	ns
t _{OH}	Output Hold From Address Change	0	—	0	—	0	—	0	—	0	—	ns
t _{LZ}	Output Low Z Time ^(1,4)	0	—	0	—	0	—	0	—	0	—	ns
t _{HZ}	Output High Z Time ^(1,4)	—	10	—	15	—	20	—	30	—	35	ns
t _{PU}	Chip Enable to Power-Up Time ⁽⁴⁾	0	—	0	—	0	—	0	—	0	—	ns
t _{PD}	Chip Disable to Power-Down Time ⁽⁴⁾	—	50	—	50	—	50	—	50	—	50	ns

- NOTES:
- 1. Transition is measured ±500mV from low or high impedance voltage with load (Figures 1 and 2).
 - 2. 0°C to +70°C temperature range only.
 - 3. -55°C to +125°C temperature range only.
 - 4. This parameter guaranteed but not tested.
 - 5. "x" in part numbers indicates power rating (S or L).

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE^(1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE^(1, 3)



- NOTES:
- 1. R/W is high for Read Cycles.
 - 2. Device is continuously enabled, $\overline{CE} = V_{IL}$.
 - 3. Addresses valid prior to coincident with $\overline{CE}$ transition low.
 - 4. $\overline{OE} = V_{IL}$.

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AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE⁽⁶⁾

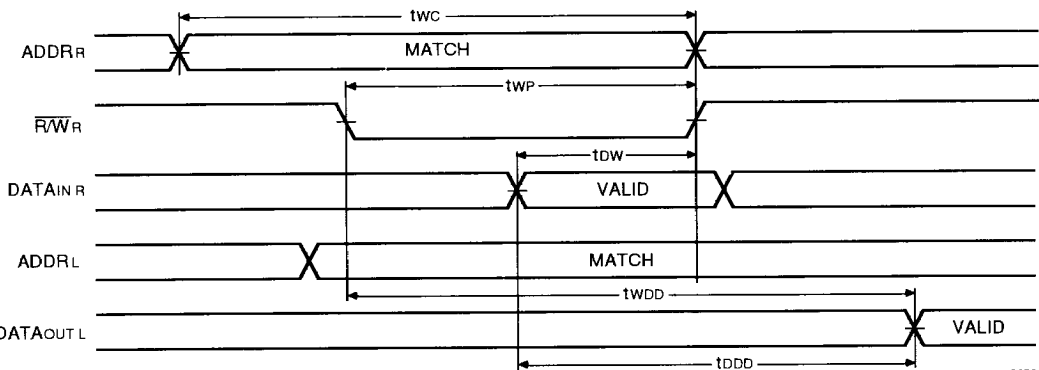
Symbol	Parameter	7012 x 25 ⁽²⁾		7012 x 35		7012 x 45		7012 x 55		7012 x 70 ⁽³⁾		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle												
tWC	Write Cycle Time	25	—	35	—	45	—	55	—	70	—	ns
tEW	Chip Enable to End of Write	20	—	30	—	35	—	40	—	50	—	ns
tAW	Address Valid to End of Write	20	—	30	—	35	—	40	—	50	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width ⁽⁵⁾	20	—	30	—	35	—	40	—	50	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	12	—	20	—	20	—	20	—	30	—	ns
tHZ	Output High Z Time ^(1,4)	—	10	—	15	—	20	—	30	—	35	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns
tWZ	Write Enabled to Output in High Z ^(1,4)	—	10	—	15	—	20	—	30	—	35	ns
tOW	Output Active From End of Write ^(1,4)	0	—	0	—	0	—	0	—	0	—	ns
tWDD	Write Pulse to Data Delay	—	50	—	60	—	70	—	80	—	95	ns
tDDD	Write Data Valid to Read Data Delay	—	35	—	45	—	55	—	65	—	80	ns

NOTES:

1. Transition is measured $\pm 500\text{mV}$ from low or high impedance voltage with load (Figures 1 and 2).
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. This parameter guaranteed but not tested.
5. Specified for OE at high (refer to "Timing Waveform of Write Cycle", Note 7).
6. "x" in part numbers indicates power rating (S or L).

2653 tbl 09

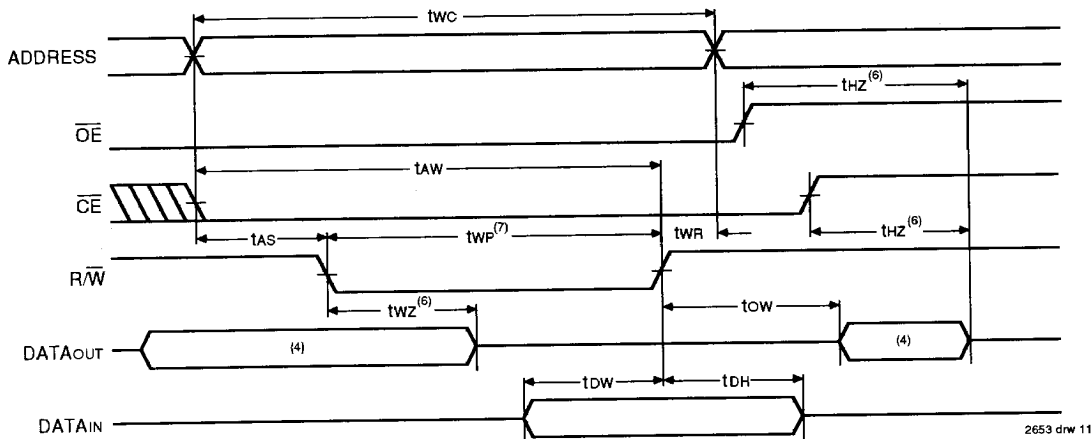
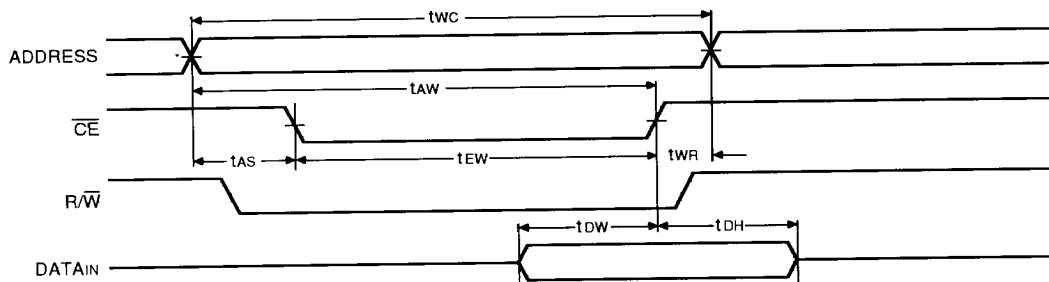
TIMING WAVEFORM OF READ WITH PORT-TO-PORT DELAY⁽¹⁾



2653 drw 14

NOTE:

1. Write cycle parameters should be adhered to in order to ensure proper writing.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, (R/W CONTROLLED TIMING)^(1, 2, 3, 7)TIMING WAVEFORM OF WRITE CYCLE NO. 2, (CE CONTROLLED TIMING)^(1, 2, 3, 5)

NOTES:

1. R/W must be high during all address transitions.
2. A write occurs during the overlap (tEW or tWP) of a low CE and a low R/W.
3. tWR is measured from the earlier of CE or R/W going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the CE low transition occurs simultaneously with or after the R/W low transition, the outputs remain in the high impedance state.
6. Transition is measured $\pm 500\text{mV}$ from steady state with a 5pF load (including scope and jig).
7. If OE is low during a R/W controlled write cycle, the write pulse width must be the larger of tWP or (tWZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tWZ. If OE is high during a R/W controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

FUNCTIONAL DESCRIPTION

The IDT7012 provides two ports with separate control, address, and I/O pins that permit independent access for reads or writes to any location in memory. These devices have an automatic power-down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power-down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ high). When a port is enabled, access to the entire memory array is permitted. Each port has its own Output Enable control ($\overline{OE}$). In the read mode, the port's $\overline{OE}$ turns on the output drivers when set LOW. Non-contention READ/ WRITE conditions are illustrated in the truth table below.

TRUTH TABLE
NON-CONTENTION
READ/WRITE CONTROL

Left or Right Port ⁽¹⁾				Function
R/W	$\overline{CE}$	$\overline{OE}$	Do-s	
X	H	X	Z	Port Disabled and in Power-Down Mode, ISB2 or ISB4
X	H	X	Z	$\overline{CE} = \overline{CE}_L = H$, Power-Down Mode, ISB1 or ISB3
L	L	X	DATA _{IN}	Data on Port Written Into Memory ⁽²⁾
H	L	L	DATA _{OUT}	Data in Memory Output on Port
X	X	H	Z	High Impedance Outputs

NOTES:

2653 tbl 11

1. A0L - A10L $\neq$ A0R - A10R

2. H = HIGH, L = LOW, X = DON'T CARE, Z = HIGH IMPEDANCE

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