Integrated Device Technology, Inc.

# HIGH-SPEED 4K x 16 DUAL-PORT STATIC RAM

**ADVANCE INFORMATION**
**IDT 7024**

T-46-23-31

## FEATURES:

- High-speed access
  - Military: 45/55/70/90ns (max.)
  - Commercial: 30/35/45/55/70/90ns (max.)
- Low-power operation
  - IDT7024S
    - Active: ---mW (typ.)
    - Standby: --mW (typ.)
  - IDT7024L
    - Active: ---mW (typ.)
    - Standby: ---mW (typ.)
- Separate upper-byte and lower-byte control for multiplexed bus compatibility.
- IDT7024 easily expands data bus width to 32 bits or more using the Master/Slave chip select when cascading more than one device
- On-chip port arbitration logic
- Versatile pin-select for Master or Slave:
  M/$\overline{S}$ = H for $\overline{BUSY}$ output flag on Master
  M/$\overline{S}$ = L for $\overline{BUSY}$ input on Slave
- $\overline{INT}$ flag for port-to-port communication
- Full on-chip hardware support of semaphore signaling between ports
- Fully asychronous operation from either port
- Battery backup operation—2V data retention
- TTL compatible, single 5V (±10%) power supply
- Available in 84-pin PGA

## DESCRIPTION:

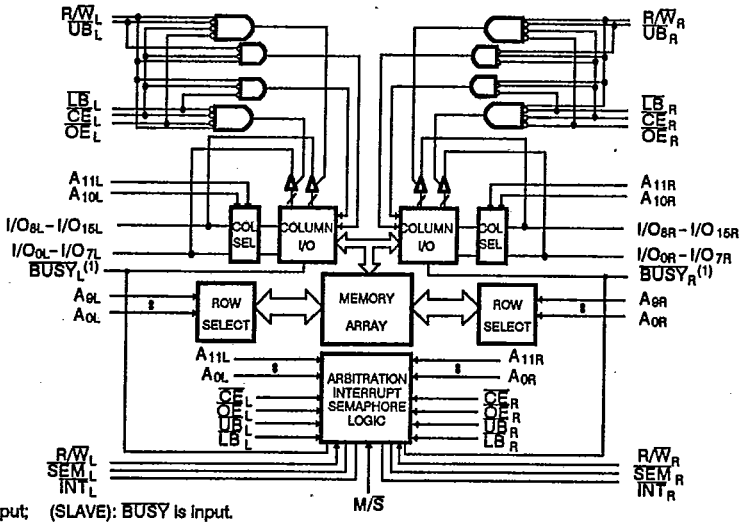
The IDT7024 is a high-speed 4K x 16 dual-port static RAM. The IDT7024 is designed to be used as a stand-alone 64K-bit dual-port RAM or as a combination MASTER/SLAVE dual-port RAM for 32-bit-or-more word width systems. Using the IDT MASTER/SLAVE dual-port RAM approach in 32 bit or wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

Both devices provide two independent ports with separate control, address and I/O pins that permit independent, asychronous access for reads or writes to any location in memory. An automatic power down feature controlled by $\overline{CE}$ permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CEMOS™ high-performance technology, these devices typically operate on only ---mW of power at maximum access times as fast as 30ns. Low-power (L) versions offer battery backup data retention capability with each port typically consuming ---µW from a 2V battery.

The IDT7024 is packaged in plastic as well as ceramic 84-pin PGA and 84-pin quad flatpack. The military devices are processed 100% in compliance to the test methods of MIL-STD-883, method 5004.

## FUNCTIONAL BLOCK DIAGRAM




**NOTES:**
1. (MASTER): $\overline{BUSY}$ is output; (SLAVE): $\overline{BUSY}$ is input.
2. LB = Lower Byte. UB = Upper Byte.

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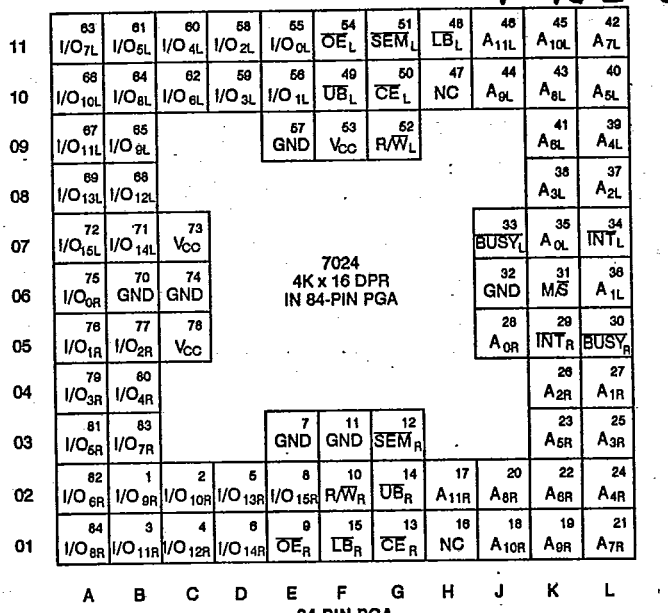
DSC-1045/-

## PIN NAMES

| LEFT PORT | RIGHT PORT | NAMES |
|---|---|---|
| $\overline{CE}_L$ | $\overline{CE}_R$ | Chip Enable |
| $R/\overline{W}_L$ | $R/\overline{W}_R$ | Read/Write Enable |
| $\overline{OE}_L$ | $\overline{OE}_R$ | Output Enable |
| $A_{0L-11L}$ | $A_{0R-11R}$ | Address |
| $I/O_{0L-15L}$ | $I/O_{0R-15R}$ | Data Input/Output |
| $\overline{SEM}_L$ | $\overline{SEM}_R$ | Semaphore Enable |
| $\overline{UB}_L$ | $\overline{UB}_R$ | Upper Byte Select |
| $\overline{LB}_L$ | $\overline{LB}_R$ | Lower Byte Select |
| $\overline{INT}_L$ | $\overline{INT}_R$ | Interrupt Flag |
| $\overline{BUSY}_L$ | $\overline{BUSY}_R$ | Busy Flag |
| $V_{CC}$ | | Power |
| GND | | Ground |
| $M/\overline{S}$ | | Master or Slave Select |




84-PIN PGA
TOP VIEW

## TRUTH TABLE: NON-CONTENTION READ/WRITE CONTROL

| INPUTS | | | | | | OUTPUTS | | MODE |
|---|---|---|---|---|---|---|---|---|
| $\overline{CE}$ | R/$\overline{W}$ | $\overline{OE}$ | $\overline{UB}$ | $\overline{LB}$ | $\overline{SEM}$ | $I/O_8 - I/O_{15}$ | $I/O_0 - I/O_7$ | |
| H | X | X | X | X | H | Hi-Z | Hi-Z | Deselected: Power Down |
| X | X | X | H | H | H | Hi-Z | Hi-Z | Deselected: Power Down |
| L | L | X | L | H | H | $DATA_{IN}$ | Hi-Z | Write to Upper Byte Only |
| L | L | X | H | L | H | Hi-Z | $DATA_{IN}$ | Write to Lower Byte Only |
| L | L | X | L | L | H | $DATA_{IN}$ | $DATA_{IN}$ | Write to Both Bytes |
| L | H | L | L | H | H | $DATA_{OUT}$ | Hi-Z | Read Upper Byte Only |
| L | H | L | H | L | H | Hi-Z | $DATA_{OUT}$ | Read Lower Byte Only |
| L | H | L | L | L | H | $DATA_{OUT}$ | $DATA_{OUT}$ | Read Both Bytes |
| X | X | H | X | X | X | Hi-Z | Hi-Z | Outputs Disabled |
| H | H | L | X | X | L | $DATA_{OUT}$ | $DATA_{OUT}$ | Read Data In Sema. Flag |
| X | H | L | H | H | L | $DATA_{OUT}$ | $DATA_{OUT}$ | Read Data In Sema. Flag |
| H | ↑ | X | X | X | L | $DATA_{IN}$ | $DATA_{IN}$ | Write $D_{IN0}$ into Sema. Flag |
| X | ↑ | X | H | H | L | $DATA_{IN}$ | $DATA_{IN}$ | Write $D_{IN0}$ into Sema. Flag |
| L | X | X | L | X | L | – | – | Not Allowed |
| L | X | X | X | L | L | – | – | Not Allowed |

Note:
1. $A_{0L} - A_{13R} \neq A_{0R} - A_{13R}$

## TRUTH TABLE: ARBITRATION OPTIONS

| OPTIONS | INPUTS | | | | | OUTPUTS | |
|---|---|---|---|---|---|---|---|
| | $\overline{CE}$ | $\overline{UB}$ | $\overline{LB}$ | $M/\overline{S}$ | $\overline{SEM}$ | $\overline{BUSY}$ | $\overline{INT}$ |
| Busy Logic Master | L<br>L | X<br>L | L<br>X | H<br>H | H<br>H | Output Signal | – |
| Busy Logic Slave | L<br>L | X<br>L | L<br>X | L<br>L | H<br>H | Input Signal | – |
| Interrupt Logic | L<br>L | X<br>L | L<br>X | X<br>X | H<br>H | – | Output Signal |
| Semaphore Logic* | H<br>H | X<br>X | X<br>X | H<br>L | L<br>L | H<br>Hi-Z | – |

*Inputs Signals are for Semaphore Flags set and test (Write and Read) operations

Note:
1. All $V_{CC}$ pins have to be connected to power supply.
2. All GND pins have to be connected ground supply.

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## ORDERING INFORMATION