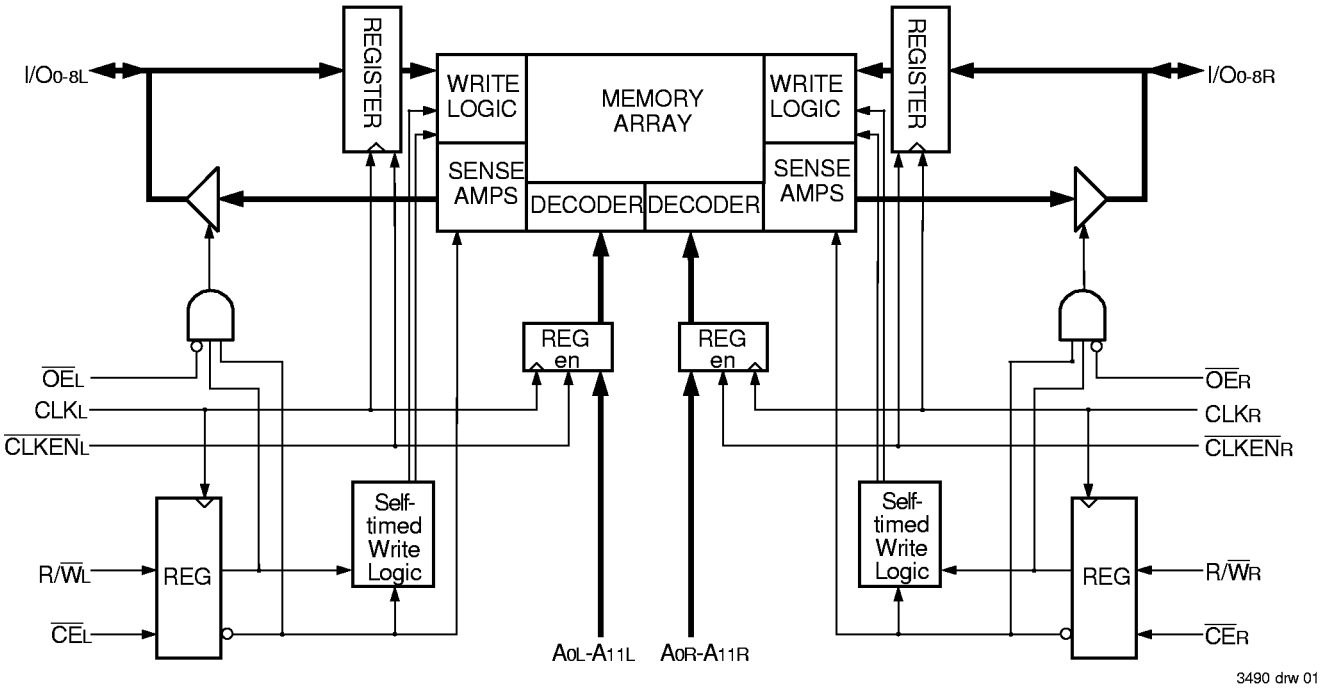
HIGH SPEED 36K (4K X 9) SYNCHRONOUS DUAL-PORT RAM

IDT70914S

Features

- **High-speed clock-to-data output times**
  - *Military: 20/25ns (max.)*
  - *Commercial: 12/15/20ns (max.)*
- **Low-power operation**
  - *IDT70914S*
    Active: 850 mW (typ.)
    Standby: 50 mW (typ.)
- **Architecture based on Dual-Port RAM cells**
  - *Allows full simultaneous access from both ports*
- **Synchronous operation**
  - *4ns setup to clock, 1ns hold on all control, data, and address inputs*
  - *Data input, address, and control registers*
  - *Fast 12ns clock to data out*
  - *Self-timed write allows fast cycle times*
  - *17ns cycle times, 58MHz operation*
- **TTL-compatible, single 5V (± 10%) power supply**
- **Clock Enable feature**
- **Guaranteed data output hold times**
- **Available in 68-pin PGA, PLCC, and 80-pin TQFP**
- **Military product compliant to MIL-PRF-38535 QML**
- **Industrial temperature range (-40°C to +85°C) is available for selected speeds.**
- **Recommended for replacement of IDT7099 (4K x 9) if separate 9th bit data control signals are not required.**

Functional Block Diagram



MARCH 1999

Description

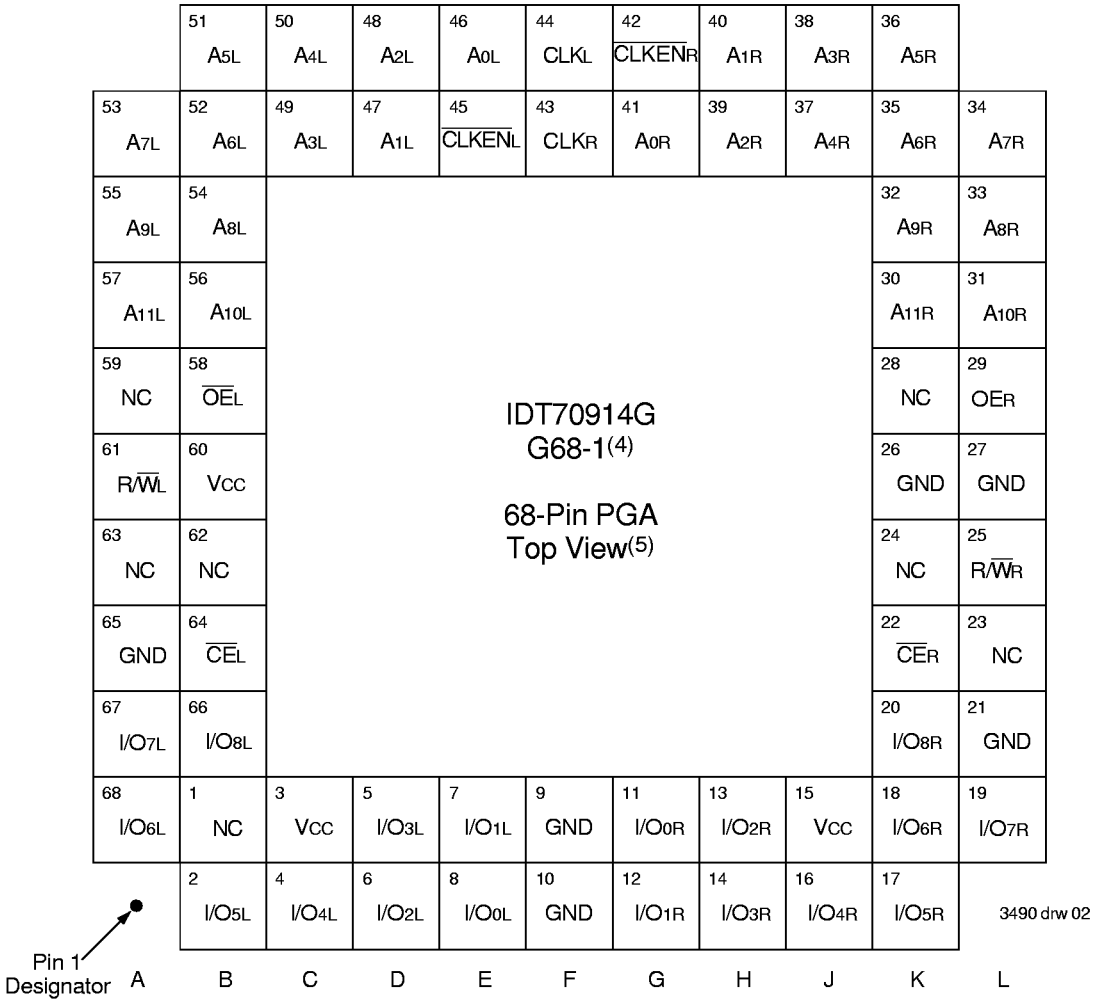
The IDT70914 is a high-speed 4K x 9 bit synchronous Dual-Port RAM. The memory array is based on Dual-Port memory cells to allow simultaneous access from both ports. Registers on control, data, and address inputs provide low set-up and hold times. The timing latitude provided by this approach allow systems to be designed with very short cycle times. With an input data register, this device has been optimized for applications having unidirectional data flow or bi-directional data flow in bursts.

The IDT70914 utilizes a 9-bit wide data path to allow for parity at the user's option. This feature is especially useful in data communication applications where it is necessary to use a parity bit for transmission/reception error checking.

Fabricated using IDT's CMOS high-performance technology, these Dual-Ports typically operate on only 850mW of power at maximum high-speed clock-to-data output times as fast as 12ns. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

The IDT70914 is packaged in a 68-pin PGA, 68-pin PLCC, and an 80-pin TQFP. Military grade product is manufactured in compliance with the latest revision of MIL-PRF-38535 QML, making it ideally suited for military temperature applications demanding the highest level of performance and reliability.

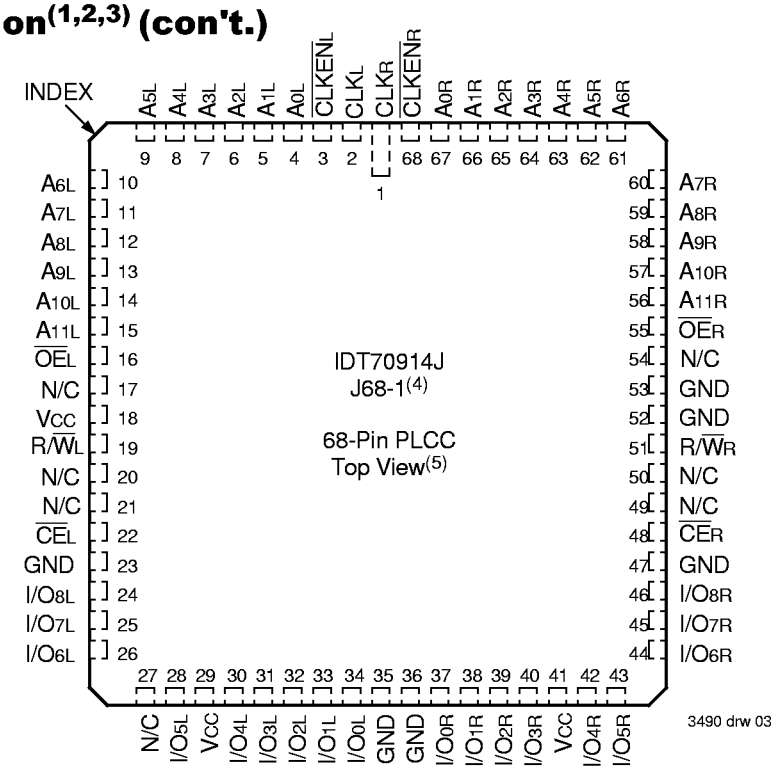
Pin Configurations[1,2,3]

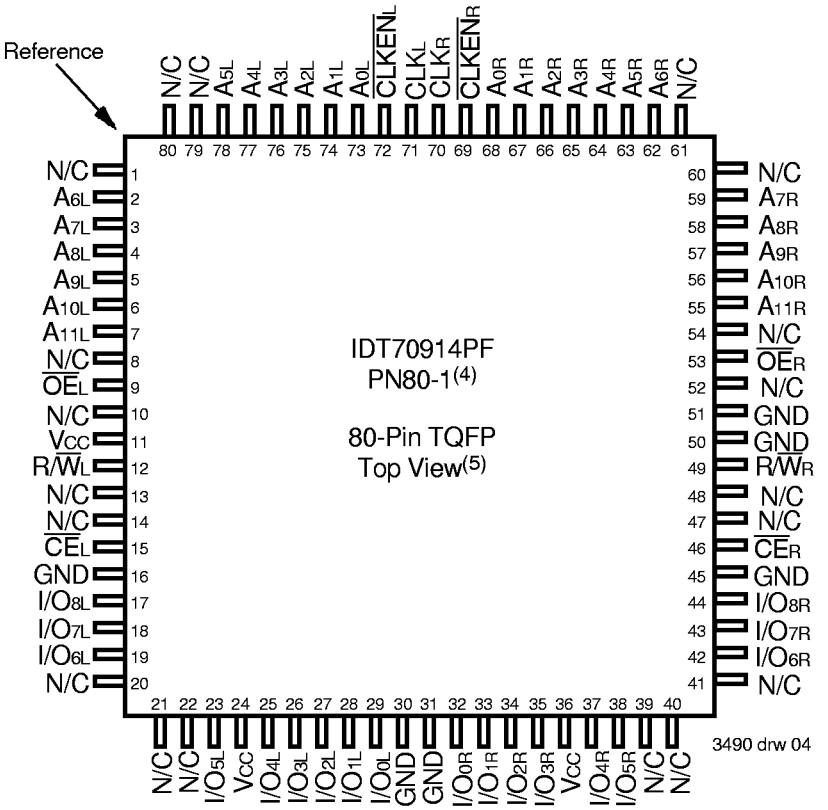


	A	B	C	D	E	F	G	H	J	K	L
		51 A5L	50 A4L	48 A2L	46 A0L	44 CLKL	42 $\overline{CLKEN}$R	40 A1R	38 A3R	36 A5R	
1	53 A7L	52 A6L	49 A3L	47 A1L	45 $\overline{CLKEN}$L	43 CLKR	41 A0R	39 A2R	37 A4R	35 A6R	34 A7R
2	55 A9L	54 A8L								32 A9R	33 A8R
3	57 A11L	56 A10L								30 A11R	31 A10R
4	59 NC	58 $\overline{OE}$L								28 NC	29 OER
5	61 R/$\overline{W}$L	60 VCC								26 GND	27 GND
6	63 NC	62 NC								24 NC	25 R/$\overline{W}$R
7	65 GND	64 $\overline{CE}$L								22 $\overline{CE}$R	23 NC
8	67 I/O7L	66 I/O8L								20 I/O8R	21 GND
9	68 I/O6L	1 NC	3 VCC	5 I/O3L	7 I/O1L	9 GND	11 I/O0R	13 I/O2R	15 VCC	18 I/O6R	19 I/O7R
		2 I/O5L	4 I/O4L	6 I/O2L	8 I/O0L	10 GND	12 I/O1R	14 I/O3R	16 I/O4R	17 I/O5R	

NOTES:
1. All Vcc pins must be connected to power supply.
2. All ground pins must be connected to ground supply.
3. Package body is approximately 1.18 in x 1.18 in x .16 in.
4. This package code is used to reference the package diagram.
5. This text does not indicate orientation of the actual part-marking.

Pin Configuration[1,2,3] (con't.)





NOTES:

1. All Vcc pins must be connected to power supply.
2. All ground pins must be connected to ground supply.
3. J68-1 package body is approximately .95 in x .95 in x .17 in.
   PN80-1 package body is approximately 14mm x 14mm x 1.4mm.
4. This package code is used to reference the package diagram.
5. This text does not indicate orientation of the actual part-marking.

Absolute Maximum Ratings(1)

Symbol	Rating	Commercial & Industrial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
V_{TERM}(2)	Terminal Voltage	-0.5 to V_{CC}	-0.5 to V_{CC}	V
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

3490 tbl 01

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed V_{CC} + 10% for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of $V_{TERM} \geq V_{CC}$ + 10%.

Capacitance

(T_A = +25°C, f = 1.0MHz) TQFP Only

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 3dV	9	pF

3490 tbl 04

NOTES:
1. These parameters are determined by device characterization, but are not production tested.
2. 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.

Maximum Operating Temperature and Supply Voltage(1,2)

Grade	Ambient Temperature	GND	V_{CC}
Military	-55°C to+125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%
Industrial	-40°C to +85°C	0V	5.0V ± 10%

3490 tbl 02

NOTES:
1. This is the parameter T_A.
2. Industrial temperature: for specific speeds, packages and powers contact your

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0(2)	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

3490 tbl 03

NOTES:
1. $V_{IL} \geq$ -1.5V for pulse width less than 10ns.
2. V_{TERM} must not exceed V_{CC} + 10%.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	70914S		Unit
			Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current(1)	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = +4mA	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	V

3490 tbl 05

NOTE:
1. At $V_{CC} \leq$ 2.0V, input leakages are undefined

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range[4,5] (V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Version	70914S12 Com'l Only		70914S15 Com'l Only		Unit
				Typ.[2]	Max.	Typ.[2]	Max.	
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}_L$ and $\overline{CE}_R$ = V_{IL}, Outputs Open f = f_{MAX}[1]	COM'L	190	310	180	300	mA
			MIL & IND	—	—	—	—	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R$ = V_{IH} f = f_{MAX}[1]	COM'L	95	150	90	140	mA
			MIL & IND	—	—	—	—	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_{"A"}$ = V_{IL} and $\overline{CE}_{"B"}$ = V_{IH}[3] Active Port Outputs Open, f=f_{MAX}[1]	COM'L	170	220	160	210	mA
			MIL & IND	—	—	—	—	
I_{SB3}	Full Standby Current (Both Ports - All CMOS Level Inputs)	Both Ports $\overline{CE}_R$ and $\overline{CE}_L$ ≥ V_{CC} - 0.2V V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V, f = 0[2]	COM'L	10	15	10	15	mA
			MIL & IND	—	—	—	—	
I_{SB4}	Full Standby Current (One Port - All CMOS Level Inputs)	$\overline{CE}_{"A"}$ ≤ 0.2V and $\overline{CE}_{"B"}$ ≥ V_{CC} - 0.2V[3] V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs Open f = f_{MAX}[1]	COM'L	165	210	155	200	mA
			MIL & IND	—	—	—	—	

3490 tbl 06a

Symbol	Parameter	Test Condition	Version	70914S20 Com'l & Military		70914S25 Military Only		Unit
				Typ.[2]	Max.	Typ.[2]	Max.	
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}_L$ and $\overline{CE}_R$ = V_{IL}, Outputs Open f = f_{MAX}[1]	COM'L	170	290	—	—	mA
			MIL & IND	170	310	160	290	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R$ = V_{IH} f = f_{MAX}[1]	COM'L	85	130	—	—	mA
			MIL & IND	85	140	80	130	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_{"A"}$ = V_{IL} and $\overline{CE}_{"B"}$ = V_{IH}[3] Active Port Outputs Open, f=f_{MAX}[1]	COM'L	150	200	—	—	mA
			MIL & IND	150	210	140	200	
I_{SB3}	Full Standby Current (Both Ports - All CMOS Level Inputs)	Both Ports $\overline{CE}_R$ and $\overline{CE}_L$ ≥ V_{CC} - 0.2V V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V, f = 0[2]	COM'L	10	15	—	—	mA
			MIL & IND	10	20	10	20	
I_{SB4}	Full Standby Current (One Port - All CMOS Level Inputs)	$\overline{CE}_{"A"}$ ≤ 0.2V and $\overline{CE}_{"B"}$ ≥ V_{CC} - 0.2V[3] V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs Open f = f_{MAX}[1]	COM'L	145	190	—	—	mA
			MIL & IND	145	200	135	190	

3490 tbl 06b

NOTES:

1. At f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of 1/t_{CYC}, using "AC TEST CONDITIONS" at input levels of GND to 3V.
2. f = 0 means no address, clock, or control lines change. Applies only to input at CMOS level standby.
3. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
4. V_{CC} = 5V, T_A = 25°C for Typ, and are not production tested. $I_{CC\,DC}$ = 150mA (Typ).
5. Industrial temperature: for specific speeds, packages and powers contact your sales office.

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1,2 and 3

3490 tbl 07

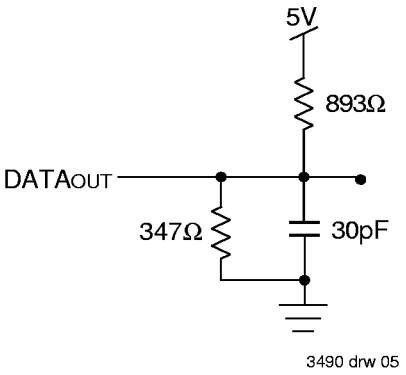


Figure 1. AC Output Test load.

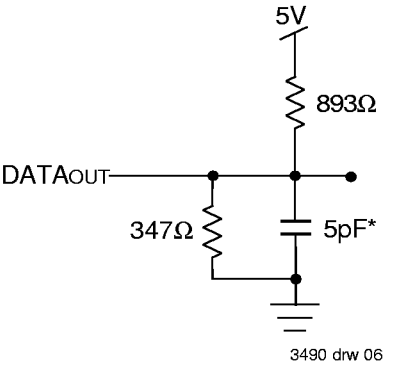


Figure 2. Output Test Load
(For t_{CKLZ}, t_{CKHZ}, t_{OLZ}, and t_{OHZ}).
*Including scope and jig.

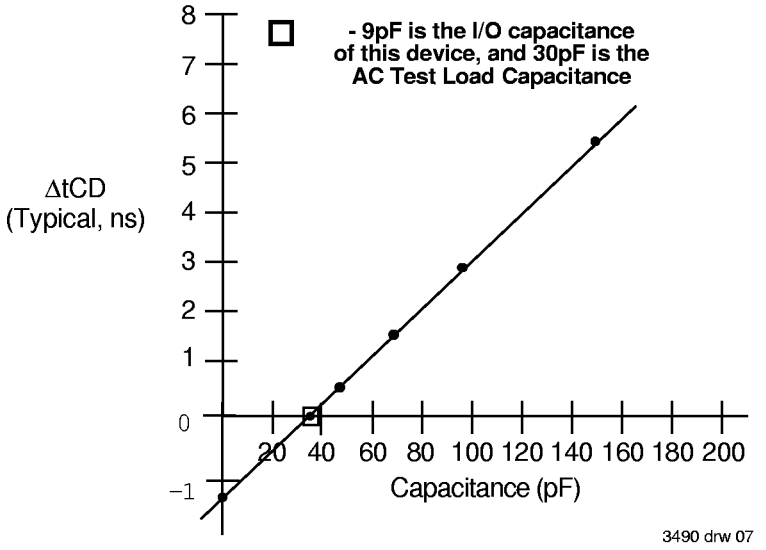


Figure 3. Typical Output Derating (Lumped Capacitive Load).

AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing)[3]

(Commercial: Vcc = 5V ± 10%, TA = 0°C to +70°C; Military: Vcc = 5V ± 10%, TA = -55°C to +125°C)

Symbol	Parameter	70914S12 Com'l Only		70914S15 Com'l Only		Unit
		Min.	Max.	Min.	Max.	
t_{CYC}	Clock Cycle Time	17	—	20	—	ns
t_{CH}	Clock High Time	6	—	6	—	ns
t_{CL}	Clock Low Time	6	—	6	—	ns
t_{CD}	Clock High to Output Valid	—	12	—	15	ns
t_S	Registered Signal Set-up Time	4	—	4	—	ns
t_H	Registered Signal Hold Time	1	—	1	—	ns
t_{DC}	Data Output Hold After Clock High	3	—	3	—	ns
t_{CKLZ}	Clock High to Output Low-Z[1,2]	2	—	2	—	ns
t_{CKHZ}	Clock High to Output High-Z[1,2]	—	7	—	7	ns
t_{OE}	Output Enable to Output Valid	—	7	—	8	ns
t_{OLZ}	Output Enable to Output Low-Z[1,2]	0	—	0	—	ns
t_{OHZ}	Output Disable to Output High-Z[1,2]	—	7	—	7	ns
t_{SCK}	Clock Enable, Disable Set-up Time	4	—	4	—	ns
t_{HCK}	Clock Enable, Disable Hold Time	2	—	2	—	ns
Port-to-Port Delay						
t_{CWDD}	Write Port Clock High to Read Data Delay	—	25	—	30	ns
t_{CSS}	Clock-to-Clock Setup Time	—	13	—	15	ns

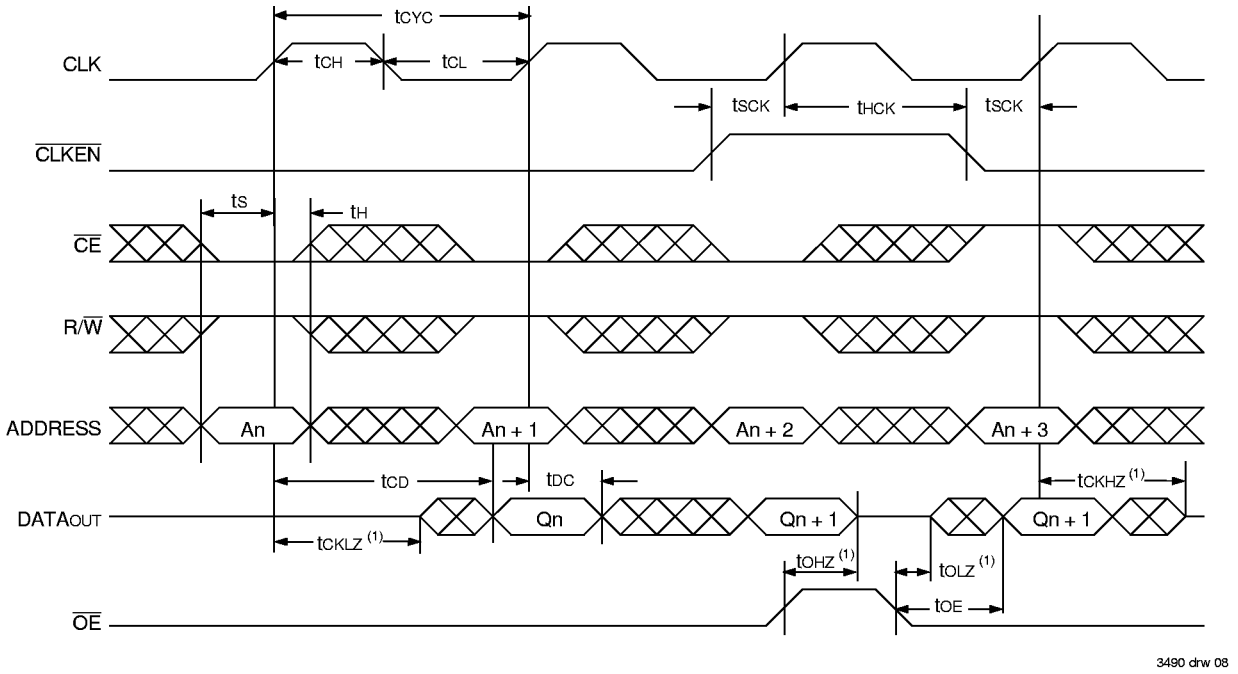
3490 tbl 08a

Symbol	Parameter	70914S20 Com'l & Military		70914S25 Military Only		Unit
		Min.	Max.	Min.	Max.	
t_{CYC}	Clock Cycle Time	20	—	25	—	ns
t_{CH}	Clock High Time	8	—	10	—	ns
t_{CL}	Clock Low Time	8	—	10	—	ns
t_{CD}	Clock High to Output Valid	—	20	—	25	ns
t_S	Registered Signal Set-up Time	5	—	6	—	ns
t_H	Registered Signal Hold Time	1	—	1	—	ns
t_{DC}	Data Output Hold After Clock High	3	—	3	—	ns
t_{CKLZ}	Clock High to Output Low-Z[1,2]	2	—	2	—	ns
t_{CKHZ}	Clock High to Output High-Z[1,2]	—	9	—	12	ns
t_{OE}	Output Enable to Output Valid	—	10	—	12	ns
t_{OLZ}	Output Enable to Output Low-Z[1,2]	0	—	0	—	ns
t_{OHZ}	Output Disable to Output High-Z[1,2]	—	9	—	11	ns
t_{SCK}	Clock Enable, Disable Set-up Time	5	—	6	—	ns
t_{HCK}	Clock Enable, Disable Hold Time	2	—	2	—	ns
Port-to-Port Delay						
t_{CWDD}	Write Port Clock High to Read Data Delay	—	35	—	45	ns
t_{CSS}	Clock-to-Clock Setup Time	—	15	—	20	ns

3490 tbl 08b

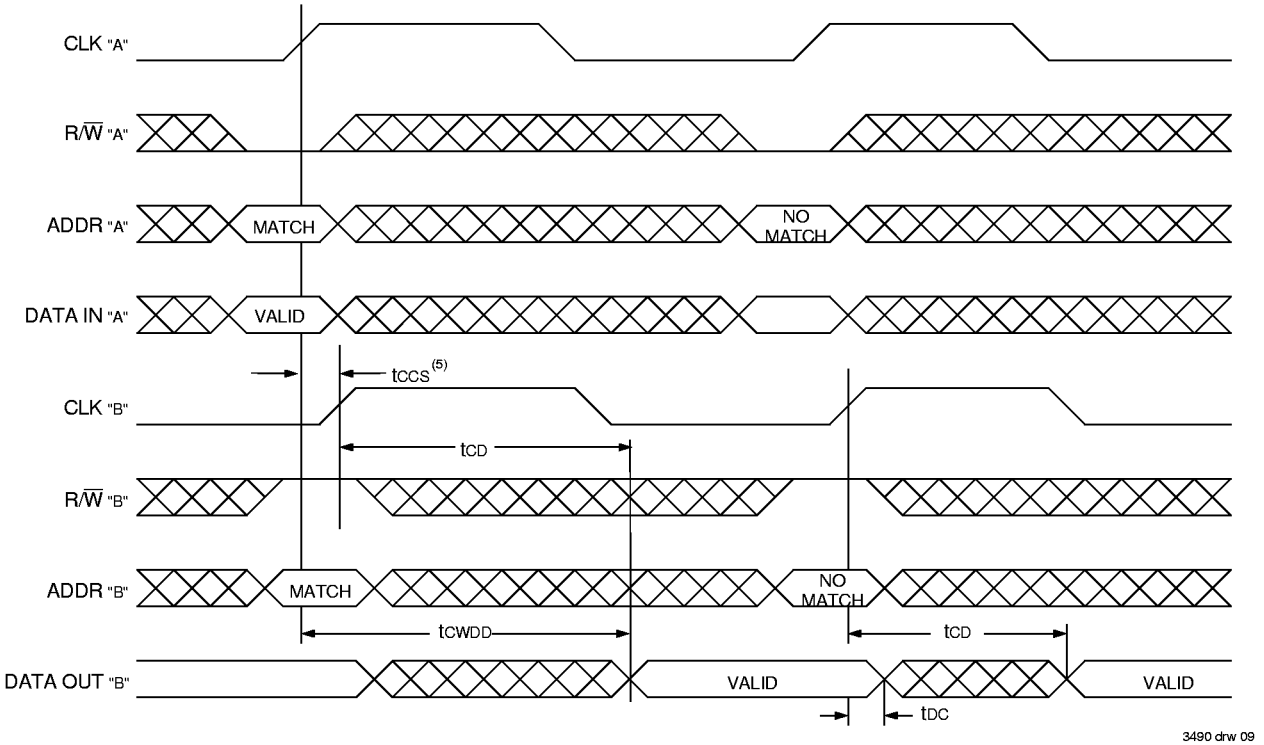
NOTES:
1. Transition is measured ±200mV from Low or High impedance voltage with the Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. Industrial temperature: for specific speeds, packages and powers contact your sales office.

Timing Waveform of Read Cycle, Either Side



3490 drw 08

Timing Waveform of Write with Port-to-Port Read(2,3,4)

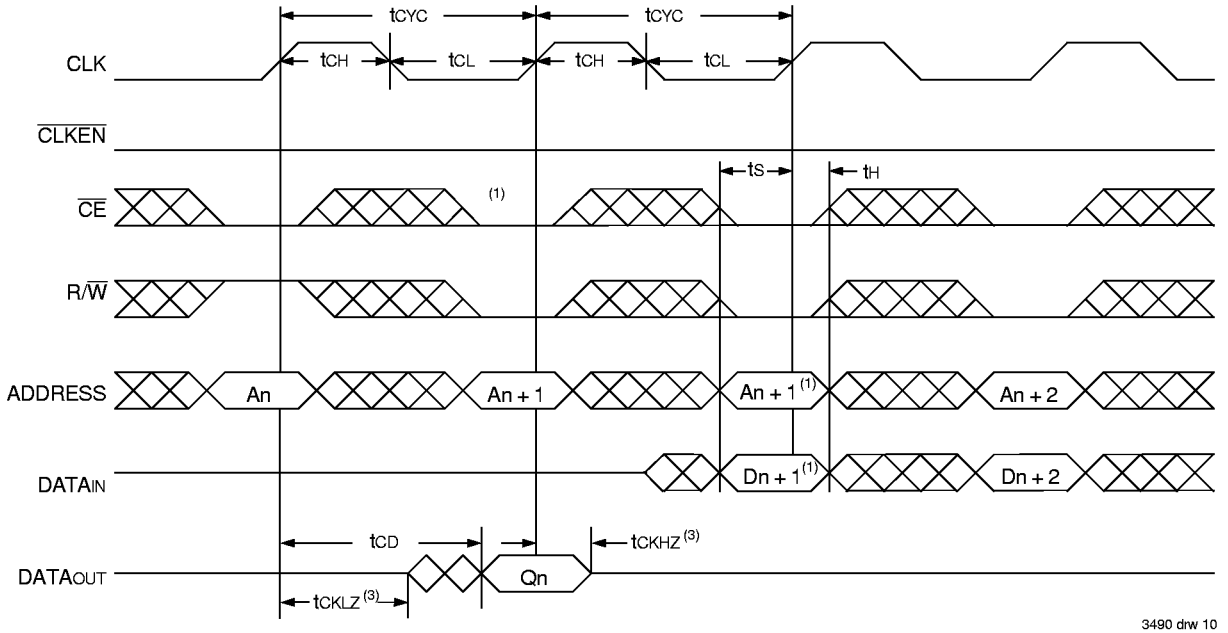


3490 drw 09

NOTES:

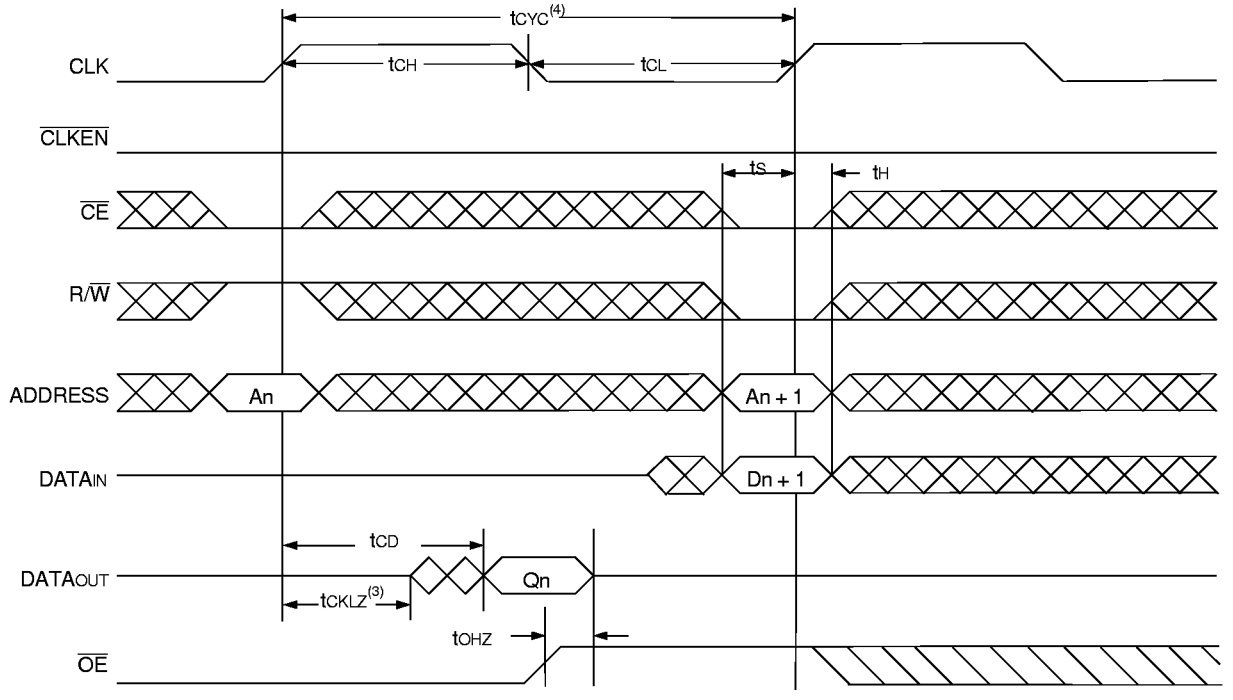
1. Transition is measured ±200mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. $\overline{CE}_L = \overline{CE}_R = V_{IL}$, $\overline{CLKEN}_L = \overline{CLKEN}_R = V_{IL}$.
3. $\overline{OE} = V_{IL}$ for the reading port, port 'B'.
4. All timing is the same for left and right ports. Ports "A" may be either the left or right port. Port "B" is opposite from port "A".
5. If $t_{CCS} \leq$ maximum specified, then data from right port READ is not valid until the maximum specified for t_{CWDD}.
   If t_{CCS} > maximum specified, then data from right port READ is not valid until $t_{CCS} + t_{CD}$. t_{CWDD} does not apply in this case.

Timing Waveform of Read-to-Write Cycle No. 1(1,2) (tCYC = min.)



3490 drw 10

Timing Waveform of Read-to-Write Cycle No. 2(4) (tCYC > min.)



3490 drw 11

NOTES:

1. For tCYC = min.; data out coincident with the rising edge of the subsequent write clock can occur. To ensure writing to the correct address location, the write must be repeated on the second write clock rising edge. If $\overline{CE}$ = VIL, invalid data will be written into array. The An+1 must be rewritten on the following cycle.
2. $\overline{OE}$ LOW throughout.
3. Transition is measured +/-200mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
4. For tCYC > min.; $\overline{OE}$ may be used to avoid data out coincident with the rising edge of the subsequent write clock. Use of $\overline{OE}$ will eliminate the need for the write to be repeated.

Functional Description

The IDT70914 provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide very short set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal. An asynchronous output enable is provided to ease asynchronous bus interfacing.

The internal write pulse width is dependent on the LOW to HIGH transitions of the clock signal allowing the shortest possible realized cycle times. Clock enable inputs are provided to stall the operation of the address and data input registers without introducing clock skew for very fast interleaved memory applications.

A HIGH on the $\overline{CE}$ input for one clock cycle will power down the internal circuitry to reduce static power consumption.

Truth Table I: Read/Write Control(1)

Inputs				Outputs	Mode
Synchronous(3)			Asynchronous		
CLK	$\overline{CE}$	R/$\overline{W}$	$\overline{OE}$	I/O0-8	
↑	H	X	X	High-Z	Deselected, Power-Down
↑	L	L	X	DATAIN	Selected and Write Enabled
↑	L	H	L	DATAOUT	Read Selected and Data Output Enable Read
↑	X	X	H	High-Z	Outputs Disabled

3490 tbl 09

Truth Table II: Clock Enable Function Table(1)

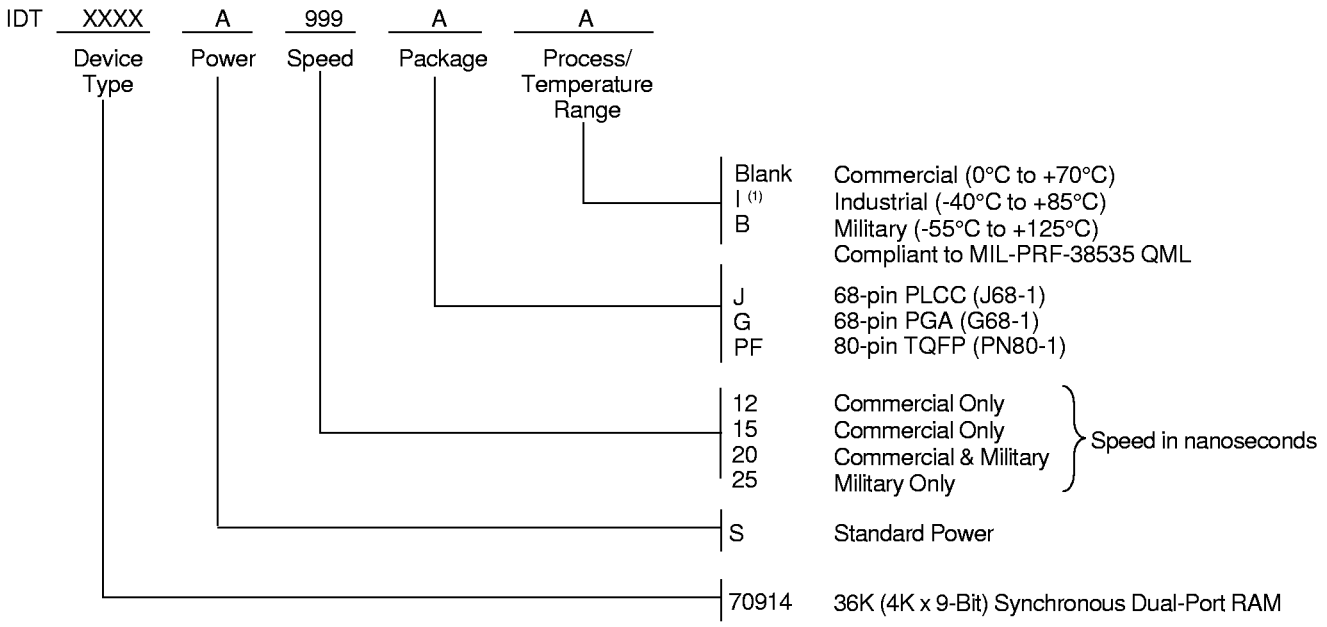
Mode	Inputs		Register Inputs		Register Outputs(4)	
	CLK(3)	$\overline{CLKEN}$(2)	ADDR	DATAIN	ADDR	DATAOUT
Load "1"	↑	L	H	H	H	H
Load "0"	↑	L	L	L	L	L
Hold (do nothing)	↑	H	X	X	NC	NC
	X	H	X	X	NC	NC

3490 tbl 10

NOTES:

1. 'H' = HIGH voltage level steady state, 'h' = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition, 'L' = LOW voltage level steady state 'l' = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition, 'X' = Don't care, 'NC' = No change
2. $\overline{CLKEN}$ = VIL must be clocked in during Power-Up.
3. Control signals are initialted and terminated on the rising edge of the CLK, depending on their input level. When R/$\overline{W}$ and $\overline{CE}$ are LOW, a write cycle is initiated on the LOW-to-HIGH transition of the CLK. Termination of a write cycle is done on the next LOW-to-HIGH transistion of the CLK.
4. The register outputs are internal signals from the register inputs being clocked in or disabled by $\overline{CLKEN}$.

Ordering Information



3490 drw 12

NOTE:
1. Industrial temperature range is available on selected TQFP packages in standard power. For specific speeds, packages and powers contact your sales office.

Datasheet Document History

3/10/99:	Initiated datasheet document history
	Converted to new format
	Cosmetic and typographical corrections
	Page 2 and 3 Added additional notes to pin configurations

CORPORATE HEADQUARTERS
2975 Stender Way
Santa Clara, CA 95054

for SALES:
800-345-7015 or 408-727-6116
fax: 408-492-8674
www.idt.com

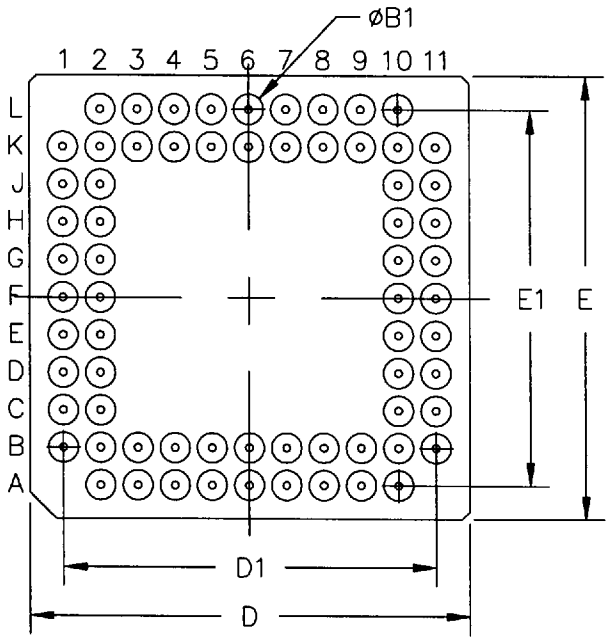
for Tech Support:
831-754-4613
DualPortHelp@idt.com

PACKAGE DIAGRAM OUTLINES

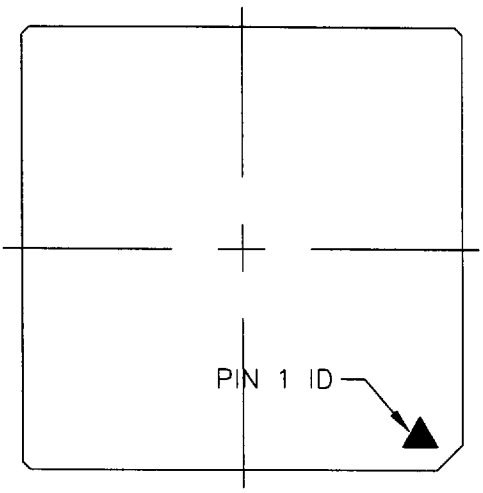
PIN GRID ARRAY

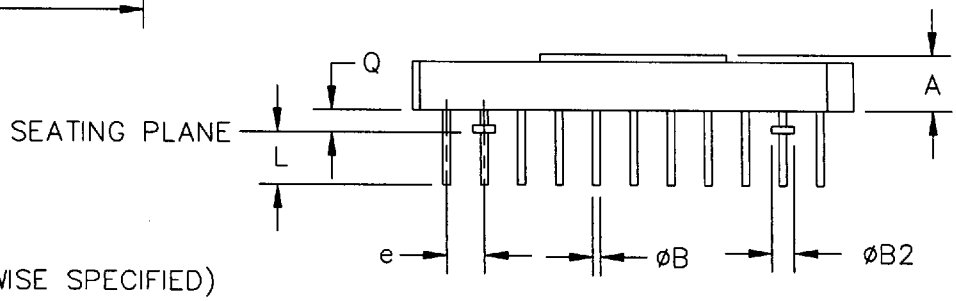
DCN	REV	DESCRIPTION	DATE	APPROVAL
17104	01	UPDATED TO STANDARDIZE DRAWING	12/21/89	S Thomas

BOTTOM VIEW



TOP VIEW





NOTES: (UNLESS OTHERWISE SPECIFIED)
1. ALL DIMENSIONS ARE IN INCHES.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "M" REPRESENTS THE PGA MATRIX SIZE.
4. SYMBOL "N" REPRESENTS THE NUMBER OF PINS.
5. CHAMFERRED CORNERS ARE IDT'S OPTION.

	CONFIGURATION	EXCEPTIONS
MIL–M–38510	LARGE OUTLINE P–AC	NONE
JEDEC	MO–067–AC	NONE

DWG #	G68–1	
SYMBOL	MIN	MAX
A	.070	.145
øB	.016	.020
øB1		.080
øB2	.040	.060
D/E	1.140	1.180
D1/E1	1.000 BSC	
e	.100 BSC	
L	.120	.140
M	11	
N	68	
Q	.040	.060

TOLERANCES UNLESS OTHERWISE SPECIFIED
FRAC ± – DEC ± – ANGLES ± –

APPROVALS	DATE
DRAWN AA	01/90
CHECKED	

Integrated Device Technology, Inc.
3236 Scott Blvd., Santa Clara, CA 95051
(408) 727–6116 FAX: (408) 727–2328

68 PIN PGA MKT DWG
(CAVITY UP)

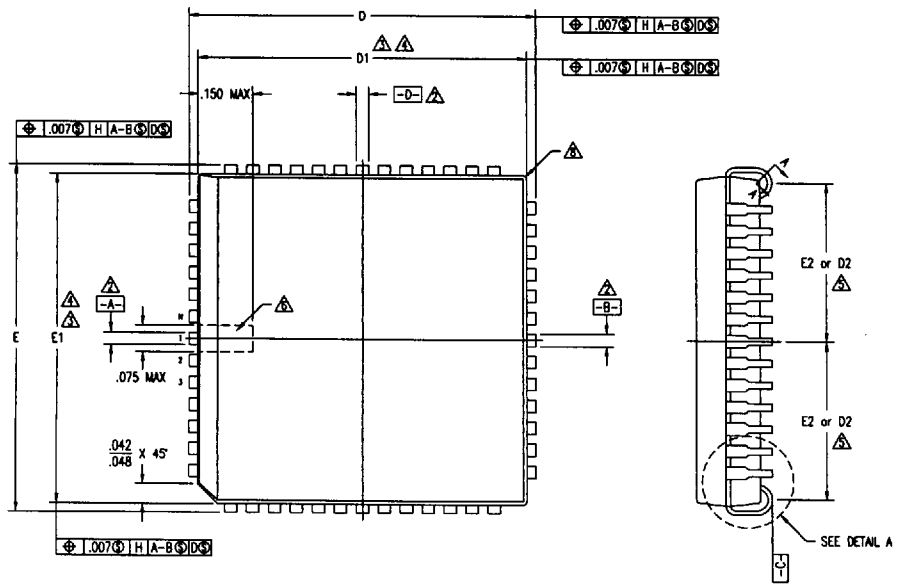
SCALE	SIZE	DRAWING NO.	REV
N/A	A	PSC–2075	01

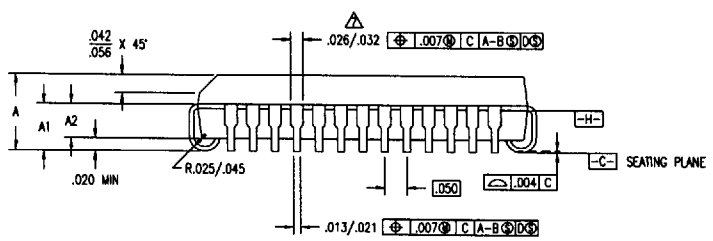
DO NOT SCALE DRAWING SHEET 46

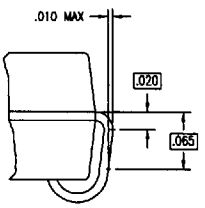
PACKAGE DIAGRAM OUTLINES

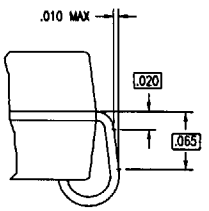
PLCC

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27647	06	REDRAW TO JEDEC FORMAT	03/15/95	

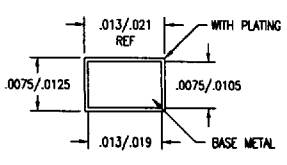








DETAIL A



SECTION A-A

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR XX± ± XXX± XXXX±		Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070	
APPROVALS	DATE	TITLE	PL PACKAGE OUTLINE SQUARE PLCC .050 PITCH
DRAWN dd	08/15/88		
CHECKED		SIZE C	DRAWING No. PSC-4008 REV 06
		DO NOT SCALE DRAWING	

PLCC (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27647	06	REDRAW TO JEDEC FORMAT	03/15/95	

DWG #	J28-1			
SYMBOL	JEDEC VARIATION AB			NOTE
	MIN	NOM	MAX	
A	.165	.172	.180	
A1	.095	.105	.115	
A2	.062	–	.083	
D	.485	.490	.495	
D1	.450	.453	.456	3,4
D2	.195	.205	.215	5
E	.485	.490	.495	
E1	.450	.453	.456	3,4
E2	.191	.205	.219	5
N	28			

DWG #	J44-1			
JEDEC VARIATION AC				NOTE
MIN	NOM	MAX		
.165	.172	.180		
.095	.105	.115		
.062	–	.083		
.685	.690	.695		
.650	.653	.656	3,4	
.295	.305	.315	5	
.685	.690	.695		
.650	.653	.656	3,4	
.291	.305	.319	5	
44				

DWG #	J52-1			
JEDEC VARIATION AD				NOTE
MIN	NOM	MAX		
.165	.172	.180		
.095	.105	.115		
.062	–	.083		
.785	.790	.795		
.750	.753	.756	3,4	
.345	.355	.365	5	
.785	.790	.795		
.750	.753	.756	3,4	
.341	.355	.369	5	
52				

DWG #	J68-1			
JEDEC VARIATION AE				NOTE
MIN	NOM	MAX		
.165	.172	.180		
.095	.105	.115		
.062	–	.083		
.985	.990	.995		
.950	.953	.956	3,4	
.445	.455	.465	5	
.985	.990	.995		
.950	.953	.956	3,4	
.441	.455	.469	5	
68				

DWG #	J84-1			
JEDEC VARIATION AF				NOTE
MIN	NOM	MAX		
.165	.172	.180		
.095	.105	.115		
.059	–	.080		
1.185	1.190	1.195		
1.150	1.154	1.156	3,4	
.545	.555	.565	5	
1.185	1.190	1.195		
1.150	1.154	1.156	3,4	
.541	.555	.569	5	
84				

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. DATUMS [A-B] AND [-D-] TO BE DETERMINED AT DATUM PLANE [-H-]
3. DIMENSIONS D1 AND E1 ARE TO BE DETERMINED AT DATUM PLANE [-H-]
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .010 PER SIDE. D1 AND E1 ARE BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH
5. DIMENSIONS D2 AND E2 ARE TO BE DETERMINED AT SEATING PLANE [-C-] CONTACT POINT
6. DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
7. LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .007 TOTAL MAXIMUM PER LEAD
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL
9. THESE DIMENSIONS DETERMINE THE MAXIMUM ANGLE OF THE LEAD FOR SOCKET APPLICATIONS
10. ALL DIMENSIONS ARE IN INCHES
11. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-018, VARIATION AB, AC, AD, AE & AF. EXCEPTIONS: JEDEC MAXIMUM BASE METAL LEAD WIDTH IS .018

TOLERANCES UNLESS SPECIFIED		
DECIMAL	ANGULAR	
XX±	±	
XXX±		
XXXX±		

Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA 95054
PHONE: (408) 727-6116
FAX: (408) 492-8674 TWX: 910-338-2070

APPROVALS	DATE
DRAWN AA	06/15/95
CHECKED	

TITLE: PL PACKAGE OUTLINE
SQUARE PLCC
.050 PITCH

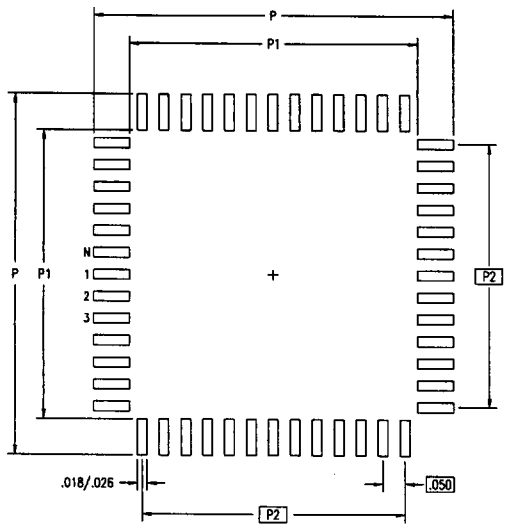
SIZE	DRAWING No.	REV
C	PSC-4008	06

DO NOT SCALE DRAWING

PLCC (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27647	08	REDRAW TO JEDEC FORMAT	03/15/95	

LAND PATTERN DIMENSIONS



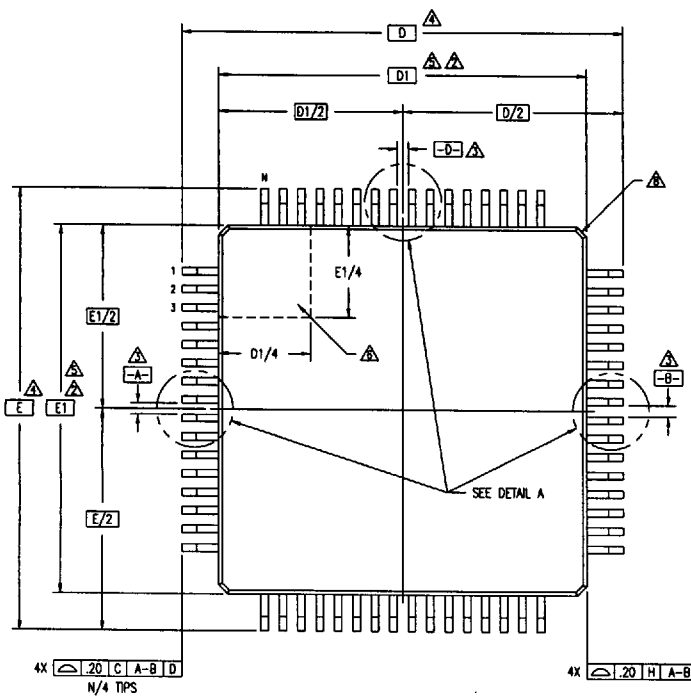
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
P	.520	.528	.720	.728	.820	.828	1.020	1.028	1.220	1.228
P1	.354	.362	.554	.562	.654	.662	.854	.862	1.054	1.062
P2	.300 BSC		.500 BSC		.600 BSC		.800 BSC		1.000 BSC	
N	28		44		52		68		84	

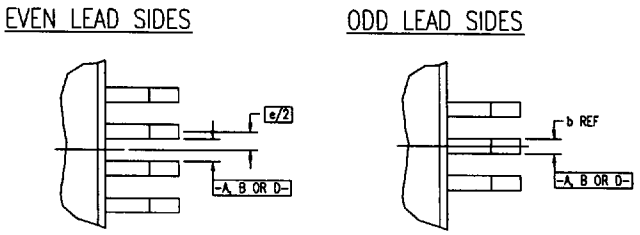
TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070
DECIMAL XX± XXX± XXXX±	ANGULAR ±	
APPROVALS	DATE	TITLE PL PACKAGE OUTLINE SQUARE PLCC .050 PITCH
DRAWN dd	08/15/89	
CHECKED		SIZE C DRAWING No. PSC-4008 REV 06
		DO NOT SCALE DRAWING

PACKAGE DIAGRAM OUTLINES

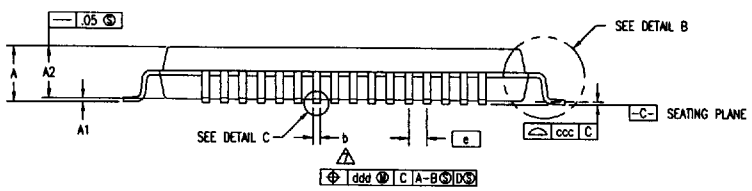
TQFP

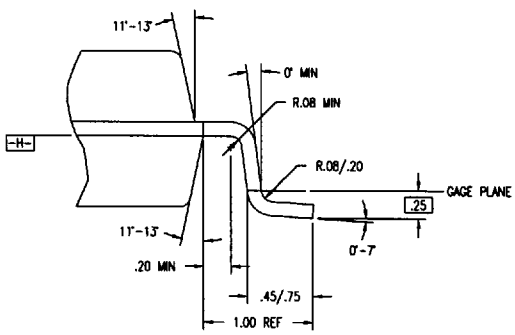
REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
22167	00	INITIAL RELEASE	03/12/92	T. VU
23823	01	ADD 80 & 100 LD	02/26/93	T. VU
24911	02	ADD 120 LD	10/06/93	T. VU
27384	03	REDRAW TO JEDEC FORMAT	12/10/94	



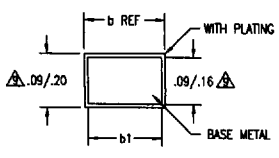


DETAIL A





DETAIL B



DETAIL C

TOLERANCES UNLESS SPECIFIED			Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070		
DECIMAL	ANGULAR				
XX±	±				
XXX±					
XXXX±					
APPROVALS	DATE		TITLE	PN PACKAGE OUTLINE 14.0 X 14.0 X 1.4 mm TQFP 1.00/.10 FORM	
DRAWN AA	03/12/92				
CHECKED			SIZE C	DRAWING No. PSC-4036	REV 03
			DO NOT SCALE DRAWING		

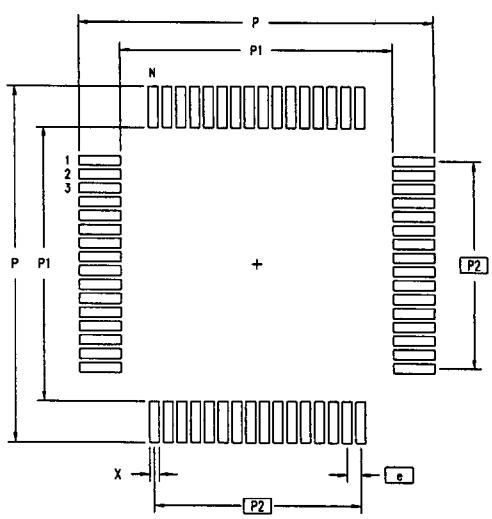
PACKAGE DIAGRAM OUTLINES

TQFP (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
22167	00	INITIAL RELEASE	03/12/92	T. VU
23823	01	ADD 80 & 100 LD	02/26/93	T. VU
24911	02	ADD 120 LD	10/06/93	T. VU
27384	03	REDRAW TO JEDEC FORMAT	11/18/94	

DWG #	PN64-1				PN80-1				PN100-1				PN120-1			
SYMBOL	JEDEC VARIATION BP			NOTE	JEDEC VARIATION BQ			NOTE	JEDEC VARIATION BR			NOTE	JEDEC VARIATION BS			NOTE
	MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX	
A	–	–	1.60		–	–	1.60		–	–	1.60		–	–	1.60	
A1	.05	.10	.15		.05	.10	.15		.05	.10	.15		.05	.10	.15	
A2	1.35	1.40	1.45		1.35	1.40	1.45		1.35	1.40	1.45		1.35	1.40	1.45	
D	16.00 BSC			4	16.00 BSC			4	16.00 BSC			4	16.00 BSC			4
D1	14.00 BSC			5,2	14.00 BSC			5,2	14.00 BSC			5,2	14.00 BSC			5,2
E	16.00 BSC			4	16.00 BSC			4	16.00 BSC			4	16.00 BSC			4
E1	14.00 BSC			5,2	14.00 BSC			5,2	14.00 BSC			5,2	14.00 BSC			5,2
N	64				80				100				120			
e	.80 BSC				.65 BSC				.50 BSC				.40 BSC			
b	.30	.37	.45	7	.22	.32	.38	7	.17	.22	.27	7	.13	.18	.23	7
b1	.30	.35	.40		.22	.30	.33		.17	.20	.23		.13	.16	.19	
ccc	–	–	.10		–	–	.10		–	–	.08		–	–	.08	
ddd	–	–	.20		–	–	.13		–	–	.08		–	–	.07	

LAND PATTERN DIMENSIONS



	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
P	16.80	17.00	16.80	17.00	16.80	17.00	16.80	17.00
P1	13.80	14.00	13.80	14.00	13.80	14.00	13.80	14.00
P2	12.00 BSC		12.35 BSC		12.00 BSC		11.60 BSC	
X	.40	.60	.30	.50	.30	.40	.20	.30
e	.80 BSC		.65 BSC		.50 BSC		.40 BSC	
N	64		80		100		120	

NOTES:

1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982

2 TOP PACKAGE MAY BE SMALLER THAN BOTTOM PACKAGE BY .15 mm

3 DATUMS A-B AND -D- TO BE DETERMINED AT DATUM PLANE -H-

4 DIMENSIONS D AND E ARE TO BE DETERMINED AT SEATING PLANE -C-

5 DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .25 mm PER SIDE. D1 AND E1 ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH

6 DETAILS OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED

7 DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

8 EXACT SHAPE OF EACH CORNER IS OPTIONAL

9 THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP

10 ALL DIMENSIONS ARE IN MILLIMETERS

11 THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-136, VARIATION BP, BQ, BR & BS

TOLERANCES UNLESS SPECIFIED	
DECIMAL	ANGULAR
XX±	±
XXX±	
XXXX±	

Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA 95054
PHONE: (408) 727-6116
FAX: (408) 492-8674 TWX: 910-338-2070

APPROVALS	DATE
DRAWN AA	03/12/92
CHECKED	

TITLE PN PACKAGE OUTLINE
14.0 X 14.0 X 1.4 mm TQFP
1.00/.10 FORM

SIZE	DRAWING No.	REV
C	PSC-4036	03

DO NOT SCALE DRAWING