



Integrated Device Technology, Inc.

CMOS STATIC RAM 256K (32K x 8-BIT)

IDT71256S
IDT71256L

T-46-23-13

FEATURES:

- High-speed address/chip select time
 - Military: 25/30/35/45/55/70/85/100/120/150ns (max.)
 - Commercial: 20/25/35/45ns (max.)
- Low-power operation
- Battery Backup operation — 2V data retention
- Produced with advanced high-performance CMOS technology
- Input and output directly TTL-compatible
- Available in standard 28-pin (600 mil) Cerdip, 28-pin (300 or 600 mil) plastic DIP, 28-pin (300 mil) ceramic sidebrazed DIP, 28-pin (330 mil) SOIC and (300 mil) SOJ, 28-pin CERPACK, 32-pin LCC or PLCC, 28-pin LCC
- Military product compliant to MIL-STD-883, Class B
- This function is listed as Standard Military Drawing #5962-88552 (L-Power) and #5962-88662 (S-Power)

DESCRIPTION:

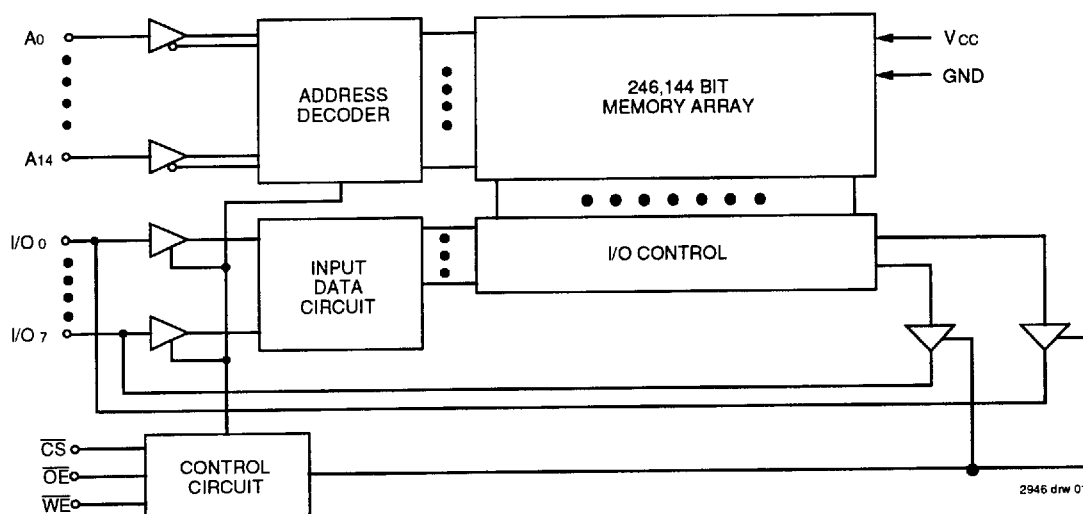
The IDT71256 is a 262,144-bit high-speed static RAM organized as 32K x 8. It is fabricated using IDT's high-performance, high-reliability CMOS technology.

Address access times as fast as 20ns are available with power consumption of only 350mW (typ.). The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes HIGH, the circuit will automatically go to, and remain in, a low-power standby mode as long as $\overline{CS}$ remains HIGH. In the full standby mode, the low-power device consumes less than 15 μ W, typically. This capability provides significant system level power and cooling savings. The low-power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 5 μ W when operating off a 2V battery.

The IDT71256 is packaged in a 28-pin (330 mil) gull-wing or 300 mil J-bend SOIC, a 28-pin 600 mil Cerdip, 28-pin (300 or 600 mil) plastic DIP, 28-pin (300 mil) ceramic sidebrazed DIP, 28-pin CERPACK, 32-pin LCC or PLCC, 28-pin LCC, providing high board-level packing densities.

The IDT71256 military RAM is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

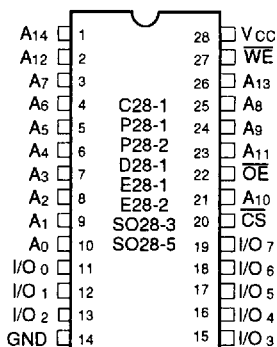
FUNCTIONAL BLOCK DIAGRAM



The IDT logo is a registered trademark of Integrated Device Technology, Inc.

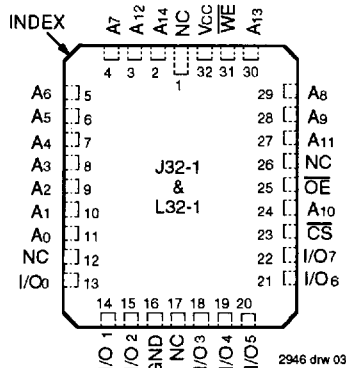
MILITARY AND COMMERCIAL TEMPERATURE RANGES
SEPTEMBER 1992

PIN CONFIGURATIONS



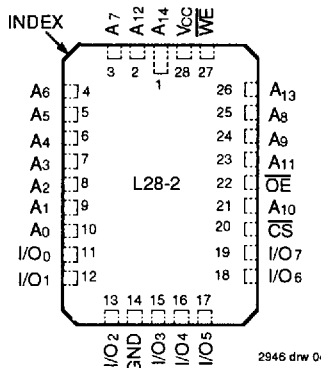
2946 drw 02

DIP/SOJ/SOIC TOP VIEW



2946 drw 03

32-Pin LCC/PLCC TOP VIEW



2946 drw 04

28-Pin LCC TOP VIEW

PIN DESCRIPTIONS

Name	Description
A0-A14	Addresses
I/O0-I/O7	Data Input/Output
CS	Chip Select
WE	Write Enable
OE	Output Enable
GND	Ground
VCC	Power

2946 tbl 01

TRUTH TABLE⁽¹⁾

WE	CS	OE	I/O	Function
X	H	X	High-Z	Standby (ISB)
X	V _{HC}	X	High-Z	Standby (ISB1)
H	L	H	High-Z	Output Disabled
H	L	L	DOUT	Read Data
L	L	X	DIN	Write Data

NOTE:

1. H = V_{HH}, L = V_{IL}, X = Don't Care

2946 tbl 02

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Com'l.	Mil.	Unit
V _{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T _A	Operating Temperature	0 to +70	-55 to +125	°C
T _{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T _{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P _T	Power Dissipation	1.0	1.0	W
I _{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2946 tbl 03

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	11	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	11	pF

NOTE:

1. This parameter is determined by device characterization, but is not production tested.

2946 tbl 04

RECOMMENDED OPERATING
TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	V _{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2946 tbi 05

RECOMMENDED DC OPERATING
CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V _{IH}	Input High Voltage	2.2	—	6.0	V
V _{IL}	Input Low Voltage	-0.5 ⁽¹⁾	—	0.8	V

NOTE:

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns, once per cycle.

2946 tbi 06

DC ELECTRICAL CHARACTERISTICS^(1, 2)(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	71256x20		71256x25		71256x30		71256x35		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I _{CC}	Dynamic Operating Current CS ≤ V _{IL} , Outputs Open V _{CC} = Max., f = f _{MAX} ⁽³⁾	S	155	—	145	150	—	145	135	140	mA
		L	135	—	115	130	—	125	105	120	
I _{SB}	Standby Power Supply Current (TTL Level) CS ≥ V _{IH} , V _{CC} = Max., Outputs Open, f = f _{MAX} ⁽³⁾	S	20	—	20	20	—	20	20	20	mA
		L	3	—	3	3	—	3	3	3	
I _{SB1}	Full Standby Power Supply Current (CMOS Level) CS ≥ V _{HC} , V _{CC} = Max., f = 0	S	15	—	15	20	—	20	15	20	mA
		L	0.4	—	0.4	1.5	—	1.5	0.4	1.5	

Symbol	Parameter	Power	71256x45		71256x55		71256x70		71256x85 ⁽⁵⁾		71256x100		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I _{CC}	Dynamic Operating Current CS ≤ V _{IL} , Outputs Open V _{CC} = Max., f = f _{MAX} ⁽³⁾	S	130	135	—	135	—	135	—	135	—	135	mA
		L	100	115	—	115	—	115	—	115	—	115	
I _{SB}	Standby Power Supply Current (TTL Level) CS ≥ V _{IH} , V _{CC} = Max., Outputs Open, f = f _{MAX} ⁽³⁾	S	20	20	—	20	—	20	—	20	—	20	mA
		L	3	3	—	3	—	3	—	3	—	3	
I _{SB1}	Full Standby Power Supply Current (CMOS Level) CS ≥ V _{HC} , V _{CC} = Max., f = 0	S	15	20	—	20	—	20	—	20	—	20	mA
		L	0.4	1.5	—	1.5	—	1.5	—	1.5	—	1.5	

NOTES:

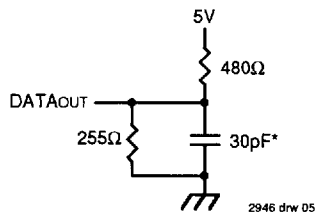
1. All values are maximum guaranteed values.
2. An "x" in part numbers indicates power rating (S or L).
3. f_{MAX} = 1/t_{RC}, all address inputs cycling at f_{MAX}; f = 0 means no address pins are cycling.
4. Standby current mode not available at 20ns.
5. Also available: 120 and 150 ns military devices.

2946 tbi 07

AC TEST CONDITIONS

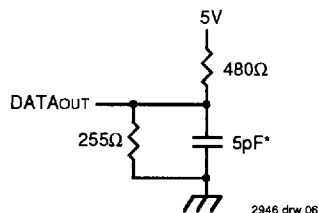
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2946 tbl 08



2946 drw 05

Figure 1. AC Test Load



2946 drw 06

Figure 2. AC Test Load
(for tCLZ, tOLZ, tCHZ, tOHZ, tLOW, tWHZ)

*Includes scope and jig capacitances

DC ELECTRICAL CHARACTERISTICS

VCC = 5.0V ± 10%

Symbol	Parameter	Test Condition		IDT71256S			IDT71256L			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
ILI	Input Leakage Current	VCC = Max., VIN = GND to VCC	MIL. COM'L.	— —	— —	10 5	— —	— —	5 2	μA
ILO	Output Leakage Current	VCC = Max., CS = VIH, VOUT = GND to VCC	MIL. COM'L.	— —	— —	10 5	— —	— —	5 2	μA
VOL	Output Low Voltage	IOL = 8mA, VCC = Min.			—	0.4	—	—	0.4	V
		IOL = 10mA, VCC = Min.		—	—	0.5	—	—	0.5	
VOH	Output High Voltage	IOH = -4mA, VCC = Min.		2.4	—	—	2.4	—	—	V

2946 tbl 09

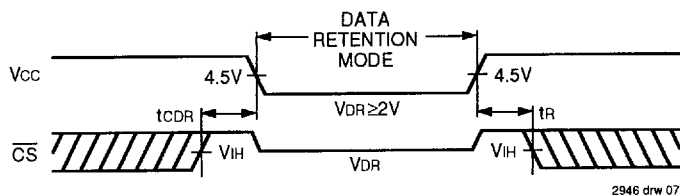
DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES(L Version Only) $V_{LC} = 0.2V$, $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	Test Condition	Min.	Typ. ⁽¹⁾ V _{CC} @		Max. V _{CC} @		Unit
				2.0V	3.0V	2.0V	3.0V	
V _{DR}	V _{CC} for Data Retention	—	2.0	—	—	—	—	V
I _{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$	MIL. COM'L.	—	—	500	800	μA
				—	—	120	200	
t _{CDR}	Chip Deselect to Data Retention Time		0	—	—	—	—	ns
t _R ⁽³⁾	Operation Recovery Time		t _{RC} ⁽²⁾	—	—	—	—	ns

NOTES:

1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed, but not tested.

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LOW V_{CC} DATA RETENTION WAVEFORM

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71256S20 ⁽¹⁾ 71256L20 ⁽¹⁾		71256S25 71256L25		71256S30 ⁽³⁾ 71256L30 ⁽³⁾		71256S35 71256L35		71256S45 71256L45		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
		Read Cycle										
tRC	Read Cycle Time	20	—	25	—	30	—	35	—	45	—	ns
tAA	Address Access Time	—	20	—	25	—	30	—	35	—	45	ns
tACS	Chip Select Access Time	—	20	—	25	—	30	—	35	—	45	ns
tCLZ ⁽²⁾	Chip Select to Output in Low-Z	5	—	5	—	5	—	5	—	5	—	ns
tCHZ ⁽²⁾	Chip Deselect to Output in High-Z	—	10	—	11	—	15	—	15	—	20	ns
tOE	Output Enable to Output Valid	—	10	—	11	—	13	—	15	—	20	ns
tOLZ ⁽²⁾	Output Enable to Output in Low-Z	2	—	2	—	2	—	2	—	0	—	ns
tOHZ ⁽²⁾	Output Disable to Output in High-Z	2	8	2	10	2	12	2	15	—	20	ns
tOH	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns
Write Cycle												
tWC	Write Cycle Time	20	—	25	—	30	—	35	—	45	—	ns
tCW	Chip Select to End-of-Write	15	—	20	—	25	—	30	—	40	—	ns
tAW	Address Valid to End-of-Write	15	—	20	—	25	—	30	—	40	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	15	—	20	—	25	—	30	—	35	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tDW	Data to Write Time Overlap	11	—	13	—	14	—	15	—	20	—	ns
tWHZ ⁽²⁾	Write Enable to Output in High-Z	—	10	—	11	—	15	—	15	—	20	ns
tDH	Data Hold from Write Time	0	—	0	—	0	—	0	—	0	—	ns
tOW ⁽²⁾	Output Active from End-of-Write	5	—	5	—	5	—	5	—	5	—	ns

NOTES:

1. 0° to +70°C temperature range only.
2. This parameter guaranteed by device characterization, but is not production tested.
3. -55° to +125°C temperature range only.

2968 tbl 11

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IDT71256 CMOS STATIC RAM 256K (32K x 8-BIT)

MILITARY AND COMMERCIAL TEMPERATURE RANGES

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0V \pm 10\%$, All Temperature Ranges)

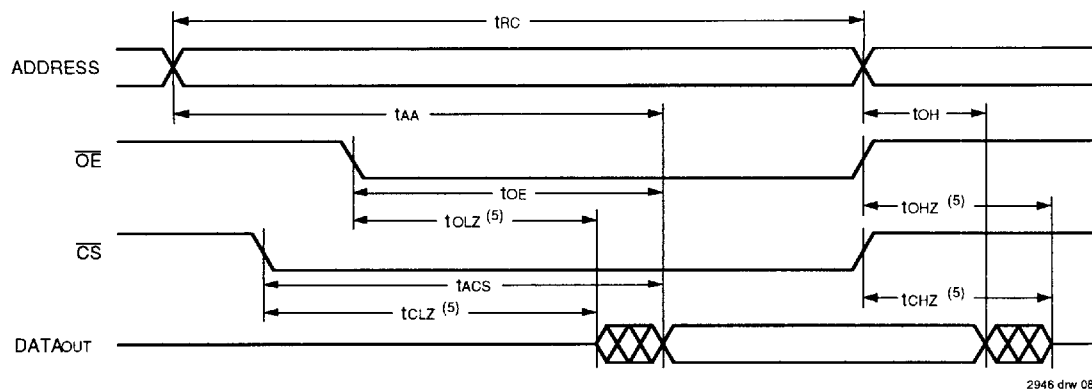
AC ELECTRICAL CHARACTERISTICS (V _{DD} = 5.0V ± 10%, All Temperatures)										
Symbol	Parameter	71256S55 ⁽¹⁾ 71256L55 ⁽¹⁾		71256S70 ⁽¹⁾ 71256L70 ⁽¹⁾		71256S85 ⁽¹⁾ 71256L85 ⁽¹⁾		71256S100 ^(1,2) 71256L100 ^(1,2)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t _{RC}	Read Cycle Time	55	—	70	—	85	—	100	—	ns
t _{AA}	Address Access Time	—	55	—	70	—	85	—	100	ns
t _{ACS}	Chip Select Access Time	—	55	—	70	—	85	—	100	ns
t _{CLZ} ⁽²⁾	Chip Deselect to Output in Low-Z	5	—	5	—	5	—	5	—	ns
t _{CHZ} ⁽²⁾	Output Enable to Output in Low-Z	—	25	—	30	—	35	—	40	ns
t _{OE}	Output Enable to Output Valid	—	25	—	30	—	35	—	40	ns
t _{OLZ} ⁽²⁾	Output Enable to Output in Low-Z	0	—	0	—	0	—	0	—	ns
t _{OHZ} ⁽²⁾	Output Disable to Output in High-Z	0	25	0	30	—	35	—	40	ns
t _{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
Write Cycle										
t _{WC}	Write Cycle Time	55	—	70	—	85	—	100	—	ns
t _{CW}	Chip Select to End-of-Write	50	—	60	—	70	—	80	—	ns
t _{AW}	Address Valid to End-of-Write	50	—	60	—	70	—	80	—	ns
t _{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t _{WP}	Write Pulse Width	40	—	45	—	50	—	55	—	ns
t _{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t _{DW}	Data to Write Time Overlap	25	—	30	—	35	—	40	—	ns
t _{DH}	Data Hold from Write Time (WE)	0	—	0	—	0	—	0	—	ns
t _{WHZ} ⁽²⁾	Write Enable to Output in High-Z	—	25	—	30	—	35	—	40	ns
t _{OW} ⁽²⁾	Output Active from End-of-Write	5	—	5	—	5	—	5	—	ns

NOTES:

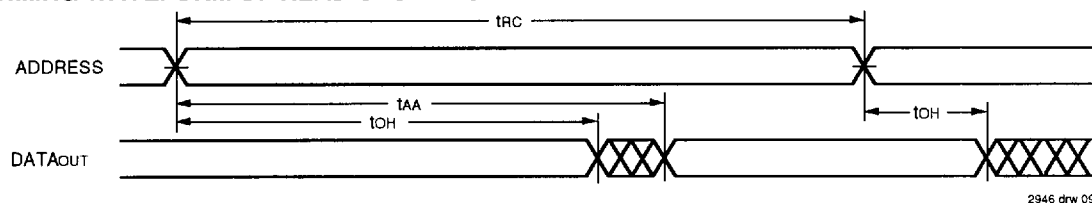
2968 tbl 11

1. -55°C to +125°C temperature range only.
2. This parameter guaranteed by device characterization, but is not production tested.
3. Also available: 120 and 150 ns military devices.

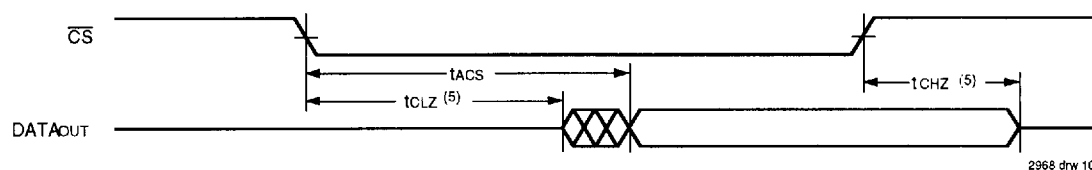
TIMING WAVEFORM OF READ CYCLE NO. 1⁽¹⁾



TIMING WAVEFORM OF READ CYCLE NO. 2^(1, 2, 4)

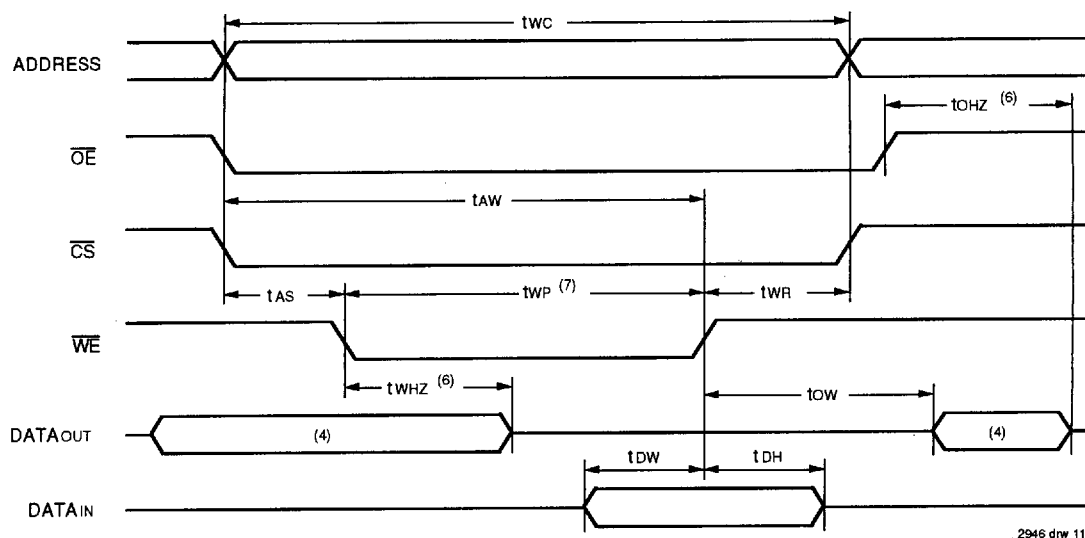


TIMING WAVEFORM OF READ CYCLE NO. 3^(1, 3, 4)

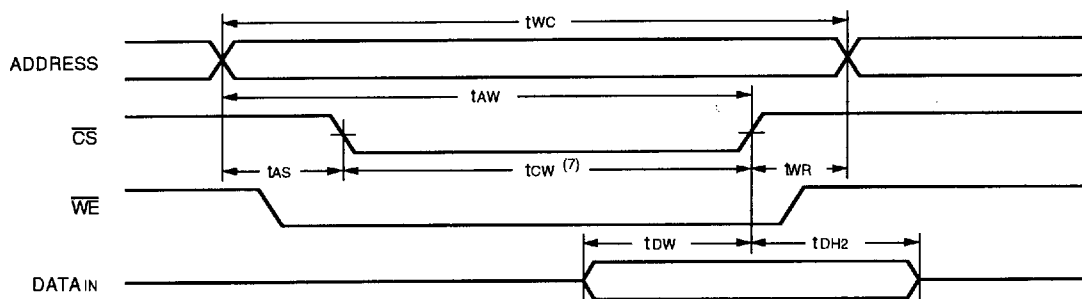


NOTES:

1. $\overline{WE}$ is HIGH for read cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
4. $\overline{OE} = V_{IL}$.
5. Transition is measured $\pm 200\text{mV}$ from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)^(1, 2, 3, 5, 7)

2946 drw 11

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)^(1, 2, 3, 5)

2946 drw 12

NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals must not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
6. Transition is measured $\pm 200\text{mV}$ from steady state.
7. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or $(t_{WHZ} + t_{OW})$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{OW} . If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP} . For a $\overline{CS}$ controlled write cycle, $\overline{OE}$ may be LOW with no degradation to t_{CW} .

ORDERING INFORMATION

IDT 71256	X	XXX	XX	X	
Device Type	Power	Speed	Package	Process/ Temperature Range	
				Blank	Commercial (0°C to +70°C)
				B	Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B
				TC	300 mil SIDEBRAZE DIP (C28-1)
				TP	300 mil Plastic DIP (P28-2)
				Y	300 mil SOJ (SO28-5)
				PE	330 mil SOIC (SO28-3)
				P	600 mil Plastic DIP (P28-1)
				D	600 mil CERDIP (D28-1)
				J	Plastic Leaded Chip Carrier (J32-1)
				L28	Leadless Chip Carrier (28-pin) (L28-2)
				L32	Leadless Chip Carrier (32-pin) (L32-1)
				XE	Cerpack F11 (E28-2)
				E	Cerpack F11A (E28-1)
				20	Commercial Only
				25	
				30	Military Only
				35	
				45	
				55	Military Only
				70	Military Only
				85	Military Only
				100	Military Only
				120	Military Only
				150	Military Only
				Speed in Nanoseconds	
				S	Standard Power
				L	Low Power

2946 drw 13