



Integrated Device Technology, Inc.

CMOS STATIC RAM 256K (32K x 8-BIT) IN PE PACKAGES

IDT71256SA

FEATURES:

- 32K x 8 CMOS static RAM
- Equal access and cycle times
 - Commercial: 15/20/25/35/45/70ns
- One Chip Select plus one Output Enable pin
- Bidirectional data inputs and outputs directly TTL-compatible
- Low power consumption via chip deselect
- Available in 28-pin 330 mil Plastic SOIC.

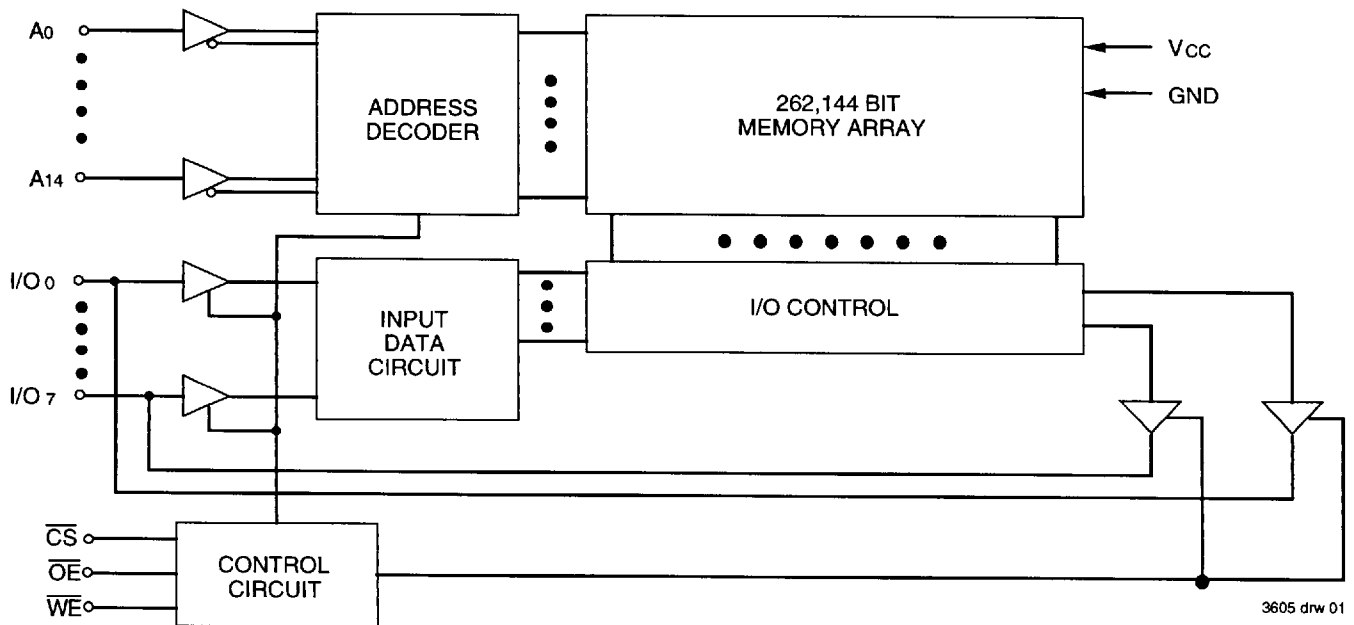
DESCRIPTION:

The IDT71256SA is a 262,144-bit Static RAM organized as 32K x 8. It is fabricated using IDT's high-performance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for your memory needs.

All bidirectional inputs and outputs of the IDT71256SA are TTL-compatible and operation is from a single 5V supply. Fully static asynchronous circuitry is used, requiring no clocks or refresh for operation.

The IDT71256SA is packaged in a 28-pin 330 mil Plastic SOIC.

FUNCTIONAL BLOCK DIAGRAM



The IDT logo is a registered trademark of Integrated Device Technology, Inc.

COMMERCIAL TEMPERATURE RANGE

JULY 1996

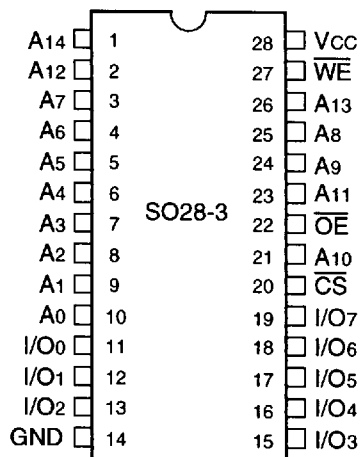
©1996 Integrated Device Technology, Inc.

3605/-

4825771 0022134 914

1-1

PIN CONFIGURATIONS



3605 drw 02

SOIC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Com'l.	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	-55 to +125	°C
TSTG	Storage Temperature	-55 to +125	°C
PT	Power Dissipation	1.0	W
IOUT	DC Output Current	50	mA

NOTES:

3605 tbl 02

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- VTERM must not exceed VCC + 0.5V.

CAPACITANCE

(TA = +25°C, f = 1.0MHz, SOJ package)

Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 3dV	11	pF
CIO	I/O Capacitance	VOUT = 3dV	11	pF

NOTE:

3605 tbl 03

- This parameter is guaranteed by device characterization, but not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	VCC+0.5	V
VIL	Input Low Voltage	-0.5 ⁽¹⁾	—	0.8	V

NOTE:

3605 tbl 01

- VIL (min.) = -1.5V for pulse width less than 10ns, once per cycle.

TRUTH TABLE^(1,2)

CS	OE	WE	I/O	Function
L	L	H	DATAOUT	Read Data
L	X	L	DATAIN	Write Data
L	H	H	High-Z	Outputs Disabled
H	X	X	High-Z	Deselected — Standby (ISB)
VHC ⁽³⁾	X	X	High-Z	Deselected — Standby (ISB1)

NOTES:

3605 tbl 04

- H = VIH, L = VIL, x = Don't care.
- VLC = 0.2V, VHC = VCC - 0.2V.
- Other inputs ≥ VHC or ≤ VLC.

DC ELECTRICAL CHARACTERISTICS

VCC = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT71256SA		Unit
			Min.	Max.	
II _L	Input Leakage Current	VCC = Max., VIN = GND to VCC	—	5	μA
II _O	Output Leakage Current	VCC = Max., CS = VIH, VOUT = GND to VCC	—	5	μA
VOL	Output Low Voltage	IOL = 8mA, VCC = Min.	—	0.4	V
VOH	Output High Voltage	IOH = -4mA, VCC = Min.	2.4	—	V

3605 tbl 05

DC ELECTRICAL CHARACTERISTICS⁽¹⁾

(VCC = 5.0V ± 10%, VLC = 0.2V, VHC = VCC - 0.2V)

Symbol	Parameter	71256SA15	71256SA20	71256SA25	Unit
ICC	Dynamic Operating Current $\overline{CS} \leq V_{IL}$, Outputs Open, VCC = Max., f = fMAX ⁽²⁾	150	145	145	mA
ISB	Standby Power Supply Current (TTL Level) $\overline{CS} \geq V_{IH}$, Outputs Open, VCC = Max., f = fMAX ⁽²⁾	40	40	40	mA
ISB1	Standby Power Supply Current (CMOS Level) $\overline{CS} \geq V_{HC}$, Outputs Open, VCC = Max., f = 0 ⁽²⁾ VIN ≤ VLC or VIN ≥ VHC	15	15	15	mA

DC ELECTRICAL CHARACTERISTICS (CONTINUED)⁽¹⁾

(VCC = 5.0V ± 10%, VLC = 0.2V, VHC = VCC - 0.2V)

Symbol	Parameter	71256SA35	71256SA45	71256SA70	Unit
ICC	Dynamic Operating Current $\overline{CS} \leq V_{IL}$, Outputs Open, VCC = Max., f = fMAX ⁽²⁾	140	135	130	mA
ISB	Standby Power Supply Current (TTL Level) $\overline{CS} \geq V_{IH}$, Outputs Open, VCC = Max., f = fMAX ⁽²⁾	30	30	20	mA
ISB1	Standby Power Supply Current (CMOS Level) $\overline{CS} \geq V_{HC}$, Outputs Open, VCC = Max., f = 0 ⁽²⁾ VIN ≤ VLC or VIN ≥ VHC	15	15	15	mA

NOTES:

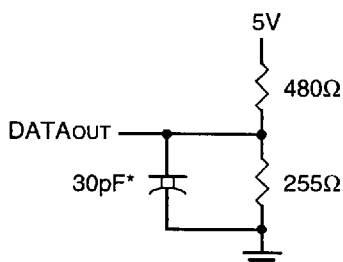
- All values are maximum guaranteed values.
- fMAX = 1/trc (all address inputs are cycling at fMAX); f = 0 means no address input lines are changing.

3605 tbl 06

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

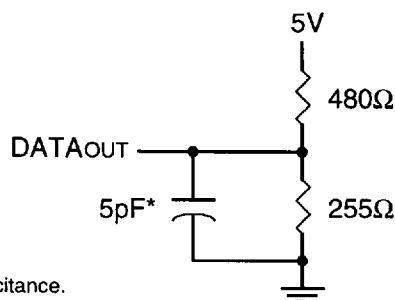
3605 tbl 07



3605 drw 03

*Including jig and scope capacitance.

Figure 1. AC Test Load



3605 drw 04

Figure 2. AC Test Load
(for tCLZ, tOLZ, tCHZ, tOHZ, tWZ, and tWHZ)

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	71256SA15		71256SA20		71256SA25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
tRC	Read Cycle Time	15	—	20	—	25	—	ns
tAA	Address Access Time	—	15	—	20	—	25	ns
tACS	Chip Select Access Time	—	15	—	20	—	25	ns
tCLZ ⁽¹⁾	Chip Select to Output in Low-Z	4	—	4	—	4	—	ns
tCHZ ⁽¹⁾	Chip Deselect to Output in High-Z	0	7	0	10	0	11	ns
tOE	Output Enable to Output Valid	—	7	—	10	—	11	ns
tOLZ ⁽¹⁾	Output Enable to Output in Low-Z	0	—	0	—	0	—	ns
tOHZ ⁽¹⁾	Output Disable to Output in High-Z	0	6	0	8	0	10	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	ns
tPU ⁽¹⁾	Chip Select to Power Up Time	0	—	0	—	0	—	ns
tPD ⁽¹⁾	Chip Deselect to Power Down Time	—	15	—	20	—	25	ns
Write Cycle								
tWC	Write Cycle Time	15	—	20	—	25	—	ns
tAW	Address Valid to End of Write	10	—	15	—	20	—	ns
tCW	Chip Select to End of Write	10	—	15	—	20	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWP	Write Pulse Width	10	—	15	—	20	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	7	—	11	—	13	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	ns
tOW ⁽¹⁾	Output Active from End of Write	4	—	4	—	4	—	ns
tWHZ ⁽¹⁾	Write Enable to Output in High-Z	0	6	0	10	0	11	ns

NOTE:

1. This parameter is guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.

3605 tbl 08

AC ELECTRICAL CHARACTERISTICS (CONTINUED) ($V_{CC} = 5.0V \pm 10\%$)

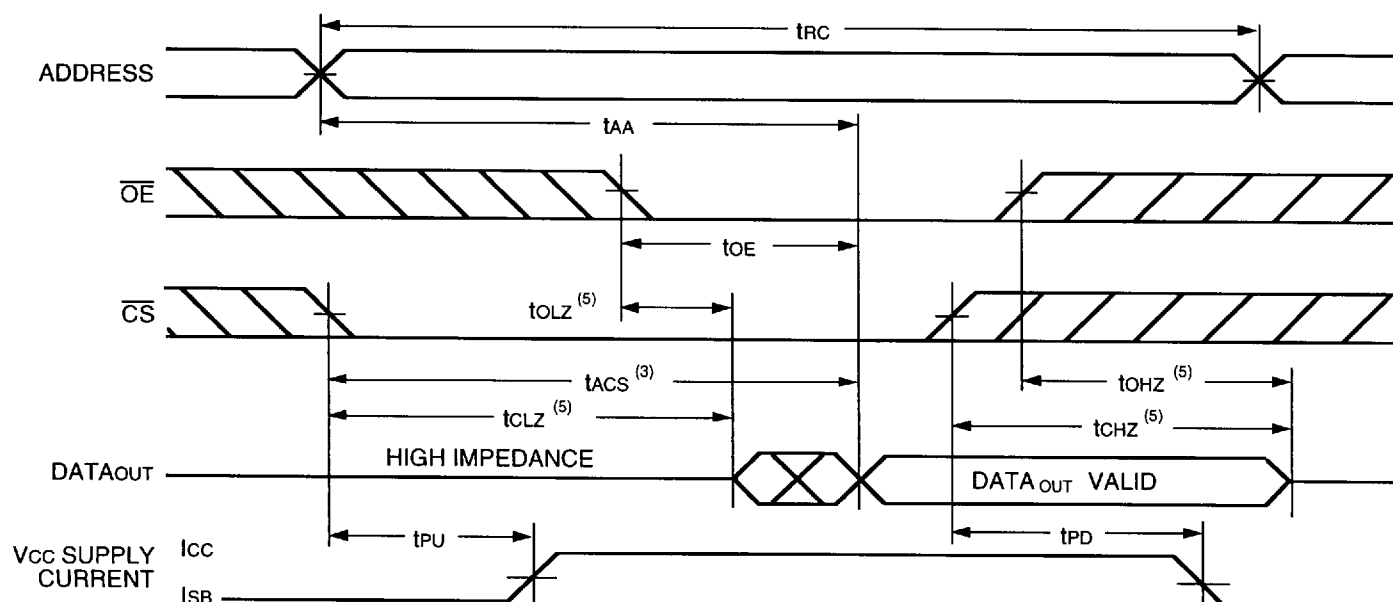
Symbol	Parameter	71256SA35		71256SA45		71256SA70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
tRC	Read Cycle Time	35	—	45	—	70	—	ns
tAA	Address Access Time	—	35	—	45	—	70	ns
tACS	Chip Select Access Time	—	35	—	45	—	70	ns
tCLZ ⁽¹⁾	Chip Select to Output in Low-Z	4	—	4	—	4	—	ns
tCHZ ⁽¹⁾	Chip Deselect to Output in High-Z	0	11	0	11	0	11	ns
tOE	Output Enable to Output Valid	—	11	—	11	—	11	ns
tOLZ ⁽¹⁾	Output Enable to Output in Low-Z	0	—	0	—	0	—	ns
tOHZ ⁽¹⁾	Output Disable to Output in High-Z	0	10	0	10	0	10	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	ns
tPU ⁽¹⁾	Chip Select to Power Up Time	0	—	0	—	0	—	ns
tPD ⁽¹⁾	Chip Deselect to Power Down Time	—	25	—	25	—	25	ns
Write Cycle								
tWC	Write Cycle Time	35	—	45	—	70	—	ns
tAW	Address Valid to End of Write	20	—	20	—	20	—	ns
tCW	Chip Select to End of Write	20	—	20	—	20	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWP	Write Pulse Width	20	—	20	—	20	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tdW	Data Valid to End of Write	13	—	13	—	13	—	ns
tdH	Data Hold Time	0	—	0	—	0	—	ns
tOW ⁽¹⁾	Output Active from End of Write	4	—	4	—	4	—	ns
tWHZ ⁽¹⁾	Write Enable to Output in High-Z	0	11	0	11	0	11	ns

NOTE:

1. This parameter is guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.

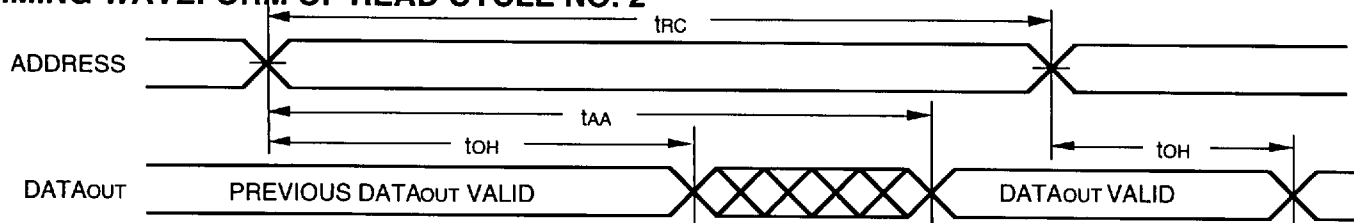
3605 tbi 08

TIMING WAVEFORM OF READ CYCLE NO. 1⁽¹⁾



3605 drw 05

TIMING WAVEFORM OF READ CYCLE NO. 2^(1,2,4)

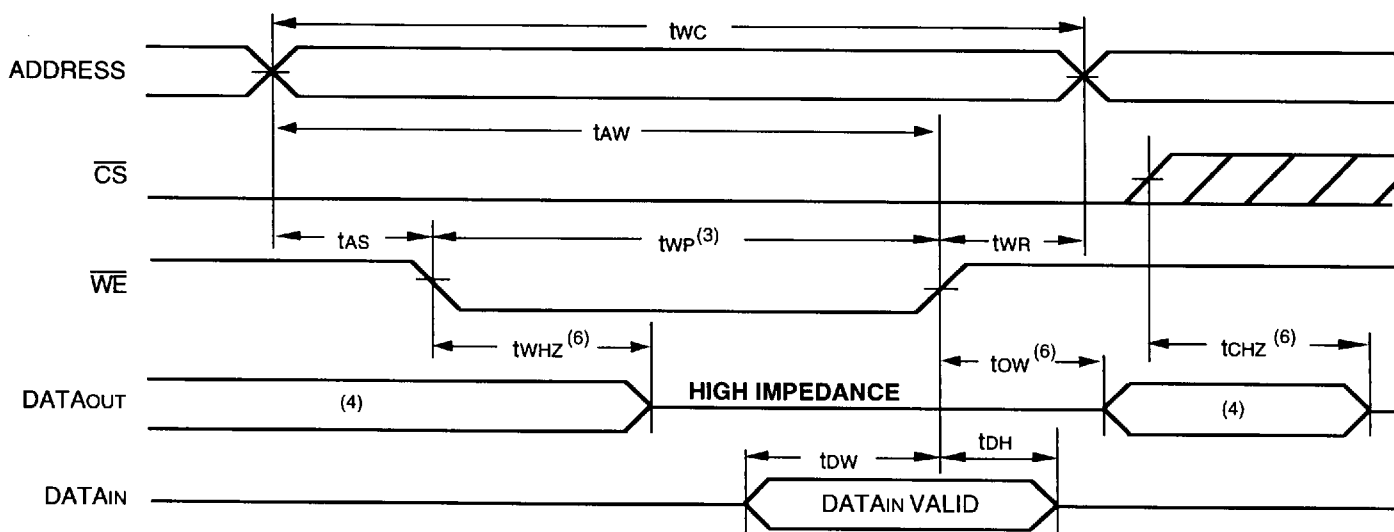


NOTES:

1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ is LOW.
3. Address must be valid prior to or coincident with the later of $\overline{CS}$ transition LOW; otherwise t_{AA} is the limiting parameter.
4. $\overline{OE}$ is LOW.
5. Transition is measured $\pm 200\text{mV}$ from steady state.

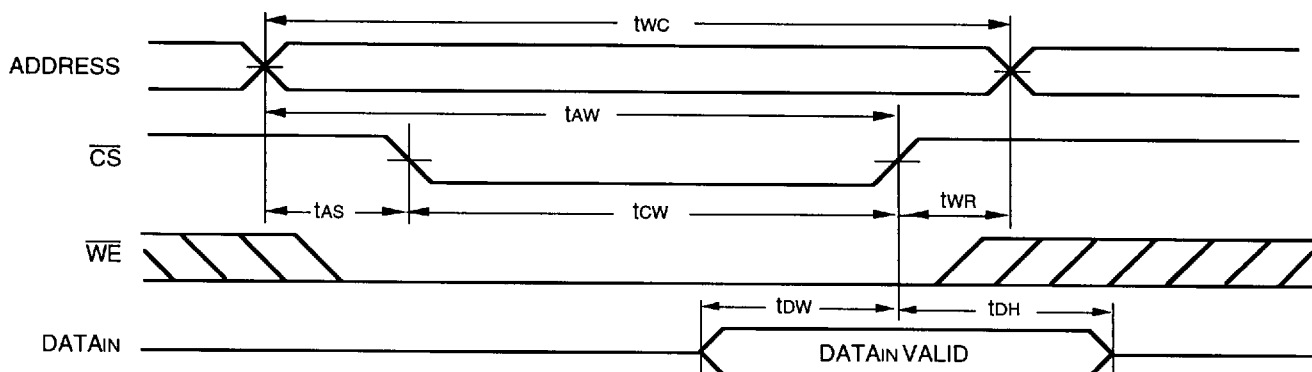
3605 drw 06

TIMING WAVEFORM OF WRITE CYCLE NO.1 ($\overline{WE}$ CONTROLLED TIMING)^(1,2,3,5)



3605 drw 07

TIMING WAVEFORM OF WRITE CYCLE NO.2 ($\overline{CS}$ CONTROLLED TIMING)^(1,2,5)

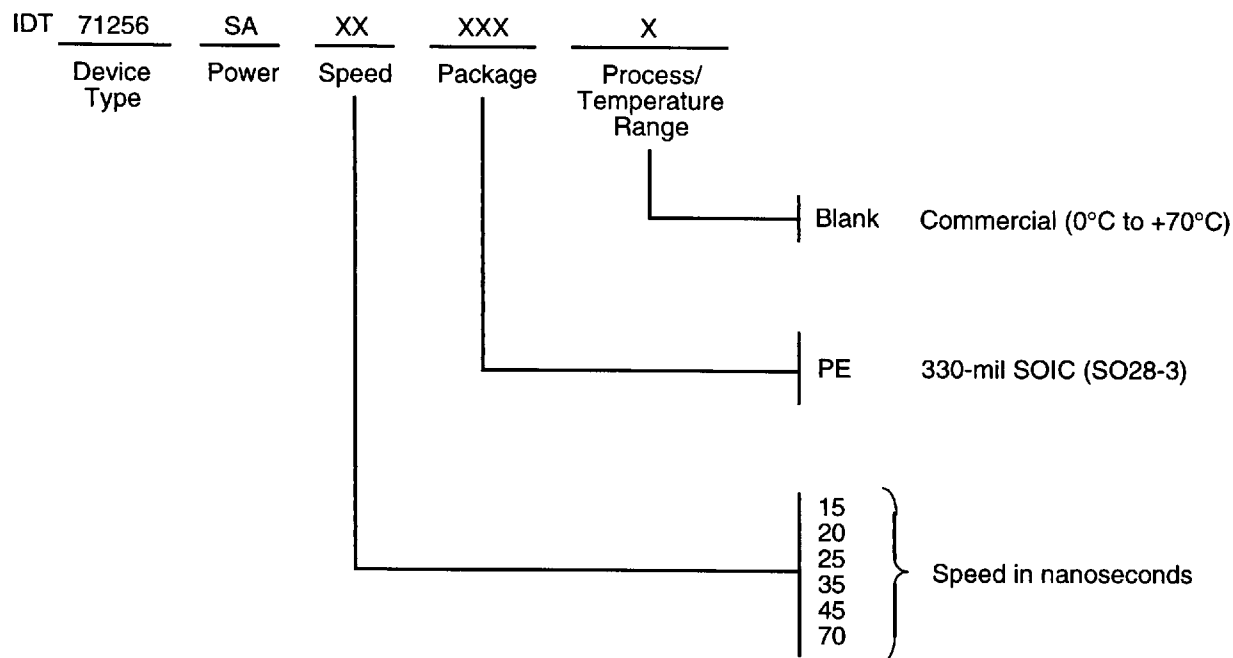


NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. $\overline{OE}$ is continuously HIGH. If during a $\overline{WE}$ controlled write cycle $\overline{OE}$ is LOW, t_{WP} must be greater than or equal to $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{OW} . If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is as short as the specified t_{WP} .
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
6. Transition is measured $\pm 200\text{mV}$ from steady state.

3605 drw 08

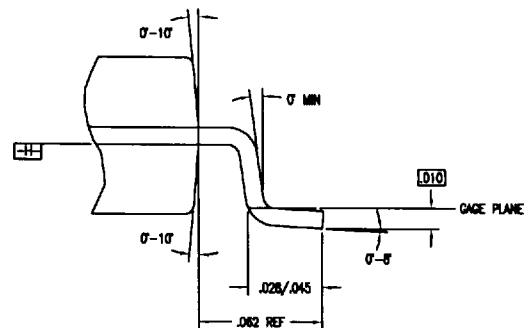
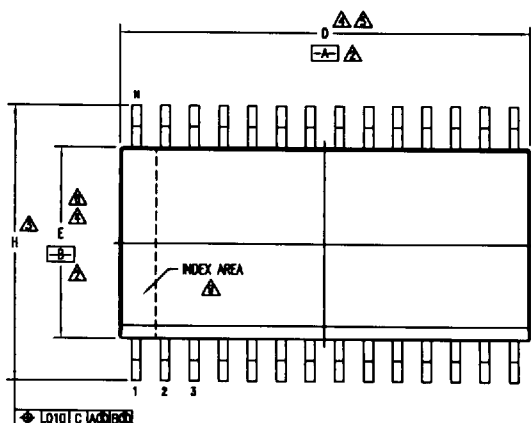
ORDERING INFORMATION



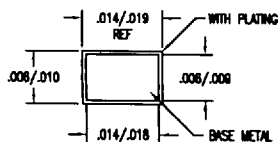
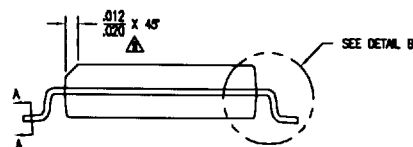
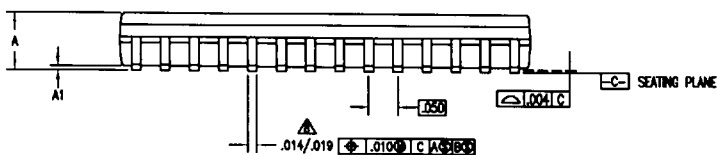
3605 drw 09

PACKAGE DIAGRAM OUTLINES
SOIC (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27842	03	REDRAW TO JEDEC FORMAT	03/15/98	



DETAIL B



SECTION A-A

TOLERANCES UNLESS SPECIFIED		INTEGRATED DEVICE TECHNOLOGY, INC.	
DECIMAL	ANGULAR	2878 Shafter Way, Santa Clara, CA 95054	
.XXX	±	PHONE: (408) 737-8116	
.XXXX		FAX: (408) 482-8874	
.XXXXX		TIRE: 810-338-2070	
APPROVALS	DATE	TITLE	
DESIGNED	07/19/98	PE PACKAGE OUTLINE	
CHECKED		.330" BODY WIDTH SOIC	
		.050" PITCH	
		SIZE	REV
		C	03
		PSC-4016	
		DO NOT SCALE DRAWING	

PACKAGE DIAGRAM OUTLINES
SOIC (Continued)

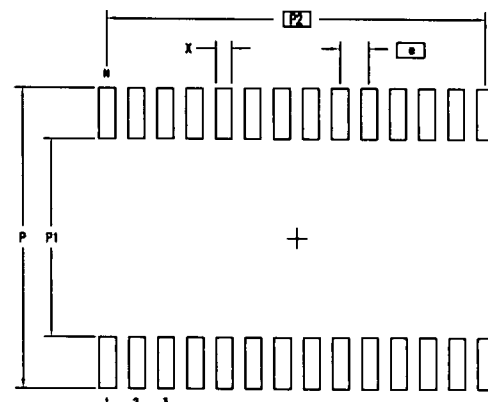
DWG #		S026-3		
SYMBOL	JEDEC VARIATION			NOTE
	AD			
	MIN	NOM	MAX	
A	.110	.115	.120	
A1	.005	.010	.014	
D	.718	.723	.728	4,5
E	.340	.345	.350	4,6
H	.462	.470	.478	3
N	28			

NOTES:

- ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
- DATUMS $\square$ -A- AND $\square$ -B- TO BE DETERMINED AT DATUM PLANE $\square$ -H-
- DIMENSION H TO BE DETERMINED AT SEATING PLANE $\square$ -C-
- DIMENSIONS D AND E ARE TO BE DETERMINED AT DATUM PLANE $\square$ -H-
- DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 PER SIDE
- DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 PER SIDE
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND .010 FROM LEAD TIP
- LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .004 IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT
- THE CHAMFER ON THE PACKAGE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE ZONE INDICATED
- ALL DIMENSIONS ARE IN INCHES
- THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-059, VARIATION AD. EXCEPTIONS: JEDEC MAXIMUM INTERLEAD FLASH OR PROTRUSIONS IS .006

KEYS0003B				
DCN	REV	DESCRIPTION	DATE	APPROVED
27842	03	REDRAW TO JEDEC FORMAT	03/15/95	

LAND PATTERN DIMENSIONS



	MIN	MAX
P	.512	.520
P1	.336	.344
P2	.650	BSC
X	.024	.032
e	.050	BSC
N	28	

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR X.XX ± X.XXX ± X.XXXX ±		Integrated Device Technology, Inc. 2878 Shafter Way, Santa Clara, CA 95054 PHONE (408) 727-6116 FAX (408) 458-8874 TWE 910-338-8870	
APPROVALS DRAWN JLD CHECKED	DATE 07/16/98	TITLE PE PACKAGE OUTLINE .330" BODY WIDTH SOIC .050" PITCH	
		SIZE C	REV 03
DO NOT SCALE DRAWING			