Integrated Device Technology, Inc.

VERY LOW POWER CMOS SRAM FOR NOTEBOOK/LAPTOP CACHE 256K (32K x 8-BIT)

IDT71256SL
IDT71256L

T-46-23-13

FEATURES:

- Optimized for 16/32bit notebook/laptop cache at 20 and 25MHz
- Very-low standby current (maximums):
  - — 3.0mA standby
  - — 0.4mA full standby (L)
  - — 1.0mA full standby (SL)
- Fast access times:
  - — 25/35ns
- Battery-backup operation: 2V data retention
  - — 120uA data retention current (max.)
- Small package for space-efficient layouts:
  - — 28-pin 300 mil SOJ
- Ideal configuration for large cache sizes, with minimum space and minimum power:
  - — 32K x 8
- Produced with advanced high-performance CMOS technology
- Static operation: no clocks or refresh required
- Input and output are TTL-compatible
- Single 5V(+/-10%) power supply

DESCRIPTION:

The IDT71256SL/L is a 262,144-bit high-speed static RAM organized as 32K x 8. It is fabricated using IDT's high-performance, high-reliability CMOS technology.

Both versions (SL and L) have outstanding low power characteristics, but differ slightly in dynamic and full standby currents, giving the designer flexibility to choose the one that fits his application better.

Address access times of 25, and 35ns are ideal for 16 and 32-bit notebook and laptop cache designs running at 20 and 25MHz. For instance, two of these SRAMs interface directly to many 386 notebook cache controllers to form a 64kB cache.

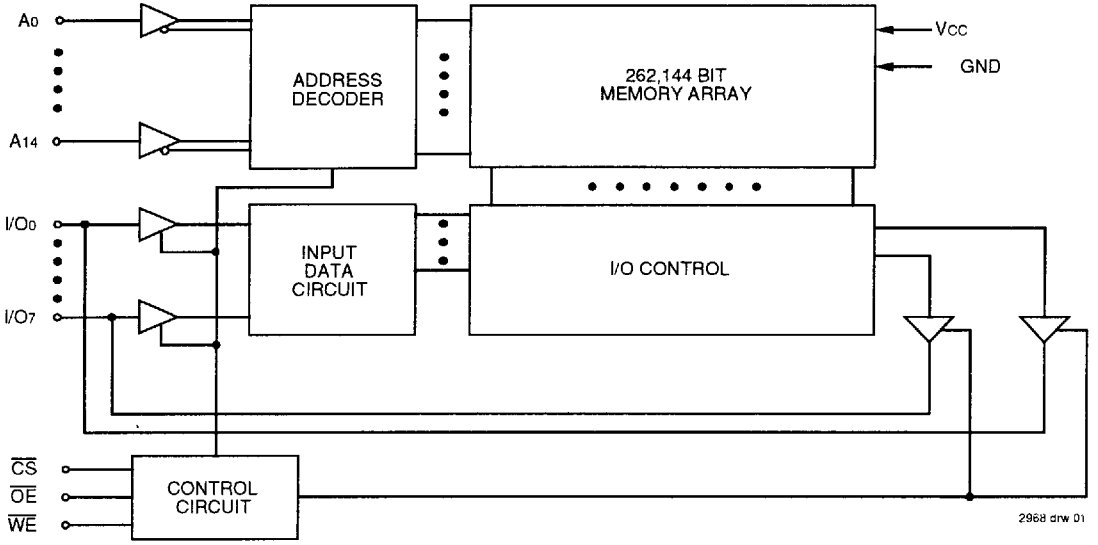
When the power management logic puts these SRAMs in standby mode, their very low power characteristics contribute to extended battery life.

When $\overline{CS}$ goes high, the SRAM will automatically go to a low power standby mode and will remain in standby as long as $\overline{CS}$ remains high. Furthermore, under full standby mode ($\overline{CS}$ at CMOS level, f=0), power consumption is guaranteed to always be less than 2mW (L version) and typically will be much smaller.

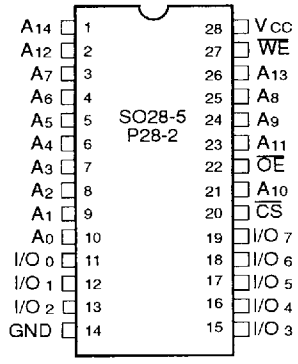
These SRAMs also offer battery-backup data retention at as little as 2 volts. Under this condition, power consumption is guaranteed not to exceed 0.6mW and typically will be much smaller.

The package chosen for this device, 28-pin 300mil SOJ, helps the designer attain the stringent space goals typical of notebook and laptop designs.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



2968 drw 02

SOJ/DIP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2968 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

PIN DESCRIPTIONS

Name	Description
A_0–A_{14}	Addresses
I/O_0–I/O_7	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
GND	Ground
V_{CC}	Power

2968 tbl 01

TRUTH TABLE(1)

$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	I/O	Function
X	H	X	High-Z	Standby (I_{SB})
X	V_{HC}	X	High-Z	Standby (I_{SB1})
H	L	H	High-Z	Output Disable
H	L	L	D_{OUT}	Read
L	L	X	D_{IN}	Write

NOTE: 2968 tbl 02

1. H = V_{IH}, L = V_{IL}, X = Don't Care

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	11	pF

NOTE: 2968 tbl 04

1. This parameter is determined by device characterization, but is not production tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

2968 tbl 05

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5	—	0.8	V

NOTE: 2968 tbl 06

1. V_{IL} (min.) = –3.0V for pulse width less than 20ns, once per cycle.

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DC ELECTRICAL CHARACTERISTICS(1, 2)

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	71256SL25 71256L25 Com'l.	71256SL35 71256L35 Com'l.	Unit
I_{CC}	Dynamic Operating Current, $\overline{CS} \leq V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}(2)	SL	120	110	mA
		L	115	105	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \geq V_{IH}$, V_{CC} = Max., Outputs Open, f = f_{MAX}(2)	SL	3	3	mA
		L	3	3	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \geq V_{HC}$, V_{CC} = Max., f = 0	SL	1	1	mA
		L	0.4	0.4	

NOTES:

2968 tbl 07

1. All values are maximum guaranteed values.
2. f_{MAX} = 1/t_{RC}, all address inputs cycling at f_{MAX}; f = 0 means that the address pins are not cycling.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2968 tbl 08

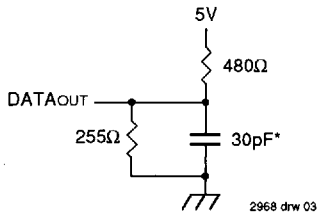


Figure 1. AC Test Load

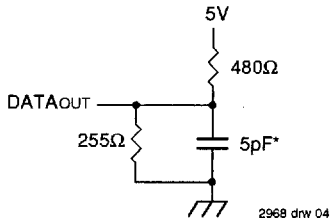


Figure 2. AC Test Load
(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, t_{WHZ})

*Includes scope and jig capacitances

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition		IDT71256SL Min.	IDT71256SL Typ.	IDT71256SL Max.	IDT71256L Min.	IDT71256L Typ.	IDT71256L Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	COM'L.	—	—	2	—	—	2	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	COM'L.	—	—	2	—	—	2	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.			—	0.4	—	—	0.4	V
		I_{OL} = 10mA, V_{CC} = Min.		—	—	0.5	—	—	0.5	
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.		2.4	—	—	2.4	—	—	V

2968 tbl 09

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

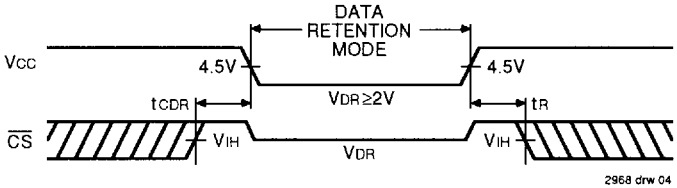
(L,SL Versions) V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V

Symbol	Parameter	Test Condition		Min.	Typ.(1) Vcc @ 2.0v	Typ.(1) Vcc @ 3.0V	Max. Vcc @ 2.0V	Max. Vcc @ 3.0V	Unit
V_{DR}	Vcc for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$	COM'L.	—	—	—	120	200	µA
t_{CDR}	Chip Deselect to Data Retention Time			0	—	—	—	—	ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	—	—	—	—	ns

NOTES:
2968 tbl 10

1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed, but not tested.

LOW Vcc DATA RETENTION WAVEFORM



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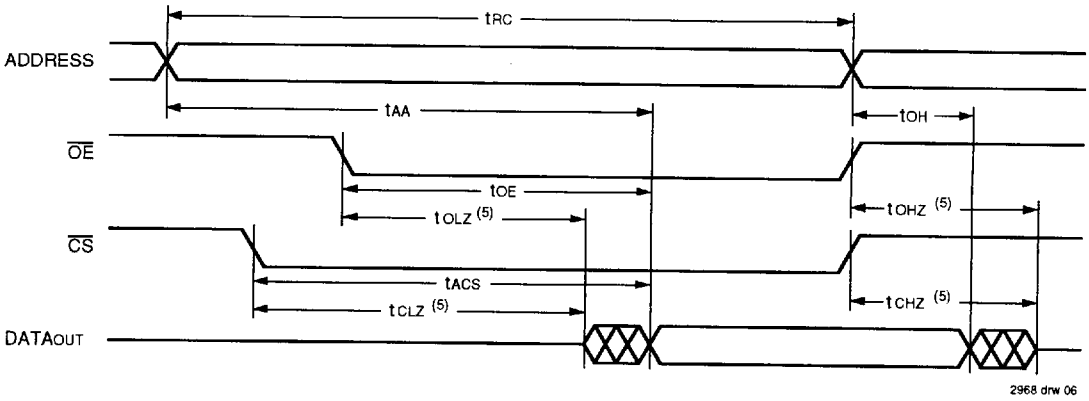
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71256SL25 71256L25		71256SL35 71256L35		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t_{RC}	Read Cycle Time	25	—	35	—	ns
t_{AA}	Address Access Time	—	25	—	35	ns
t_{ACS}	Chip Select Access Time	—	25	—	35	ns
t_{CLZ}	Chip Select to Output in Low Z[1]	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	11	—	15	ns
t_{OLZ}	Output Enable to Output in Low Z[1]	2	—	2	—	ns
t_{CHZ}	Chip Select to Output in High Z[1]	—	11	—	15	ns
t_{OHZ}	Output Disable to Output in High Z[1]	2	10	2	15	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	ns
Write Cycle						
t_{WC}	Write Cycle Time	25	—	35	—	ns
t_{CW}	Chip Select to End of Write	20	—	30	—	ns
t_{AW}	Address Valid to End of Write	20	—	30	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	ns
t_{WP}	Write Pulse Width	20	—	30	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	ns
t_{WHZ}	Write Enable to Output in High Z[1]	—	11	—	15	ns
t_{DW}	Data to Write Time Overlap	13	—	15	—	ns
t_{DH1}	Data Hold from Write Time ($\overline{WE}$)	0	—	0	—	ns
t_{DH2}	Data Hold from Write Time ($\overline{CS}$)	3	—	3	—	ns
t_{OW}	Output Active from End of Write[1]	5	—	5	—	ns

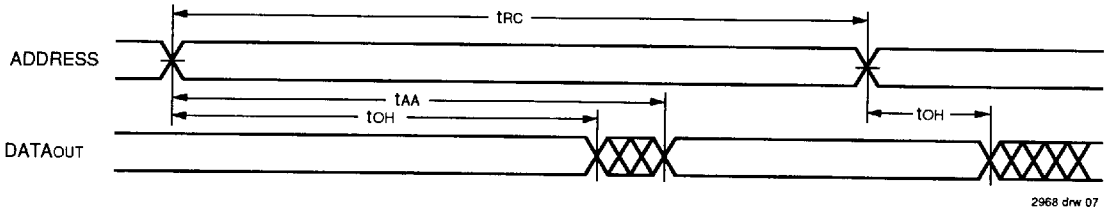
2968 tbl 11

NOTE:
1. This parameter guaranteed with the AC test load (Figure 2) by device characterization, but is not production tested.

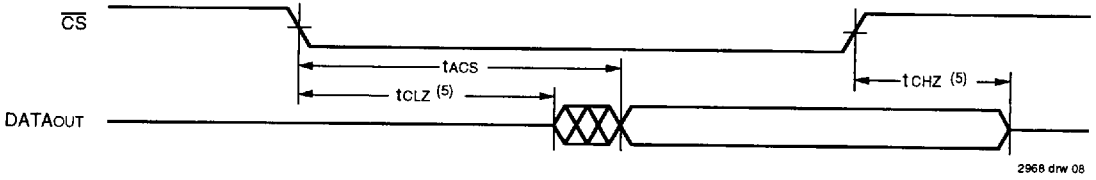
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



NOTES:
1. $\overline{WE}$ is HIGH for read cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state.

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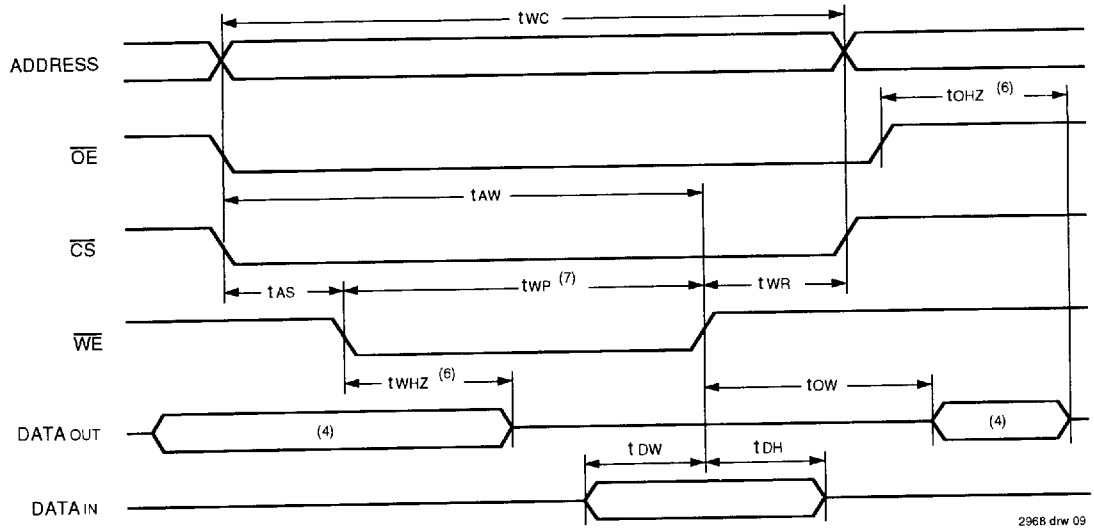
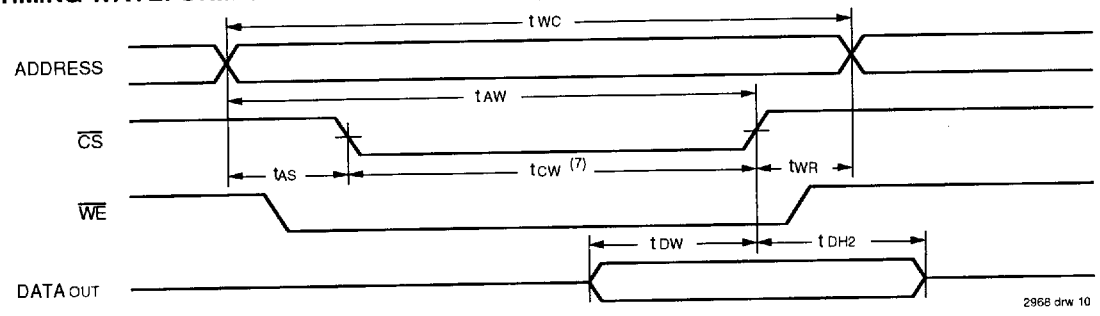
TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 5)



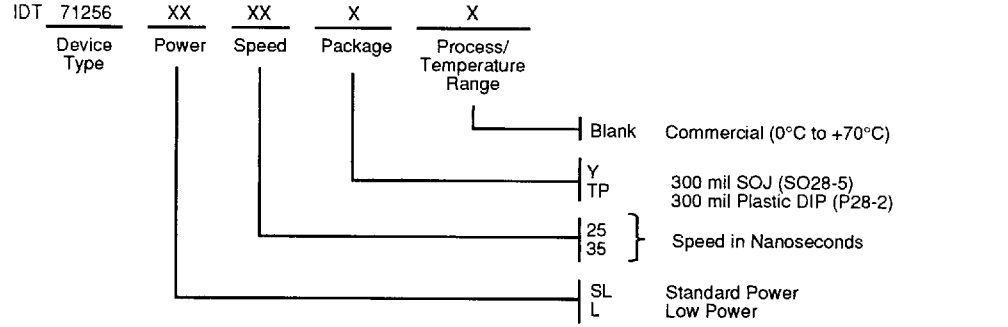
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (tCW or tWP) of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals must not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
6. Transition is measured ±200mV from steady state.
7. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP. For a $\overline{CS}$ controlled write cycle, $\overline{OE}$ may be LOW with no degradation to tCW.

ORDERING INFORMATION



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