

**ADVANCE
INFORMATION
IDT71281S/L
IDT71282S/L**

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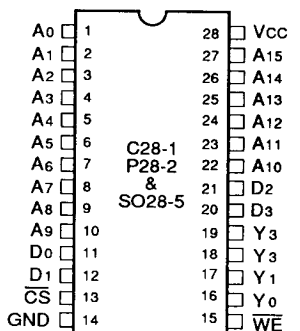
2969 drw 01

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DESCRIPTION (Continued)

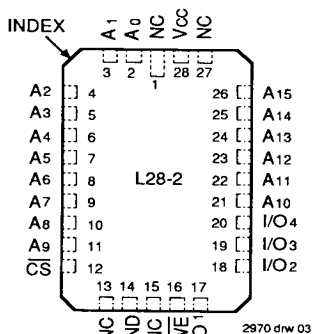
Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

PIN CONFIGURATION



2969 drw 02

DIP/SOJ
TOP VIEW



2970 drw 03

LCC
TOP VIEW

TRUTH TABLE⁽¹⁾

Mode	$\overline{CS}$	$\overline{WE}$	Output	Power
Standby	H	X	High-Z	Standby
Read	L	H	DOUT	Active
Write ⁽¹⁾	L	L	DIN	Active
Write ⁽²⁾	L	L	High-Z	Active

NOTE:

- For IDT71281 only.
- For IDT71282 only.
- H = V_{IH} , L = V_{IL} , X = Don't Care.

2969 tbi 02

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
PT	Power Dissipation	1.0	1.0	W
IOUT	DC Output Current	50	50	mA

NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2969 tbi 03

CAPACITANCE ($T_A = +25^\circ\text{C}$, $f = 1.0\text{MHz}$)

Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
CIN	Input Capacitance	$V_{IN} = 0V$	11	pF
COUT	Output Capacitance	$V_{OUT} = 0V$	11	pF

NOTE:

- This parameter is determined by device characterization, but is not production tested.

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PIN DESCRIPTIONS

Name	Description
A0-A15	Address Inputs
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
VCC	Power
D0-D3	DATAin
Y0-Y3	DATAout
GND	Ground

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RECOMMENDED OPERATING
TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

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RECOMMENDED DC OPERATING
CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	-0.5 ⁽¹⁾	—	0.8	V

NOTE:
1. VIL (min.)= -3.0V for pulse width less than 20ns.

2969 tkl 06

DC ELECTRICAL CHARACTERISTICS⁽¹⁾
(Vcc = 5V ± 10%, VLC = 0.2V, VHC = Vcc - 0.2V)

Symbol	Parameter	Power	71281/2S25 71281/2L25		71281/2S30 71281/2L30		71281/2S35 71281/2L35		71281/2S45 71281/2L45		71281/2S55 71281/2L55		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
Icc1	Operating Power Supply Current CS = VIL, Outputs Open Vcc = Max., f = 0 ⁽³⁾	S	130	—	—	140	120	130	120	130	—	130	mA
		L	120	—	—	130	110	120	110	120	—	120	
Icc2	Dynamic Operating Current CS = VIL, Outputs Open Vcc = Max., f = fMAX ⁽²⁾	S	170	—	—	180	160	170	160	170	—	170	mA
		L	150	—	—	150	130	140	130	140	—	150	
ISB	Standby Power Supply Current (TTL Level) CS ≥ VIH, Vcc = Max., Outputs Open, f = fMAX ⁽²⁾	S	35	—	—	35	35	35	35	35	—	35	mA
		L	20	—	—	20	20	20	20	20	—	20	
ISB1	Full Standby Power Supply Current (CMOS Level) CS ≥ VHC, Vcc = Max., f = 0 ⁽²⁾	S	30	—	—	35	30	35	30	35	—	35	mA
		L	1.5	—	—	4.5	1.5	4.5	1.5	4.5	—	4.5	

NOTES:
1. All values are maximum guaranteed values.
2. At f = fMAX address and data inputs are cycling at the maximum frequency of read cycles of 1/trc. f = 0 means no input lines change.

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AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

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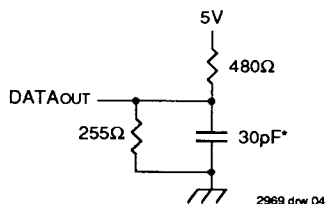


Figure 1. Output Load

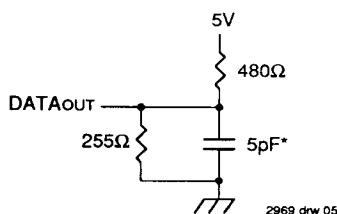


Figure 2. Output Load
(for tCLZ, tCHZ, tOW, and tWHZ)

*Includes scope and jig capacitances

DC ELECTRICAL CHARACTERISTICS

VCC = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT71281S/L			IDT71282S/L			Unit
			Min.	Typ. ⁽¹⁾	Max.	Min.	Typ.	Max.	
ILI	Input Leakage Current	VCC = Max., VIN = GND to VCC	—	—	10 5	—	—	5 2	μA
ILO	Output Leakage Current	VCC = Max., $\overline{CS}$ = VIH, VOUT = GND to VCC	—	—	10 5	—	—	5 2	μA
VOL	Output Low Voltage	IOL = 8mA, VCC = Min. IOL = 10mA, VCC = Min.	—	—	0.4 0.5	—	—	0.4 0.5	V
VOH	Output High Voltage	IOH = -4mA, VCC = Min.	2.4	—	—	2.4	—	—	V

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) VLC = 0.2V, VHC = VCC - 0.2V

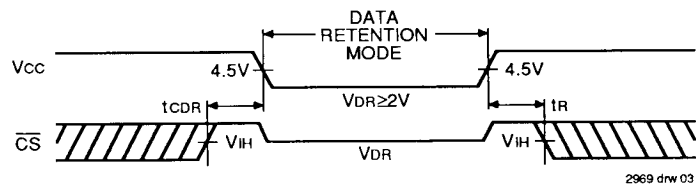
Symbol	Parameter	Test Condition	Min.	Typ. ⁽¹⁾ VCC @		Max. VCC @		Unit
				2.0V	3.0V	2.0V	3.0V	
VDR	VCC for Data Retention	—	2.0	—	—	—	—	V
ICCDR	Data Retention Current	$\overline{CS} \geq VHC$	MIL. COM'L	— 50	75 75	2000 500	3000 750	μA
tCDR ⁽³⁾	Chip Deselect to Data Retention Time		0	—	—	—	—	ns
tR ⁽³⁾	Operation Recovery Time		tRC ⁽²⁾	—	—	—	—	ns
ILI ⁽³⁾	Input Leakage Current		—	—	—	2	2	μA

NOTES:

- TA = +25°C.
- tRC = Read Cycle Time.
- This parameter is guaranteed, but not tested.

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LOW Vcc DATA RETENTION WAVEFORM



AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71281S/L25 ⁽¹⁾ 71282S/L25 ⁽¹⁾		71281S/L30 ⁽²⁾ 71282S/L30 ⁽²⁾		71281S/L35 71282S/L35		71281S/L45 71282S/L45		71281S/L55 ⁽²⁾ 71282S/L55 ⁽²⁾		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
tRC	Read Cycle Time	25	—	30	—	35	—	45	—	55	—	ns
tAA	Address Access Time	—	25	—	30	—	35	—	45	—	55	ns
tACS	Chip Select Access Time ⁽³⁾	—	25	—	30	—	35	—	45	—	55	ns
tCLZ	Chip Select to Output in Low Z ⁽⁴⁾	5	—	5	—	5	—	5	—	5	—	ns
tCHZ	Chip Select to Output in High Z ⁽⁴⁾	—	13	—	13	—	15	—	20	—	25	ns
tOH	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns
tPU	Chip Select to Power Up Time ⁽⁴⁾	0	—	0	—	0	—	0	—	0	—	ns
tPD	Chip Deselect to Power Down Time ⁽⁴⁾	—	25	—	30	—	35	—	45	—	55	ns
Write Cycle												
tWC	Write Cycle Time	20	—	20	—	30	—	40	—	50	—	ns
tCW	Chip Select to End of Write ⁽³⁾	20	—	20	—	30	—	40	—	50	—	ns
tAW	Address Valid to End of Write	20	—	20	—	30	—	40	—	50	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	20	—	20	—	30	—	40	—	50	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tWHZ	Write Enable to Output in High Z ^(4,7)	—	13	—	13	—	15	—	20	—	25	ns
tDW	Data Valid to End of Write	15	—	15	—	20	—	25	—	30	—	ns
tDH	Data HoldTime	0	—	0	—	0	—	0	—	0	—	ns
tOW	Output Active from End of Write ^(4,7)	5	—	5	—	5	—	5	—	5	—	ns
tVY	Data Valid to Output Valid ^(4,6)	—	20	—	20	—	30	—	35	—	40	ns
tWY	Write Enable to Output Valid ^(4,6)	—	20	—	20	—	30	—	35	—	40	ns

- NOTES:
- 0° to +70°C temperature range only.
 - 55°C to +125°C temperature range only.
 - Both chip selects must be active low for the device to be selected.
 - This parameter guaranteed but not tested.
 - Preliminary data for military devices only.
 - For IDT71281S/L only.
 - For IDT71282S/L only.

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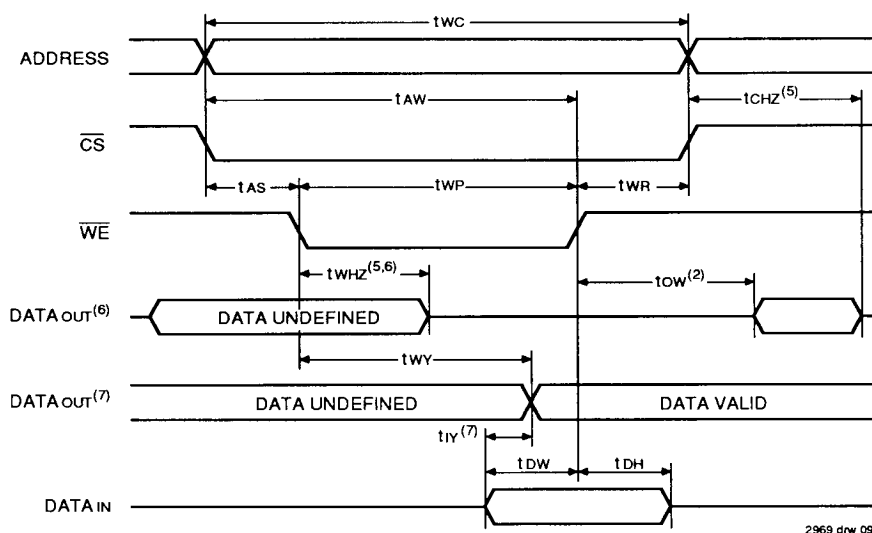
The timing diagram illustrates the relationship between the ADDRESS, CS (Chip Select), and DATAOUT signals. The ADDRESS signal is shown as a high-level signal with a pulse width labeled t_{RC} . The CS signal is shown as a low-level pulse with a width labeled t_{AA} . The DATAOUT signal is shown as a high-level signal with a pulse width labeled t_{CHZ} . The timing parameters are defined as follows:

- t_{RC} : Address pulse width.
- t_{AA} : CS pulse width.
- t_{OH} : Output hold time.
- t_{ACS} : Address setup time.
- $t_{CLZ}^{(4)}$: Address setup time (4).
- t_{CHZ} : Data output hold time.

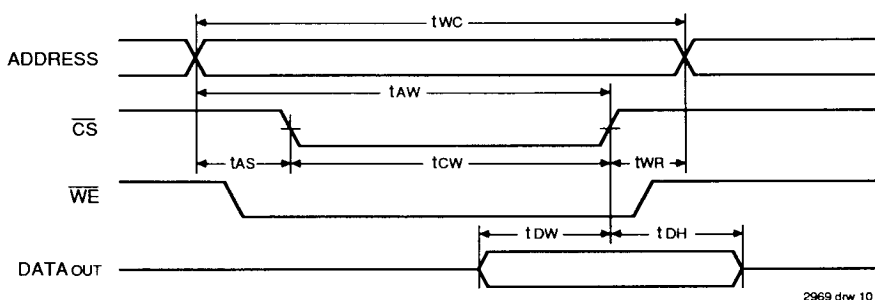
2969 dnr 06

1. WE is high for read cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured $\pm 200\text{mV}$ from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)^(1, 2, 3)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)^(1, 2, 3, 4)



NOTES:

- $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
- A write occurs during the overlap (t_{cw} or t_{wp}) of a low $\overline{CS}$ and a low $\overline{WE}$.
- t_{wr} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
- If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
- Transition is measured $\pm 200\text{mV}$ from steady state with a 5pF load (including scope and jig).
- IDT71282 only.
- IDT71281 only.

ORDERING INFORMATION

IDT	XXXXX	X	XX	X	X	
	Device Type	Power	Speed	Package	Process/ Temperature Range	
					Blank	Commercial (0°C to +70°C)
					B	Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B
					Y	SOJ
					TP	Plastic DIP
					TC	Sidebrazed DIP
					L28	28-Pin Leadless Chip Carrier
					25	Commercial Only
					30	Military Only
					35	} Speed in Nanoseconds
					45	
					55	
					S	Standard Power
					L	Low Power
					71281	256K (64K x 4-Bit)
					71282	256K (64K x 4-Bit) High Impedance Outputs

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