HIGH SPEED 2K X 16 DUAL-PORT SRAM

IDT7133SA/LA
IDT7143SA/LA

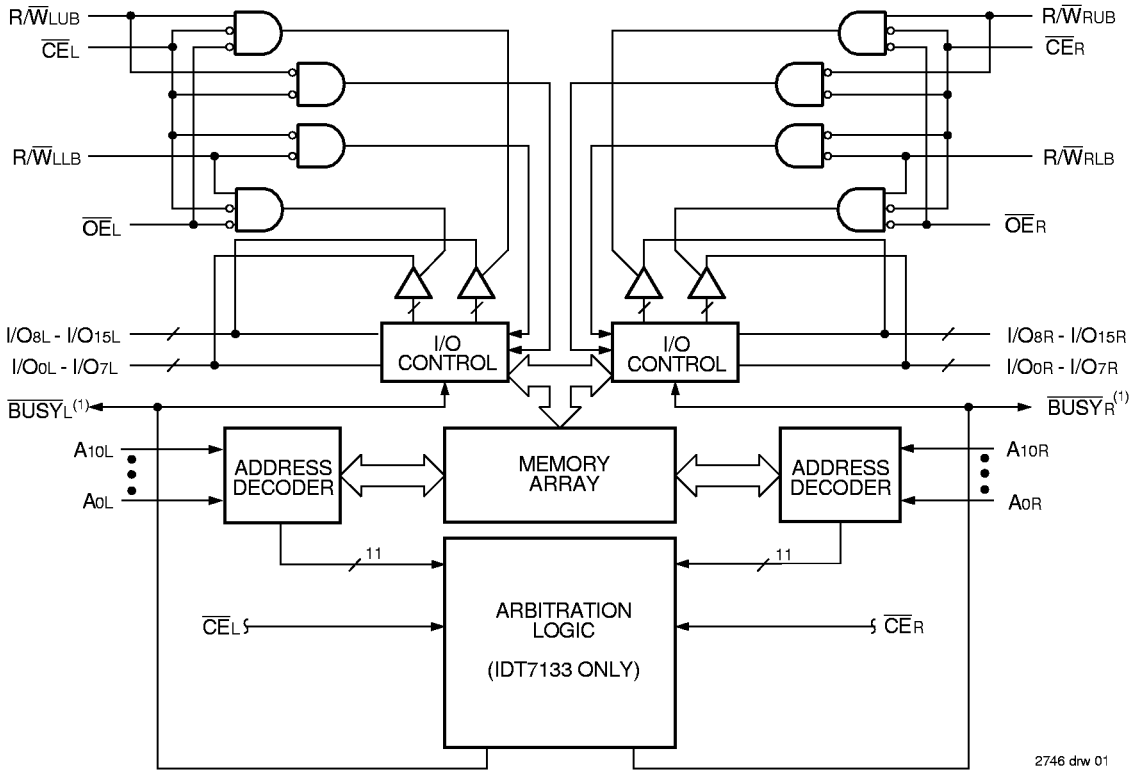
Features

- **High-speed access**
  - *Military: 25/35/45/55/70/90ns (max.)*
  - *Industrial: 55ns (max.)*
  - *Commercial: 20/25/35/45/55/70/90ns (max.)*
- Low-power operation
  - *IDT7133/43SA*
    Active: 1150mW (typ.)
    Standby: 5mW (typ.)
  - *IDT7133/43LA*
    Active: 1050mW (typ.)
    Standby: 1mW (typ.)
- Versatile control for write: separate write control for lower and upper byte of each port
- MASTER IDT7133 easily expands data bus width to 32 bits or more using SLAVE IDT7143
- On-chip port arbitration logic (IDT7133 only)
- $\overline{BUSY}$ output flag on IDT7133; $\overline{BUSY}$ input on IDT7143
- Fully asynchronous operation from either port
- Battery backup operation–2V data retention
- TTL-compatible; single 5V (±10%) power supply
- Available in 68-pin ceramic PGA, Flatpack, PLCC and 100-pin TQFP
- Military product compliant to MIL-PRF-38535 QML
- Industrial temperature range (–40°C to +85°C) is available for selected speeds

Description

The IDT7133/7143 are high-speed 2K x 16 Dual-Port Static RAMs. The IDT7133 is designed to be used as a stand-alone 16-bit Dual-Port RAM or as a "MASTER" Dual-Port RAM together with the IDT7143 "SLAVE" Dual-Port in 32-bit-or-more word width systems. Using the IDT MASTER/SLAVE Dual-Port RAM approach in 32-bit-or-wider

Functional Block Diagram



NOTE:
1. IDT7133 (MASTER): $\overline{BUSY}$ is open drain output and requires pull-up resistor.
   IDT7143 (SLAVE): $\overline{BUSY}$ is input.

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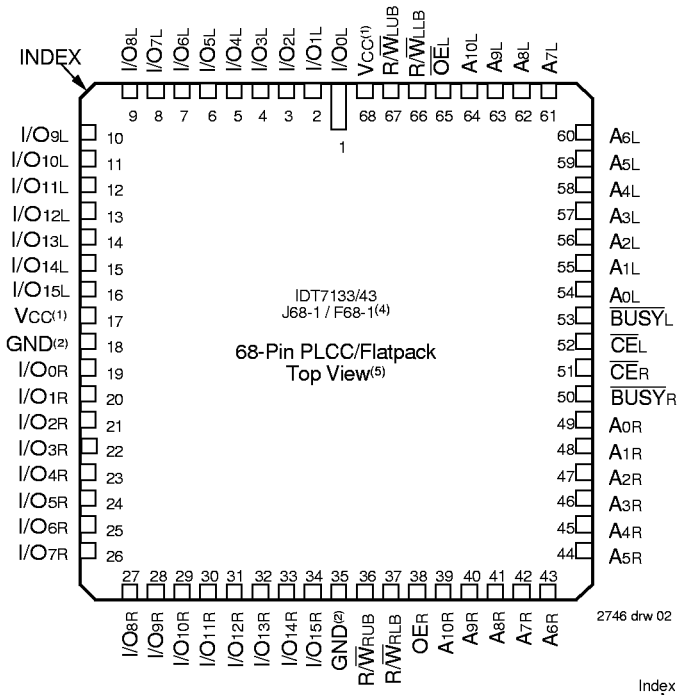
memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

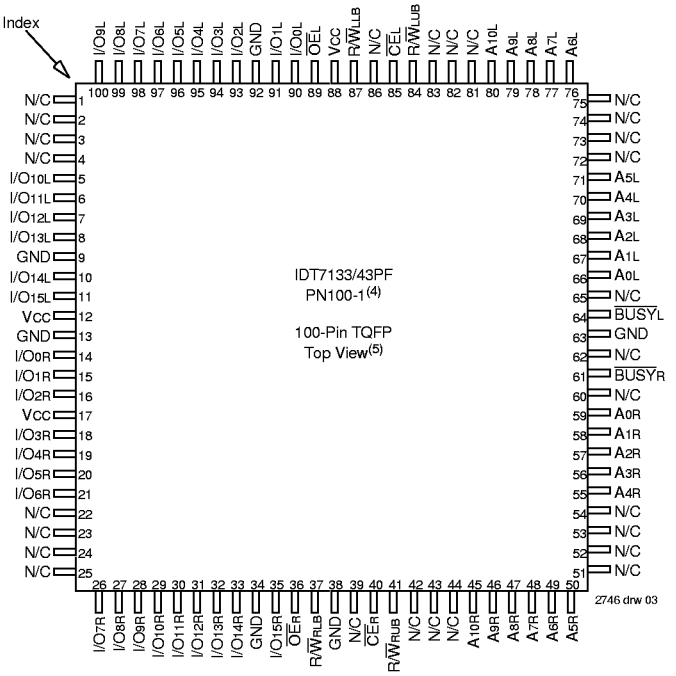
Both devices provide two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by $\overline{CE}$, permits the on-chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 500mW of power. Low-power (LA) versions offer battery backup data retention capability, with each port typically consuming 200µW for a 2V battery.

The IDT7133/7143 devices have identical pinouts. Each is packed in a 68-pin ceramic PGA, 68-pin flatpack, 68-pin PLCC and 100-pin TQFP. Military grade product is manufactured in compliance with the latest revision of MIL-PRF-38535 QML, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

Pin Configurations[1,2,3]

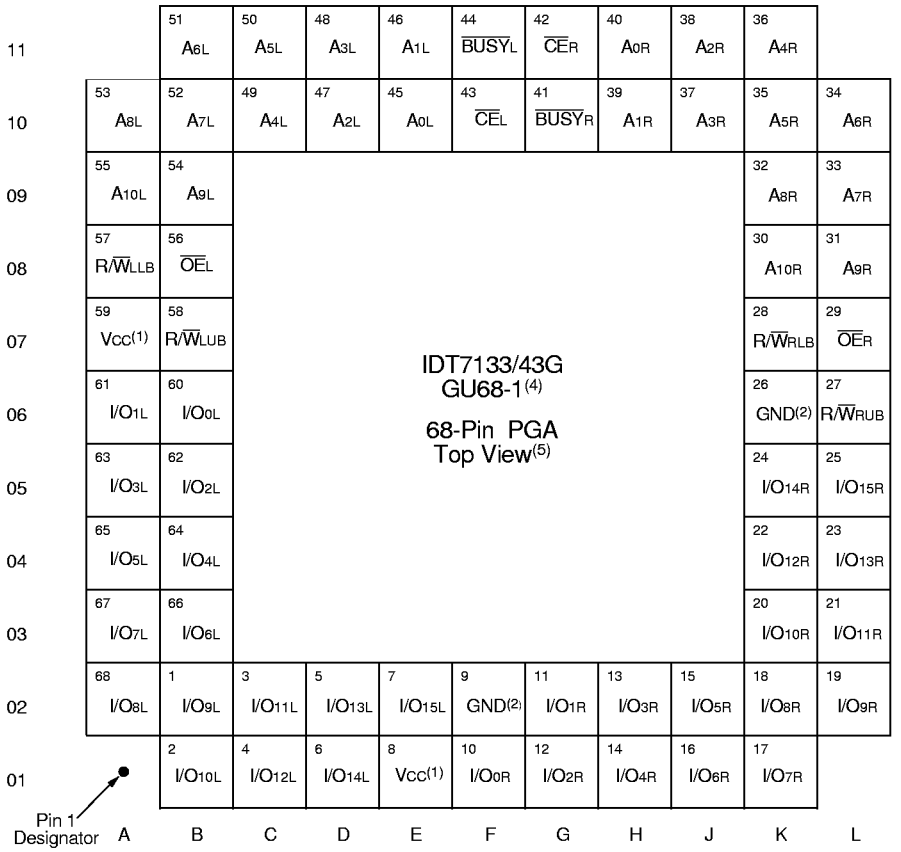




NOTES:

1. Both Vcc pins must be connected to the power supply to ensure reliable operation.
2. Both GND pins must be connected to the ground supply to ensure reliable operation.
3. J68-Package body is approximately 0.95 in x 0.95 in x 0.17 in.
   F68-Package body is approximately 1.18 in x 1.18 in x 0.16 in.
   PN100-Package body is approximately 14mm x 14mm x 1.4mm.
4. This package code is used to reference the package diagram.
5. This text does not indicate orientation of the actual part-marking.

Pin Configurations[1,2,3] (con't.)



2746 drw 04

NOTES:
1. Both Vcc pins must be connected to the power supply to ensure reliable operation.
2. Both GND pins must be connected to the ground supply to ensure reliable operation.
3. Package body is approximately 1.18 in x 1.18 in x 0.16 in.
4. This package code is used to reference the package diagram.
5. This text does not indicate orientation of the actual part-marking.

Pin Names

Left Port	Right Port	Names
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$R/\overline{W}_{LUB}$	$R/\overline{W}_{RUB}$	Upper Byte Read/Write Enable
$R/\overline{W}_{LLB}$	$R/\overline{W}_{RLB}$	Lower Byte Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
A_{0L} - A_{10L}	A_{0R} - A_{10R}	Address
I/O_{0L} - I/O_{15L}	I/O_{0R} - I/O_{15R}	Data Input/Output
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
V_{CC}		Power
GND		Ground

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Absolute Maximum Ratings(1)

Symbol	Rating	Commercial & Industrial	Military	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T(3)	Power Dissipation	2.0	2.0	W
I_{OUT}	DC Output Current	50	50	mA

2746 tbl 02

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{TERM} must not exceed Vcc + 10% for more than 25% of the cycle time or 10ns maximum, and is limited to $\leq$ 20mA for the period of $V_{TERM} \geq$ Vcc + 10%.

Capacitance (T_A = +25°C, f = 1.0mhz)

Symbol	Parameter(1)	Conditions(2)	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 3dV	11	pF

2746 tbl 03

NOTES:
1. This parameter is determined by device characterization but is not production tested.
2. 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.

Maximum Operating Temperature and Supply Voltage(1,2)

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%
Industrial	-40°C to +85°C	0V	5.0V ± 10%

2746 tbl 04

NOTES:
1. This is the parameter T_A.
2. Industrial temperature: for specific speeds, packages and powers contact your sales office.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0(2)	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

2746 tbl 05

NOTES:
1. V_{IL} (min.) = -1.5V for pulse width less than 10ns.
2. V_{TERM} must not exceed Vcc + 10%.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (Either port, Vcc = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	7133SA 7143SA		7133LA 7143LA		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current(1)	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage (I/O_0-I/O_{15})	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OL}	Open Drain Output Low Voltage ($\overline{BUSY}$)	I_{OL} = 16mA	—	0.5	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

2746 tbl 06

NOTE:
1. At Vcc $\leq$ 2.0V, input leakages are undefined.

DC Electrical Characteristics Operating Temperature and Supply Voltage Range[2,6] (Vcc = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		7133X20 7143X20 Com'l Only Typ.[1]	7133X20 7143X20 Com'l Only Max.	7133X25 7143X25 Com'l & Military Typ.[1]	7133X25 7143X25 Com'l & Military Max.	7133X35 7143X35 Com'l & Military Typ.[1]	7133X35 7143X35 Com'l & Military Max.	Unit
ICC	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = VIL, Outputs Open f = fMAX[3]	COM'L	S	250	310	250	300	240	295	mA
				L	230	280	230	270	210	250	
			MIL & IND	S	—	—	250	330	240	325	
				L	—	—	230	300	220	295	
ISB1	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R$ = VIH f = fMAX[3]	COM'L	S	25	80	25	80	25	70	mA
				L	25	70	25	70	25	60	
			MIL & IND	S	—	—	25	90	25	75	
				L	—	—	25	80	25	65	
ISB2	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}$"A" = VIL and $\overline{CE}$"B" = VIH[4] f=fMAX[3] Active Port Outputs Open	COM'L	S	140	200	140	200	120	180	mA
				L	120	180	100	170	100	160	
			MIL & IND	S	—	—	140	230	120	200	
				L	—	—	100	190	100	180	
ISB3	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ > VCC - 0.2V VIN > VCC - 0.2V or VIN < 0.2V, f = 0[4]	COM'L	S	1.0	15	1.0	15	1.0	15	mA
				L	0.2	5	0.2	4	0.2	4	
			MIL & IND	S	—	—	1.0	30	1.0	30	
				L	—	—	0.2	10	0.2	10	
ISB4	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}$"A" < 0.2V and $\overline{CE}$"B" > VCC - 0.2V[5] VIN > VCC - 0.2V or VIN < 0.2V Active Port Outputs Open f = fMAX[3]	COM'L	S	140	190	140	190	120	170	mA
				L	120	170	120	170	100	150	
			MIL & IND	S	—	—	140	220	120	190	
				L	—	—	120	200	100	170	

2746 tbl 07a

Symbol	Parameter	Test Condition	Version		7133X45 7143X45 Com'l & Military Typ.[1]	7133X45 7143X45 Com'l & Military Max.	7133X55 7143X55 Com'l, Ind & Military Typ.[1]	7133X55 7143X55 Com'l, Ind & Military Max.	7133X70/90 7143X70/90 Com'l & Military Typ.[1]	7133X70/90 7143X70/90 Com'l & Military Max.	Unit
ICC	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = VIL, Outputs Open f = fMAX[3]	COM'L	S	230	290	230	285	230	280	mA
				L	210	250	210	250	210	250	
			MIL & IND	S	230	320	230	315	230	310	
				L	210	290	210	285	210	280	
ISB1	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R$ = VIH f = fMAX[3]	COM'L	S	25	75	25	70	25	70	mA
				L	25	65	25	60	25	60	
			MIL & IND	S	25	80	25	80	25	75	
				L	25	70	25	70	25	65	
ISB2	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}$"A" = VIL and $\overline{CE}$"B" = VIH[4] f=fMAX[3] Active Port Outputs Open	COM'L	S	120	190	120	180	120	180	mA
				L	100	170	100	160	100	160	
			MIL & IND	S	120	210	120	210	120	200	
				L	100	190	100	190	100	180	
ISB3	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ > VCC - 0.2V VIN > VCC - 0.2V or VIN < 0.2V, f = 0[4]	COM'L	S	1.0	15	1.0	15	1.0	15	mA
				L	0.2	4	0.2	4	0.2	4	
			MIL & IND	S	1.0	30	1.0	30	1.0	30	
				L	0.2	10	0.2	10	0.2	10	
ISB4	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}$"A" < 0.2V and $\overline{CE}$"B" > VCC - 0.2V[5] VIN > VCC - 0.2V or VIN < 0.2V Active Port Outputs Open f = fMAX[3]	COM'L	S	120	180	120	170	120	170	mA
				L	100	160	100	150	100	150	
			MIL & IND	S	120	200	120	200	120	190	
				L	100	180	100	180	100	170	

2746 tbl 07b

NOTES:

1. VCC = 5V, TA = +25°C for Typ., and are not production tested. ICCDC = 180mA (typ.)
2. 'X' in part number indicates power rating (SA or LA)
3. At f = fMAX, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/ tRC, and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.
5. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
6. Industrial temperature: for other speeds, packages and powers contact your sales office.

Data Retention Characteristics

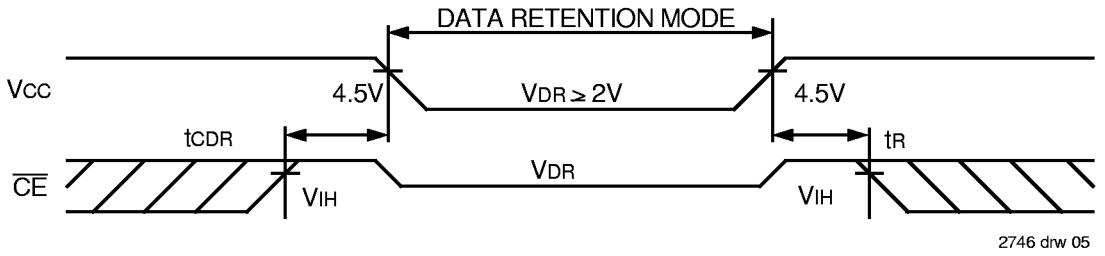
(LA Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Condition		7133LA/7143LA Min.	Typ.(1)	Max.	Unit
V_{DR}	Vcc for Data Retention	Vcc = 2V		2.0	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CE} \geq V_{HC}$	MIL. & IND.	—	100	4000	µA
		$V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	COM'L.	—	100	1500	
t_{CDR}(3)	Chip Deselect to Data Retention Time			0	—	—	V
t_R(3)	Operation Recovery Time			t_{RC}(2)	—	—	V

2746 tbl 08

NOTES:
1. Vcc = 2V, T_A = +25°C, and are not production tested.
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed by device characterization but is not production tested.

Data Retention Waveform



2746 drw 05

AC Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns Max.
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1, 2 and 3

2746 tbl 09

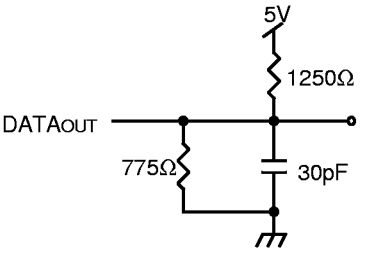


Figure 1. AC Output Test Load

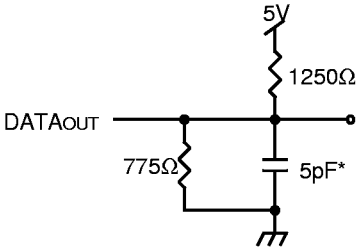
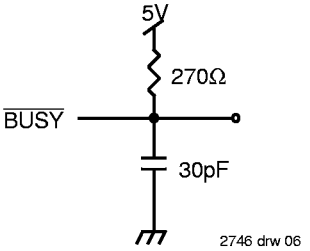


Figure 2. Output Load
(for t_{LZ}, t_{HZ}, t_{WZ}, t_{OW})
*Including scope and jig



2746 drw 06

Figure 3. $\overline{BUSY}$ Output Load
(IDT7133 only)

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage[3,4]

		7133X20 7143X20 Com'l Only		7133X25 7143X25 Com'l & Military		7133X35 7143X35 Com'l & Military		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
READ CYCLE								
t_{RC}	Read Cycle Time	20	—	25	—	35	—	ns
t_{AA}	Address Access Time	—	20	—	25	—	35	ns
t_{ACE}	Chip Enable Access Time	—	20	—	25	—	35	ns
t_{AOE}	Output Enable Access Time	—	12	—	15	—	20	ns
t_{OH}	Output Hold from Address Change	0	—	0	—	0	—	ns
t_{LZ}	Output Low-Z Time[1,2]	0	—	0	—	0	—	ns
t_{HZ}	Output High-Z Time[1,2]	—	12	—	15	—	20	ns
t_{PU}	Chip Enable to Power Up Time[2]	0	—	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time[2]	—	20	—	50	—	50	ns

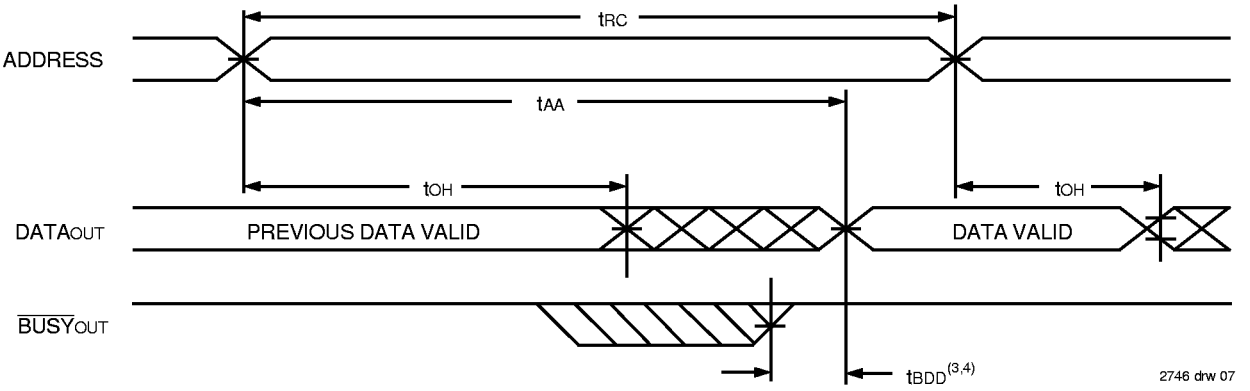
2746 tbl 10a

		7133X45 7143X45 Com'l & Military		7133X55 7143X55 Com'l, Ind & Military		7133X70/90 7143X70/90 Com'l & Military		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit
READ CYCLE								
t_{RC}	Read Cycle Time	45	—	55	—	70/90	—	ns
t_{AA}	Address Access Time	—	45	—	55	—	70/90	ns
t_{ACE}	Chip Enable Access Time	—	45	—	55	—	70/90	ns
t_{AOE}	Output Enable Access Time	—	25	—	30	—	40/40	ns
t_{OH}	Output Hold from Address Change	0	—	0	—	0/0	—	ns
t_{LZ}	Output Low-Z Time[1,2]	0	—	5	—	5/5	—	ns
t_{HZ}	Output High-Z Time[1,2]	—	20	—	20	—	25/25	ns
t_{PU}	Chip Enable to Power Up Time[2]	0	—	0	—	0/0	—	ns
t_{PD}	Chip Disable to Power Down Time[2]	—	50	—	50	—	50/50	ns

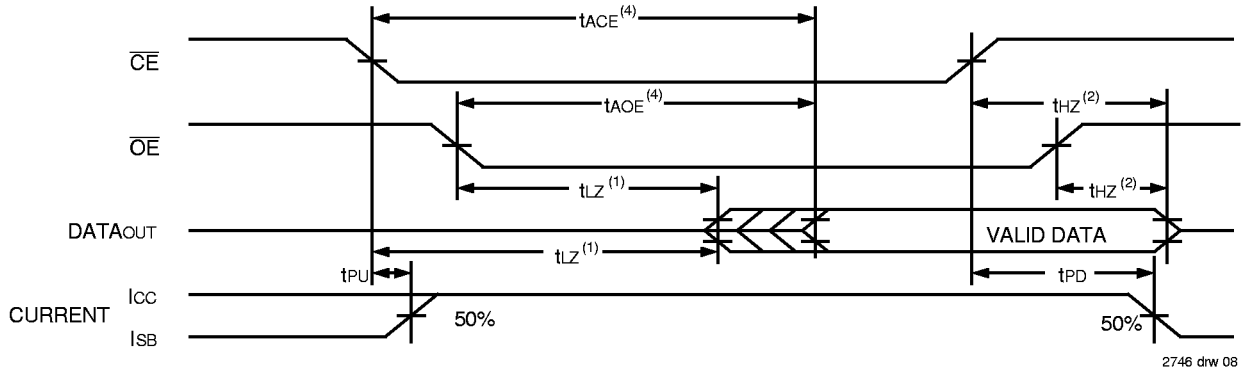
2746 tbl 10b

NOTES:
1. Transition is measured ±500mV fromLow or High-impedance voltage with load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. 'X' in part number indicates power rating (SA or LA).
4. Industrial temperature: for other speeds, packages and powers contact your sales office.

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE(5)



TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE(5)



NOTES:

1. Timing depends on which signal is asserted last, $\overline{OE}$ or $\overline{CE}$.
2. Timing depends on which signal is deasserted first, $\overline{OE}$ or $\overline{CE}$.
3. t_{BDD} delay is required only in a case where the opposite port is completing a write operation to the same address location. For simultaneous read operations, $\overline{BUSY}$ has no relationship to valid output data.
4. Start of valid data depends on which timing becomes effective last, t_{AOE}, t_{ACE}, t_{AA}, or t_{BDD}.
5. R/$\overline{W}$ = V_{IH}, and the address is valid prior to or coincidental with $\overline{CE}$ transition LOW.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage[5,6]

Symbol	Parameter	7133X20 7143X20 Com'l Only		7133X25 7143X25 Com'l & Military		7133X35 7143X35 Com'l & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE								
t_{WC}	Write Cycle Time[3]	20	—	25	—	35	—	ns
t_{EW}	Chip Enable to End-of-Write	15	—	20	—	25	—	ns
t_{AW}	Address Valid to End-of-Write	15	—	20	—	25	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	15	—	20	—	25	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	15	—	15	—	20	—	ns
t_{HZ}	Output High-Z Time[1,2]	—	12	—	15	—	20	ns
t_{DH}	Data Hold Time[4]	0	—	0	—	0	—	ns
t_{WZ}	Write Enable to Output in High-Z[1,2]	—	12	—	15	—	20	ns
t_{OW}	Output Active from End-of-Write[1,2,4]	0	—	0	—	0	—	ns

2746 tbl 11a

Symbol	Parameter	7133X45 7143X45 Com'l & Military		7133X55 7143X55 Com'l, Ind & Military		7133X70/90 7143X70/90 Com'l & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE								
t_{WC}	Write Cycle Time[3]	45	—	55	—	70/90	—	ns
t_{EW}	Chip Enable to End-of-Write	30	—	40	—	50/50	—	ns
t_{AW}	Address Valid to End-of-Write	30	—	40	—	50/50	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0/0	—	ns
t_{WP}	Write Pulse Width	30	—	40	—	50/50	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0/0	—	ns
t_{DW}	Data Valid to End-of-Write	20	—	25	—	30/30	—	ns
t_{HZ}	Output High-Z Time[1,2]	—	20	—	20	—	25/25	ns
t_{DH}	Data Hold Time[4]	5	—	5	—	5/5	—	ns
t_{WZ}	Write Enable to Output in High-Z[1,2]	—	20	—	20	—	25/25	ns
t_{OW}	Output Active from End-of-Write[1,2,4]	5	—	5	—	5/5	—	ns

2746 tbl 11b

NOTES:

1. Transition is measured ±500mV from Low or High-impedance voltage from the Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization but not production tested.
3. For MASTER/SLAVE combination, $t_{WC} = t_{BAA} + t_{WR} + t_{WP}$, since $R/\overline{W} = V_{IL}$ must occur after t_{BAA}.
4. The specification for t_{DH} must be met by the device supplying write data to the RAM under all operation conditions. Although t_{DH} and tow values will very over voltage and temperature, the actual t_{DH} will always be smaller than the actual tow.
5. 'X' in part number indicates power rating (SA or LA).
6. Industrial temperature: for other speeds, packages and powers contact your sales office.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage(6,7)

Symbol	Parameter	7133X20 7143X20 Com'l Only		7133X25 7143X25 Com'l & Military		7133X35 7143X35 Com'l & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
$\overline{BUSY}$ TIMING (For MASTER 71V33)								
t_{BAA}	$\overline{BUSY}$ Access Time from Address	—	20	—	20	—	30	ns
t_{BDA}	$\overline{BUSY}$ Disable Time from Address	—	20	—	20	—	30	ns
t_{BAC}	$\overline{BUSY}$ Access Time from Chip Enable	—	20	—	20	—	25	ns
t_{BDC}	$\overline{BUSY}$ Disable Time from Chip Enable	—	17	—	20	—	25	ns
t_{WDD}	Write Pulse to Data Delay(1)	—	40	—	50	—	60	ns
t_{DDD}	Write Data Valid to Read Data Delay(1)	—	30	—	35	—	45	ns
t_{BDD}	$\overline{BUSY}$ Disable to Valid Data(2)	—	25	—	30	—	35	ns
t_{APS}	Arbitration Priority Set-up Time(3)	5	—	5	—	5	—	ns
t_{WH}	Write Hold After $\overline{BUSY}$(5)	20	—	20	—	25	—	ns
$\overline{BUSY}$ INPUT TIMING (For SLAVE 71V43)								
t_{WB}	$\overline{BUSY}$ Input to Write(4)	0	—	0	—	0	—	ns
t_{WH}	Write Hold After $\overline{BUSY}$(5)	20	—	20	—	25	—	ns
t_{WDD}	Write Pulse to Data Delay(1)	—	40	—	50	—	60	ns
t_{DDD}	Write Data Valid to Read Data Delay(1)	—	30	—	35	—	45	ns

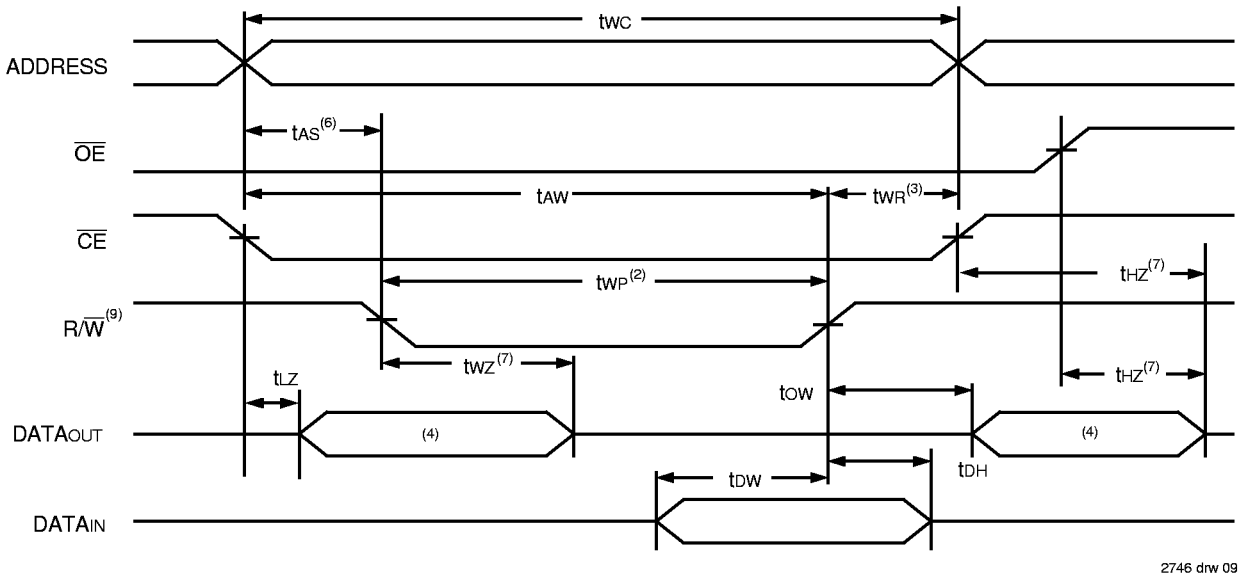
2746 tbl 12a

Symbol	Parameter	7133X45 7143X45 Com'l & Military		7133X55 7143X55 Com'l, Ind & Military		7133X70/90 7143X70/90 Com'l & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
$\overline{BUSY}$ TIMING (For MASTER 71V33)								
t_{BAA}	$\overline{BUSY}$ Access Time from Address	—	40	—	40	—	45/45	ns
t_{BDA}	$\overline{BUSY}$ Disable Time from Address	—	40	—	40	—	45/45	ns
t_{BAC}	$\overline{BUSY}$ Access Time from Chip Enable	—	30	—	35	—	35/35	ns
t_{BDC}	$\overline{BUSY}$ Disable Time from Chip Enable	—	25	—	30	—	30/30	ns
t_{WDD}	Write Pulse to Data Delay(1)	—	80	—	80	—	90/90	ns
t_{DDD}	Write Data Valid to Read Data Delay(1)	—	55	—	55	—	70/70	ns
t_{BDD}	$\overline{BUSY}$ Disable to Valid Data(2)	—	40	—	40	—	40/40	ns
t_{APS}	Arbitration Priority Set-up Time(3)	5	—	5	—	5/5	—	ns
t_{WH}	Write Hold After $\overline{BUSY}$(5)	30	—	30	—	30/30	—	ns
$\overline{BUSY}$ INPUT TIMING (For SLAVE 71V43)								
t_{WB}	$\overline{BUSY}$ Input to Write(4)	0	—	0	—	0/0	—	ns
t_{WH}	Write Hold After $\overline{BUSY}$(5)	30	—	30	—	30/30	—	ns
t_{WDD}	Write Pulse to Data Delay(1)	—	80	—	80	—	90/90	ns
t_{DDD}	Write Data Valid to Read Data Delay(1)	—	55	—	55	—	70/70	ns

2746 tbl 12b

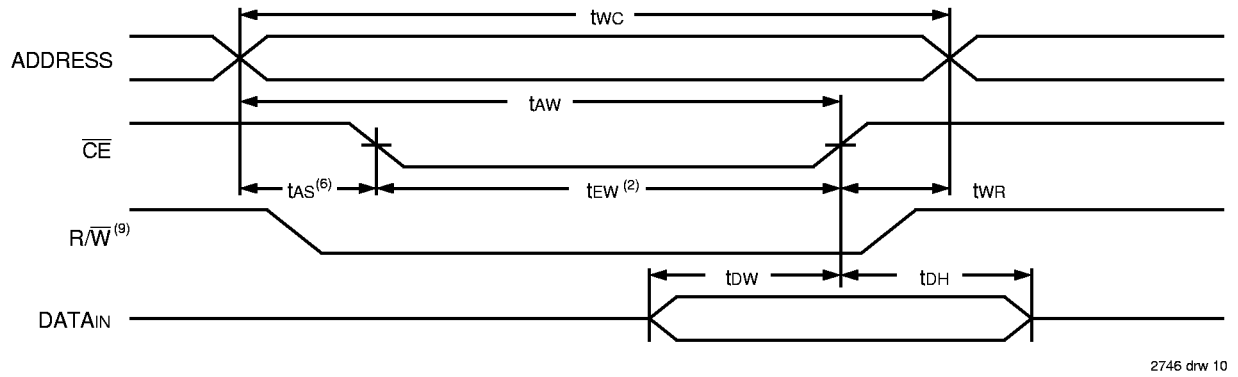
NOTES:
1. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port-to-Port Read and Busy".
2. t_{BDD} is calculated parameter and is greater of 0, t_{WDD} - t_{WP} (actual) or t_{DDD} - t_{DW} (actual).
3. To ensure that the earlier of the two ports wins.
4. To ensure that the write cycle is inhibited on port "B" during contention on port "A".
5. To ensure that a write cycle is completed on port "B" after contention on port "A".
6. 'X' in part number indicates power rating (SA or LA).
7. Industrial temperature: for other speeds, packages and powers contact your sales office.

Timing Waveform of Write Cycle No. 1 (R/$\overline{W}$ Controlled Timing)[1,5,8]



2746 drw 09

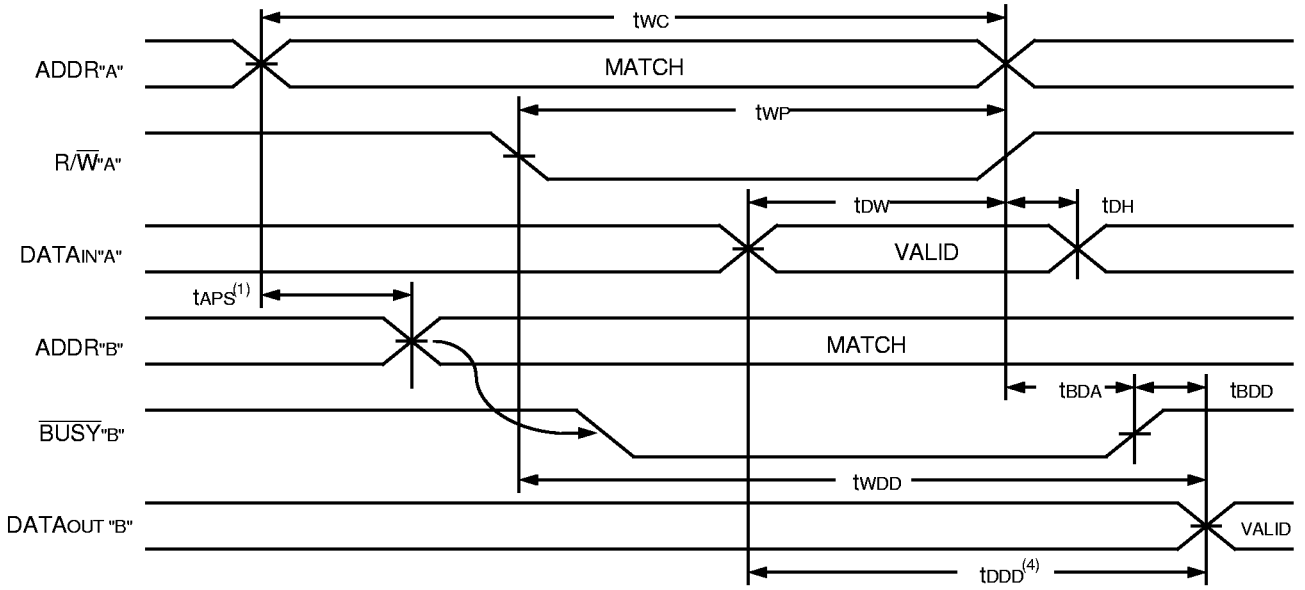
Write Cycle No. 2 ($\overline{CE}$ Controlled Timing)[1,5]



2746 drw 10

NOTES:
1. R/$\overline{W}$ or $\overline{CE}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of a $\overline{CE}$ = V_{IL} and a R/$\overline{W}$ = V_{IL}.
3. t_{WR} is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going HIGH to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CE}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition, the outputs remain in the High-impedance state.
6. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is asserted last.
7. Timing depends on which enable signal is de-asserted first, $\overline{CE}$ or $\overline{OE}$.
8. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during an R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.
9. R/$\overline{W}$ for either upper or lower byte.

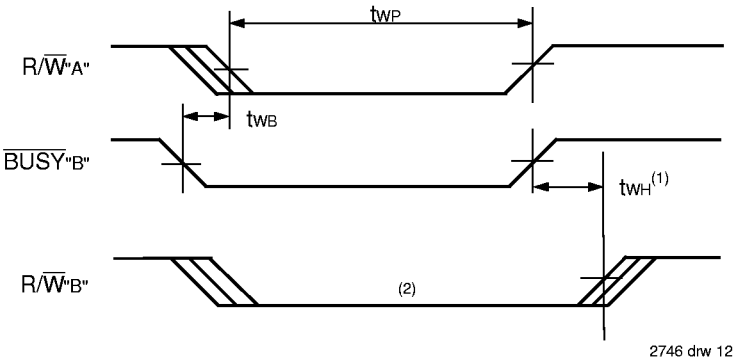
Timing Waveform of Write with Port-to-Port Read and $\overline{BUSY}$(1,2,3)



2746 drw 11

NOTES:
1. To ensure that the earlier of the two ports wins, t_{APS} is ignored for Slave (IDT7143).
2. $\overline{CE}_L = \overline{CE}_R = V_{IL}$
3. $\overline{OE} = V_{IL}$ for the reading port.
4. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".

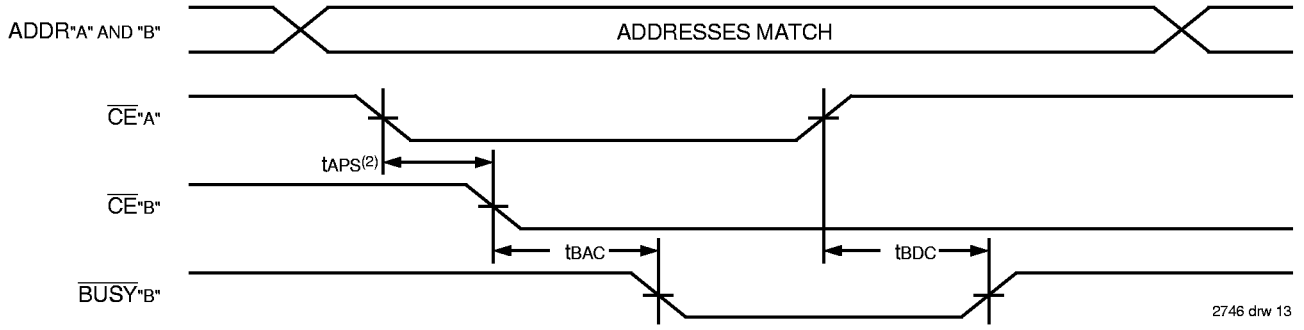
Timing Waveform of Write with $\overline{BUSY}$(3)



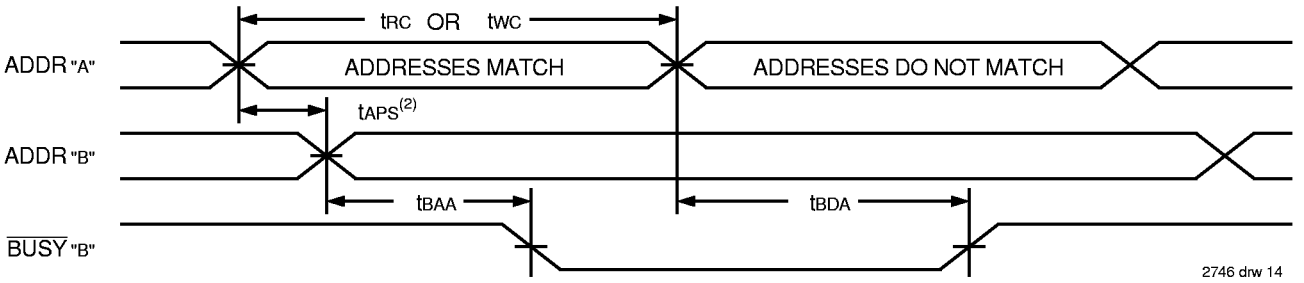
2746 drw 12

NOTES:
1. t_{WH} must be met for both $\overline{BUSY}$ input (IDT7143, slave) and output (IDT7133, master).
2. $\overline{BUSY}$ is asserted on port "B" blocking R/$\overline{W}$"B", until $\overline{BUSY}$"B" goes HIGH.
3. All timing is the same for left and right ports. Port "A" may be either left or right port. Port "B" is the opposite from port "A".

Timing Waveform of $\overline{BUSY}$ Arbitration Controlled by $\overline{CE}$ Timing(1)



Timing Waveform of $\overline{BUSY}$ Arbitration Controlled by Addresses(1)



NOTES:
1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from port "A".
2. If tAPS is not satisfied, the $\overline{BUSY}$ will be asserted on one side or the other, but there is no guarantee on which side $\overline{BUSY}$ will be asserted (IDT7133 only).

Functional Description

The IDT7133/43 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT7133/43 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ HIGH). When a port is enabled, access to the entire memory array is permitted. Non-contention READ/WRITE conditions are illustrated in Truth Table 1.

Busy Logic

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is "busy". The $\overline{BUSY}$ pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a $\overline{BUSY}$ indication, the write signal is gated internally to prevent the write from proceeding.

The use of $\overline{BUSY}$ logic is not required or desirable for all applications. In some cases it may be useful to logically OR the $\overline{BUSY}$ outputs together and use any $\overline{BUSY}$ indication as an interrupt source to flag the event of an illegal or illogical operation. If the write inhibit function of BUSY logic is not desirable, the $\overline{BUSY}$ logic can be disabled by using the IDT7143 (SLAVE). In the IDT7143, the $\overline{BUSY}$ pin operates solely as a write inhibit input pin. Normal operation can be programmed by tying the $\overline{BUSY}$ pins HIGH. If desired, unintended write operations can be prevented to a port by tying the $\overline{BUSY}$ pin for that port LOW. The $\overline{BUSY}$ outputs on the IDT 7133 RAM are open drain and require pull-up resistors.

Width Expansion with Busy Logic Master/Slave Arrays

When expanding an IDT7133/43 RAM array in width while using $\overline{BUSY}$ logic, one master part is used to decide which side of the RAM array will receive a $\overline{BUSY}$ indication, and to output that indication. Any number of slaves to be addressed in the same address range as the master, use the $\overline{BUSY}$ signal as a write inhibit signal. Thus on the IDT7133 RAM the $\overline{BUSY}$ pin is an output and on the IDT7143 RAM, the $\overline{BUSY}$ pin is an input (see Figure 3).

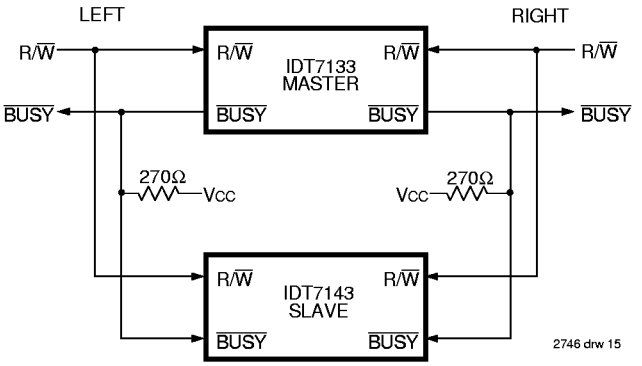


Figure 4. Busy and chip enable routing for both width and depth expansion with the IDT7133 (MASTER) and the IDT7143 (SLAVE).

Expanding the data bus width to 32 bits or more in a Dual-Port RAM system implies that several chips will be active at the same time. If each chip includes a hardware arbitrator, and the addresses for each chip arrive at the same time, it is possible that one will activate its $\overline{BUSY}_L$ while another activates its $\overline{BUSY}_R$ signal. Both sides are now $\overline{BUSY}$ and the CPUs will await indefinitely for their port to become free.

To avoid the "Busy Lock-Out" problem, IDT has developed a MASTER/SLAVE approach where only one hardware arbitrator, in the MASTER, is used. The SLAVE has $\overline{BUSY}$ inputs which allow an interface to the MASTER with no external components and with a speed advantage over other systems.

When expanding Dual-Port RAMs in width, the writing of the SLAVE RAMs must be delayed until after the $\overline{BUSY}$ input has settled. Otherwise, the SLAVE chip may begin a write cycle during a contention situation. Conversely, the write pulse must extend a hold time past $\overline{BUSY}$ to ensure that a write cycle takes place after the contention is resolved. This timing is inherent in all Dual-Port memory systems where more than one chip is active at the same time.

The write pulse to the SLAVE should be delayed by the maximum arbitration time of the MASTER. If, then, a contention occurs, the write to the SLAVE will be inhibited due to $\overline{BUSY}$ from the MASTER.

Truth Table I – Non-Contention Read/Write Control(4)

LEFT OR RIGHT PORT(1)						
$R/\overline{W}_{LB}$	$R/\overline{W}_{UB}$	$\overline{CE}$	$\overline{OE}$	I/O_{0-7}	I/O_{8-15}	Function
X	X	H	X	Z	Z	Port Disabled and in Power Down Mode, I_{SB2}, I_{SB4}
X	X	H	X	Z	Z	$CE_R = CE_L = V_{IH}$, Power Down Mode, I_{SB1} or I_{SB3}
L	L	L	X	$DATA_{IN}$	$DATA_{IN}$	Data on Lower Byte and Upper Byte Written into Memory(2)
L	H	L	L	$DATA_{IN}$	$DATA_{OUT}$	Data on Lower Byte Written into Memory(2), Data in Memory Output on Upper Byte(3)
H	L	L	L	$DATA_{OUT}$	$DATA_{IN}$	Data in Memory Output on Lower Byte(3), Data on Upper Byte Written into Memory(2)
L	H	L	H	$DATA_{IN}$	Z	Data on Lower Byte Written into Memory(2)
H	L	L	H	Z	$DATA_{IN}$	Data on Upper Byte Written into Memory(2)
H	H	L	L	$DATA_{OUT}$	$DATA_{OUT}$	Data in Memory Output on Lower Byte and Upper Byte
H	H	L	H	Z	Z	High Impedance Outputs

2746 tbl 13

NOTES:
1. A_{0L} - $A_{10L} \neq A_{0R}$ - A_{10R}
2. If $\overline{BUSY}$ = LOW, data is not written.
3. If $\overline{BUSY}$ = LOW, data may not be valid, see t_{WDD} and t_{DDD} timing.
4. "H" = HIGH, "L" = LOW, "X" = Don't Care, "Z" = High-Impedance, "LB" = Lower Byte, "UB" = Upper Byte

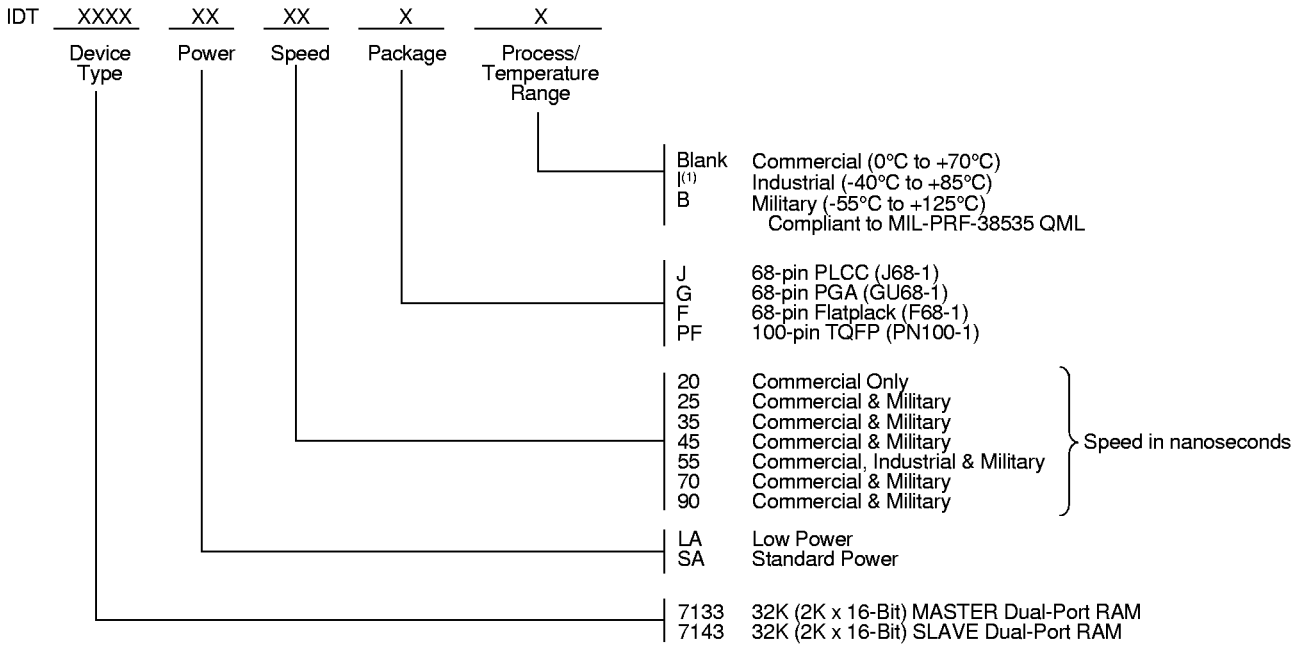
Truth Table II — Address $\overline{BUSY}$ Arbitration

Inputs			Outputs		
$\overline{CE}_L$	$\overline{CE}_R$	A_{0L}-A_{10L} A_{0R}-A_{10R}	$\overline{BUSY}_L$(1)	$\overline{BUSY}_R$(1)	Function
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	H	MATCH	H	H	Normal
L	L	MATCH	(2)	(2)	Write Inhibit(3)

2746 tbl 14

NOTES:
1. Pins $\overline{BUSY}_L$ and $\overline{BUSY}_R$ are both outputs on the IDT7133 (MASTER). Both are inputs on the IDT7143 (SLAVE). On Slaves the $\overline{BUSY}$ input internally inhibits writes.
2. "L" if the inputs to the opposite port were stable prior to the address and enable inputs of this port. "H" if the inputs to the opposite port became stable after the address and enable inputs of this port. If t_{APS} is not met, either $\overline{BUSY}_L$ or $\overline{BUSY}_R$ = V_{IL} will result $\overline{BUSY}_L$ and $\overline{BUSY}_R$ outputs can not be LOW simultaneously.
3. Writes to the left port are internally ignored when $\overline{BUSY}_L$ outputs are driving LOW regardless of actual logic level on the pin. Writes to the right port are internally ignored when $\overline{BUSY}_R$ outputs are driving LOW regardless of actual logic level on the pin.

Ordering Information



2746 drw 16

NOTE:
1. Industrial temperature range is available on selected PLCC packages in standard power. For other speeds, packages and powers contact your sales office.

Datasheet Document History

12/18/98:	Initiated datasheet document history
	Converted to new format
	Cosmetic and typographical corrections
	Added additional notes to pin configurations
	Page 2 corrected PN100 pinout
2/17/99:	Corrected PF ordering code
3/9/99:	Cosmetic and typographical corrections

CORPORATE HEADQUARTERS
2975 Stender Way
Santa Clara, CA 95054

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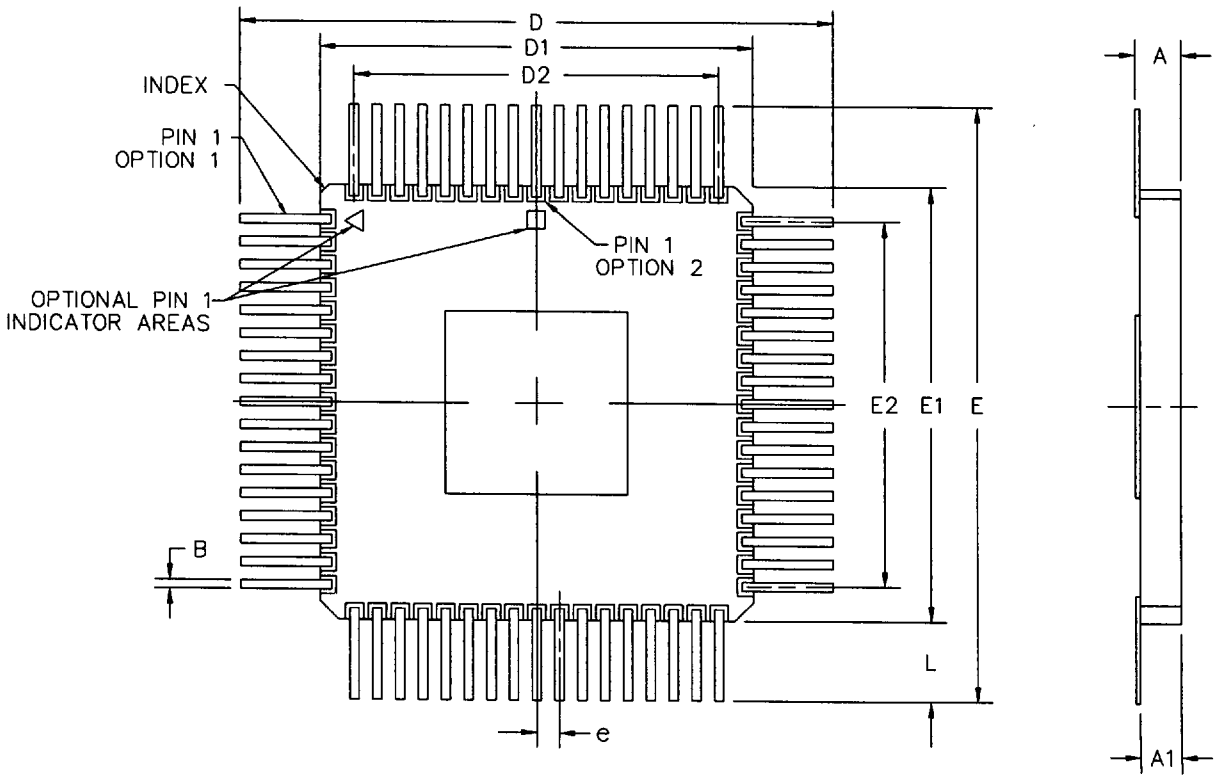
fax: 408-492-8674
www.idt.com

for Tech Support:
831-754-4613
DualPortHelp@idt.com

PACKAGE DIAGRAM OUTLINES

FLATPACK (Continued)

DCN	REV	DESCRIPTION	DATE	APPROVALS
17049	00	ORIGINAL ISSUE	11/30/89	D. G.
19350	01	CHANGE PIN 1 LOCATION	11/07/90	D. G.
27425	02	CHANGE PIN 1 LOCATION	01/05/95	D. G.
28663	03	ADDED PIN 1 OPTION 2		



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. ALL DIMENSIONS ARE IN INCHES.
2. BSC – BASIC LEAD SPACING BETWEEN CENTERS.
3. SYMBOL "N" REPRESENTS NUMBER OF LEADS.
4. INDEX CHAMFER .020, OTHER CHAMFERS .040 (X3).

DWG #	F68-1	
SYMBOL	MIN	MAX
A	.080	.145
A1	.070	.090
B	.016	.021
C	.008	.012
D/E	1.640	1.870
D1/E1	.926	.970
D2/E2	.800 BSC	
e	.050 BSC	
L	.350	.450
N	68	
ND	17	

JEDEC	CONFIGURATION	EXCEPTIONS
MIL-M-38510	MO-081-AA	NONE
	NOT LISTED	N/A

TOLERANCES UNLESS OTHERWISE SPECIFIED
FRAC ± – DEC ± – ANGLES ± –

APPROVALS	DATE
DRAWN A.A	11/89
CHECKED	

Integrated Device Technology, Inc.
3236 Scott Blvd., Santa Clara, CA 95051
(408) 727-6116 FAX: (408) 727-2328

68 LD QUAD FLAT PACK
MARKETING DRAWING

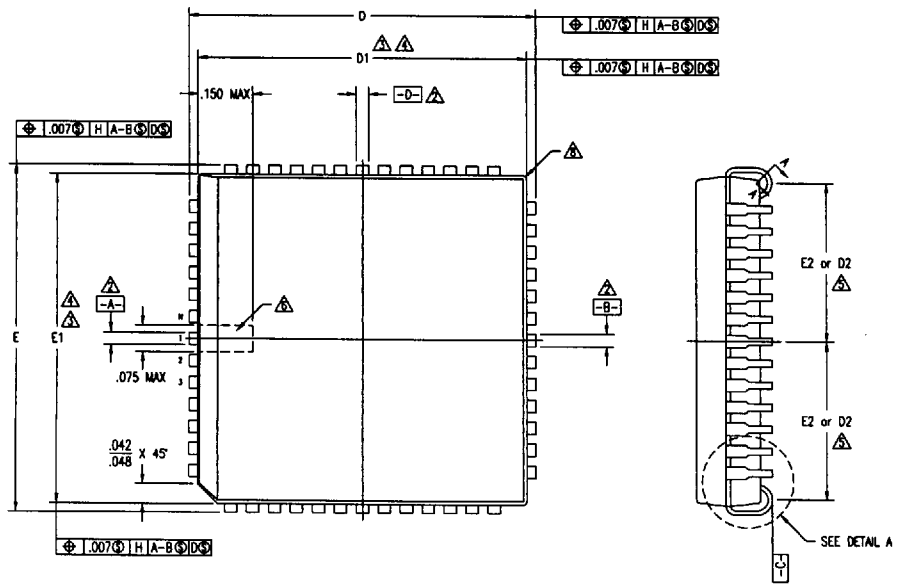
SCALE	SIZE	DRAWING NO.	REV
N/A	A	PSC-2085	03

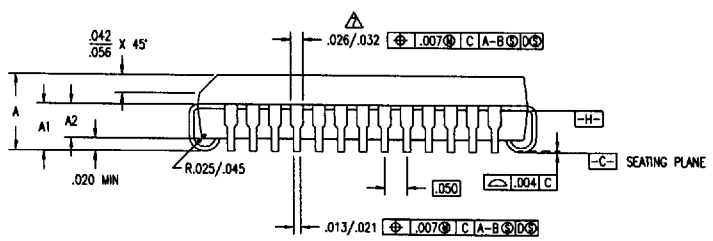
DO NOT SCALE DRAWING | SHEET 11

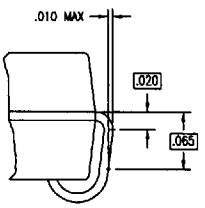
PACKAGE DIAGRAM OUTLINES

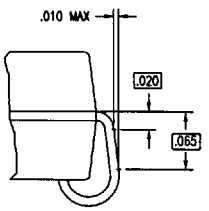
PLCC

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27647	06	REDRAW TO JEDEC FORMAT	03/15/95	

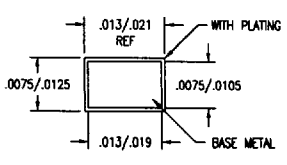








DETAIL A



SECTION A-A

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR XX± ± XXX± XXXX±		Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070	
APPROVALS	DATE	TITLE	PL PACKAGE OUTLINE SQUARE PLCC .050 PITCH
DRAWN dd	08/15/88		
CHECKED		SIZE C	DRAWING No. PSC-4008 REV 06
		DO NOT SCALE DRAWING	

PLCC (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27647	06	REDRAW TO JEDEC FORMAT	03/15/95	

DWG #	J28-1			
SYMBOL	JEDEC VARIATION AB			NOTE
	MIN	NOM	MAX	
A	.165	.172	.180	
A1	.095	.105	.115	
A2	.062	–	.083	
D	.485	.490	.495	
D1	.450	.453	.456	3,4
D2	.195	.205	.215	5
E	.485	.490	.495	
E1	.450	.453	.456	3,4
E2	.191	.205	.219	5
N	28			

DWG #	J44-1			
JEDEC VARIATION AC				NOTE
MIN	NOM	MAX		
.165	.172	.180		
.095	.105	.115		
.062	–	.083		
.685	.690	.695		
.650	.653	.656	3,4	
.295	.305	.315	5	
.685	.690	.695		
.650	.653	.656	3,4	
.291	.305	.319	5	
44				

DWG #	J52-1			
JEDEC VARIATION AD				NOTE
MIN	NOM	MAX		
.165	.172	.180		
.095	.105	.115		
.062	–	.083		
.785	.790	.795		
.750	.753	.756	3,4	
.345	.355	.365	5	
.785	.790	.795		
.750	.753	.756	3,4	
.341	.355	.369	5	
52				

DWG #	J68-1			
JEDEC VARIATION AE				NOTE
MIN	NOM	MAX		
.165	.172	.180		
.095	.105	.115		
.062	–	.083		
.985	.990	.995		
.950	.953	.956	3,4	
.445	.455	.465	5	
.985	.990	.995		
.950	.953	.956	3,4	
.441	.455	.469	5	
68				

DWG #	J84-1			
JEDEC VARIATION AF				NOTE
MIN	NOM	MAX		
.165	.172	.180		
.095	.105	.115		
.059	–	.080		
1.185	1.190	1.195		
1.150	1.154	1.156	3,4	
.545	.555	.565	5	
1.185	1.190	1.195		
1.150	1.154	1.156	3,4	
.541	.555	.569	5	
84				

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. DATUMS [A-B] AND [-D-] TO BE DETERMINED AT DATUM PLANE [-H-]
3. DIMENSIONS D1 AND E1 ARE TO BE DETERMINED AT DATUM PLANE [-H-]
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .010 PER SIDE. D1 AND E1 ARE BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH
5. DIMENSIONS D2 AND E2 ARE TO BE DETERMINED AT SEATING PLANE [-C-] CONTACT POINT
6. DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
7. LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .007 TOTAL MAXIMUM PER LEAD
8. EXACT SHAPE OF EACH CORNER IS OPTIONAL
9. THESE DIMENSIONS DETERMINE THE MAXIMUM ANGLE OF THE LEAD FOR SOCKET APPLICATIONS
10. ALL DIMENSIONS ARE IN INCHES
11. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-018, VARIATION AB, AC, AD, AE & AF. EXCEPTIONS: JEDEC MAXIMUM BASE METAL LEAD WIDTH IS .018

TOLERANCES UNLESS SPECIFIED		
DECIMAL	ANGULAR	
XX±	±	
XXX±		
XXXX±		

Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA 95054
PHONE: (408) 727-6116
FAX: (408) 492-8674 TWX: 910-338-2070

APPROVALS	DATE
DRAWN AA	06/15/95
CHECKED	

TITLE: PL PACKAGE OUTLINE
SQUARE PLCC
.050 PITCH

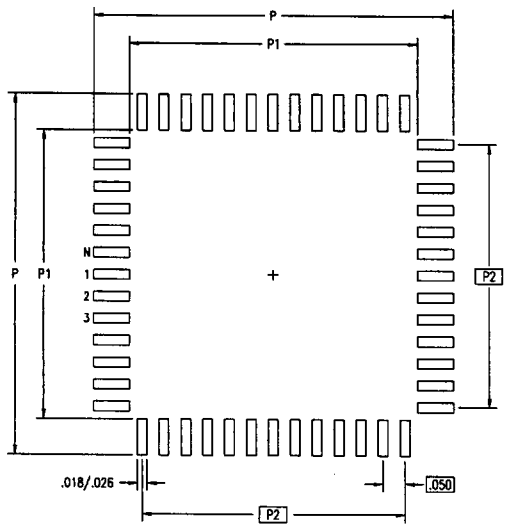
SIZE	DRAWING No.	REV
C	PSC-4008	06

DO NOT SCALE DRAWING

PLCC (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27647	08	REDRAW TO JEDEC FORMAT	03/15/95	

LAND PATTERN DIMENSIONS



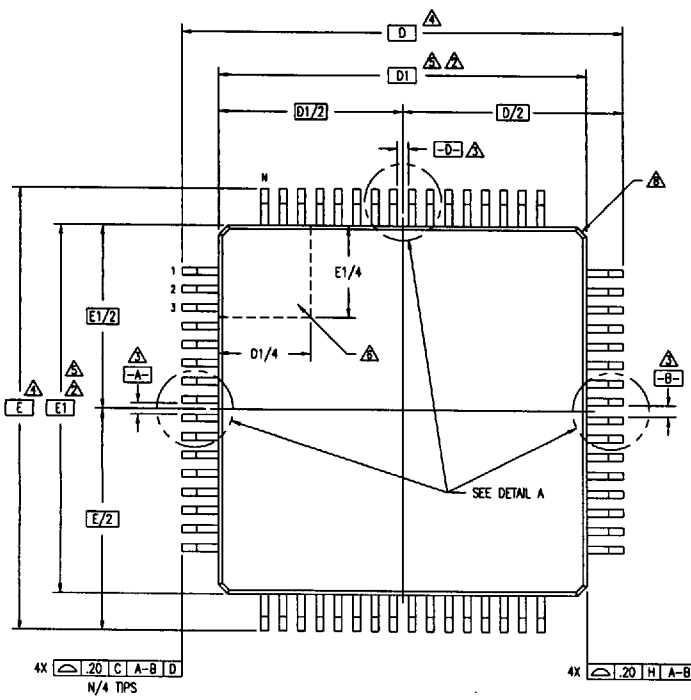
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
P	.520	.528	.720	.728	.820	.828	1.020	1.028	1.220	1.228
P1	.354	.362	.554	.562	.654	.662	.854	.862	1.054	1.062
P2	.300 BSC		.500 BSC		.600 BSC		.800 BSC		1.000 BSC	
N	28		44		52		68		84	

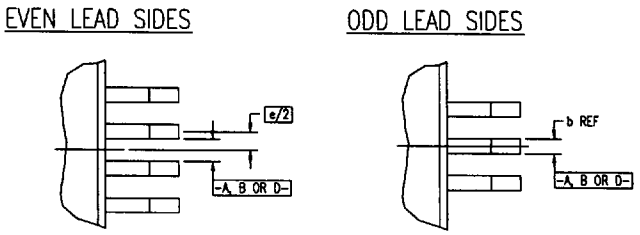
TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070
DECIMAL XX± XXX± XXXX±	ANGULAR ±	
APPROVALS	DATE	TITLE PL PACKAGE OUTLINE SQUARE PLCC .050 PITCH
DRAWN dd	08/15/89	
CHECKED		SIZE C DRAWING No. PSC-4008 REV 06
		DO NOT SCALE DRAWING

PACKAGE DIAGRAM OUTLINES

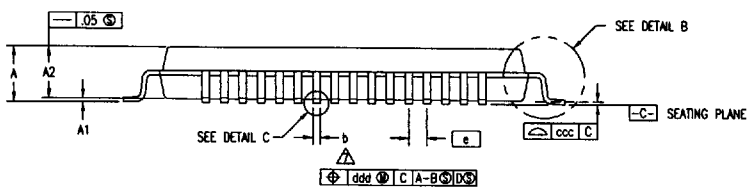
TQFP

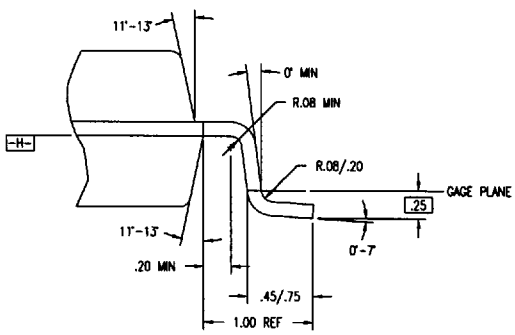
REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
22167	00	INITIAL RELEASE	03/12/92	T. VU
23823	01	ADD 80 & 100 LD	02/26/93	T. VU
24911	02	ADD 120 LD	10/06/93	T. VU
27384	03	REDRAW TO JEDEC FORMAT	12/10/94	



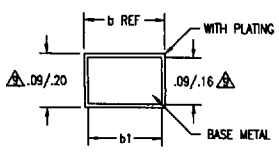


DETAIL A





DETAIL B



DETAIL C

TOLERANCES UNLESS SPECIFIED			Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070		
DECIMAL	ANGULAR				
XX±	±				
XXX±					
XXXX±					
APPROVALS	DATE		TITLE	PN PACKAGE OUTLINE 14.0 X 14.0 X 1.4 mm TQFP 1.00/.10 FORM	
DRAWN AA	03/12/92				
CHECKED			SIZE C	DRAWING No. PSC-4036	REV 03
			DO NOT SCALE DRAWING		

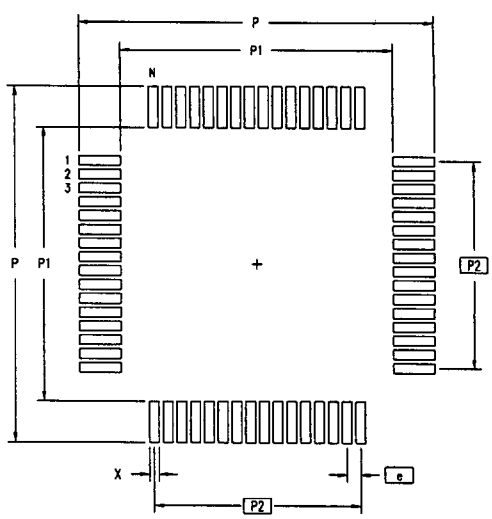
PACKAGE DIAGRAM OUTLINES

TQFP (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
22167	00	INITIAL RELEASE	03/12/92	T. VU
23823	01	ADD 80 & 100 LD	02/26/93	T. VU
24911	02	ADD 120 LD	10/06/93	T. VU
27384	03	REDRAW TO JEDEC FORMAT	11/18/94	

DWG #	PN64-1				PN80-1				PN100-1				PN120-1			
SYMBOL	JEDEC VARIATION BP			NOTE	JEDEC VARIATION BQ			NOTE	JEDEC VARIATION BR			NOTE	JEDEC VARIATION BS			NOTE
	MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX	
A	–	–	1.60		–	–	1.60		–	–	1.60		–	–	1.60	
A1	.05	.10	.15		.05	.10	.15		.05	.10	.15		.05	.10	.15	
A2	1.35	1.40	1.45		1.35	1.40	1.45		1.35	1.40	1.45		1.35	1.40	1.45	
D	16.00 BSC			4	16.00 BSC			4	16.00 BSC			4	16.00 BSC			4
D1	14.00 BSC			5,2	14.00 BSC			5,2	14.00 BSC			5,2	14.00 BSC			5,2
E	16.00 BSC			4	16.00 BSC			4	16.00 BSC			4	16.00 BSC			4
E1	14.00 BSC			5,2	14.00 BSC			5,2	14.00 BSC			5,2	14.00 BSC			5,2
N	64				80				100				120			
e	.80 BSC				.65 BSC				.50 BSC				.40 BSC			
b	.30	.37	.45	7	.22	.32	.38	7	.17	.22	.27	7	.13	.18	.23	7
b1	.30	.35	.40		.22	.30	.33		.17	.20	.23		.13	.16	.19	
ccc	–	–	.10		–	–	.10		–	–	.08		–	–	.08	
ddd	–	–	.20		–	–	.13		–	–	.08		–	–	.07	

LAND PATTERN DIMENSIONS



	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
P	16.80	17.00	16.80	17.00	16.80	17.00	16.80	17.00
P1	13.80	14.00	13.80	14.00	13.80	14.00	13.80	14.00
P2	12.00 BSC		12.35 BSC		12.00 BSC		11.60 BSC	
X	.40	.60	.30	.50	.30	.40	.20	.30
e	.80 BSC		.65 BSC		.50 BSC		.40 BSC	
N	64		80		100		120	

NOTES:

1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982

2 TOP PACKAGE MAY BE SMALLER THAN BOTTOM PACKAGE BY .15 mm

3 DATUMS A-B AND -D- TO BE DETERMINED AT DATUM PLANE -H-

4 DIMENSIONS D AND E ARE TO BE DETERMINED AT SEATING PLANE -C-

5 DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS .25 mm PER SIDE. D1 AND E1 ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH

6 DETAILS OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED

7 DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

8 EXACT SHAPE OF EACH CORNER IS OPTIONAL

9 THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP

10 ALL DIMENSIONS ARE IN MILLIMETERS

11 THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-136, VARIATION BP, BQ, BR & BS

TOLERANCES UNLESS SPECIFIED	
DECIMAL	ANGULAR
XX±	±
XXX±	
XXXX±	

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FAX: (408) 492-8674 TWX: 910-338-2070

APPROVALS	DATE
DRAWN AA	03/12/92
CHECKED	

TITLE PN PACKAGE OUTLINE
14.0 X 14.0 X 1.4 mm TQFP
1.00/.10 FORM

SIZE	DRAWING No.	REV
C	PSC-4036	03

DO NOT SCALE DRAWING