Integrated Device Technology, Inc.

CMOS STATIC RAM 64K (4K x 16-BIT) REGISTERED RAM w/SPC™

IDT 71502S
IDT 71502L

FEATURES:

- 4K x 16 RAM with registered outputs, serial or parallel load and readback capability in only 48 pins
- Serial Protocol Channel allows serial load and readback of RAM over a 4-wire channel
- RAM address counter speeds RAM load and readback
- Outputs may be programmed to be registered or non-registered in groups of 8 bits
- Initialize register allows initial microword selection
- Synchronous and asynchronous output enables allow for depth expansion and bus driving
- Programmable chip selects enable depth & width expansion without any external decode logic
- Breakpoint comparator supports system diagnostics
- Parity check on outputs for high reliability designs
- High-speed (address set-up before clock)
  - Military: 35/45/55ns (max.)
  - Commercial: 25/35/45ns (max.)
- Low-power consumption
  - IDT71502S - Active: 750mW (typ.)
  - IDT71502L - Active: 600mW (typ.)
- Input and output directly TTL-compatible
- Standard 48-pin DIP, 48-pin LCC and 52-pin PLCC.
- Military product 100% compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT71502 Registered RAM is a 65,536 bits high speed static RAM organized as 4K x 16, with a high speed register at the RAM outputs and serial load and readback capability using the IDT Serial Protocol Channel, SPC™.

This device is the first in a family of multifeatured RAM's with a built-in Serial Protocol Channel SPC™ letting the user set the best configuration for his system:

- SELF-ADDRESSING RAM
- WRITABLE CONTROL STORE
- LOGIC ANALYZER/RECORDER

The 71502 is fabricated using IDT's high-performance, high-reliability technology—CEMOS™. This technology gives the 71502 the combination of low power, high speed, and high density that makes it a cost effective solution.

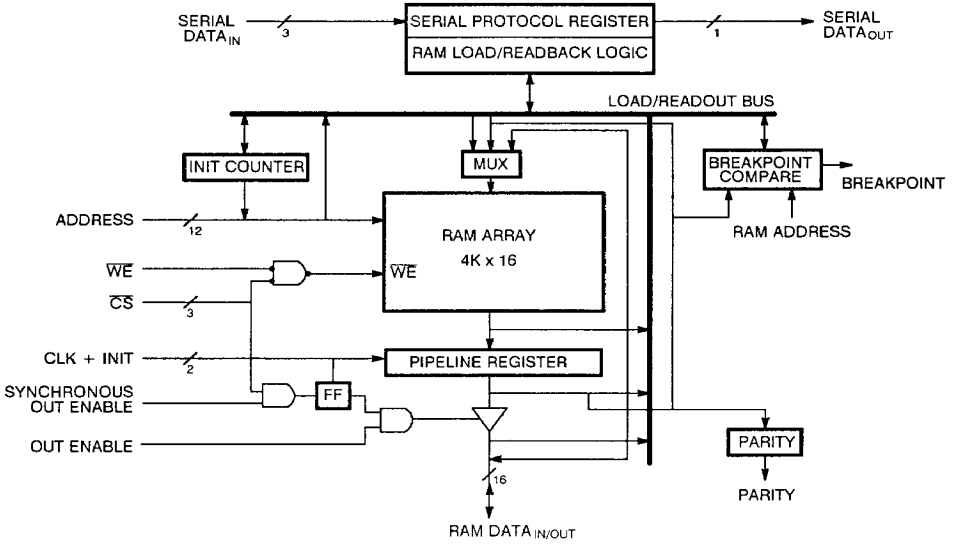
The IDT71502 is available with address set up before clock times as fast as 25ns. These times are available with a maximum power consumption of only 1.6W.

All inputs and outputs of the IDT71502 are TTL-compatible, and the device operates from a single 5V supply. Fully static, asynchronous circuitry is used, requiring no clocks (with the exception of the register clock) or refreshing for operation.

The IDT71502 is packaged in plastic and ceramic versions of either a 48-pin, 600 mil DIP; a 48-pin leadless chip carrier, or a 52-pin plastic leadless chip carrier providing high board level packing densities.

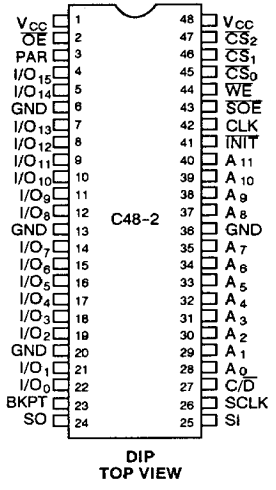
The IDT71502 is 100% processed in compliance to the test methods of MIL-STD-883, Method 5004.

FUNCTIONAL BLOCK DIAGRAM



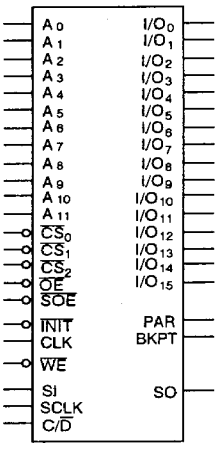
CEMOS is a trademark of Integrated Device Technology, Inc.

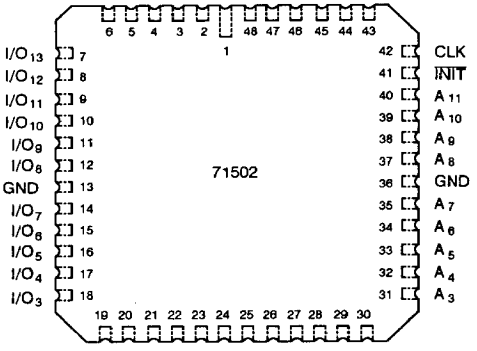
PIN CONFIGURATION



DIP
TOP VIEW

LOGIC SYMBOL



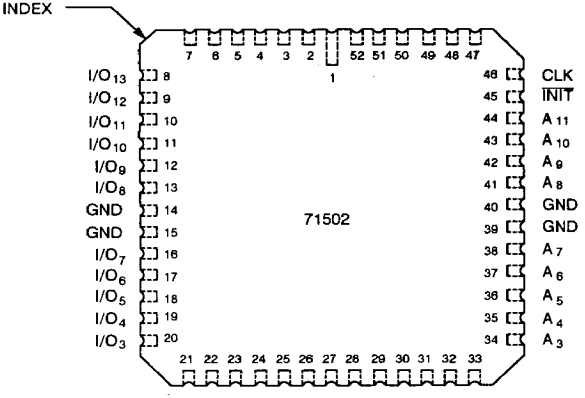


LCC PINOUT
TOP VIEW

PIN NAMES

NAME	FUNCTION
A_{0-11}	Address
I/O_{0-15}	Data Input/Output
$\overline{CS}_{0-2}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
$\overline{SOE}$	Synchronous Output Enable
CLK	Clock (to register)
$\overline{INIT}$	Initialize
BKPT	Breakpoint Detect
PAR	Parity
SI	SPC Serial $DATA_{IN}$ (1)
SO	SPC Serial $DATA_{OUT}$ (1)
SCLK	SPC Clock (1)
C/$\overline{D}$	SPC Command/$\overline{Data}$ (1)
GND	Ground
V_{CC}	Power

NOTE:
1. The Serial Protocol Channel (SPC) is discussed at length in IDT Application Note 16.



PLCC PINOUT
TOP VIEW

7

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (1) (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE:

1. This parameter is determined by device characterization but is not production tested.

TRUTH TABLE - READ/WRITE OPERATIONS STANDARD PIPELINED MODE

MODE	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{SOE}$	CLK	I/O OPERATION
Deselected	H	X	L	X	↓	High Z
Read	L	H	H	X	X	High Z
Read	L	H	L	H	↓	High Z
Read	L	H	L	L	↓	$DATA_{OUT}$ @ Address
Write	L	L	X	X	X	$DATA_{IN}$ @ Address

TRUTH TABLE - SPC OPERATIONS

MODE	C/$\overline{D}$	SCLK	FUNCTION
Command	H	↓	Shift bit into command register
Data	L	↓	Shift bit into data register
Execute	↓	↓	Execute command during time between C/$\overline{D}$ and SCLK

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V

NOTE:

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITIONS		IDT71502S MIN.	IDT71502S TYP.(1)	IDT71502S MAX.	IDT71502L MIN.	IDT71502L TYP.(1)	IDT71502L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
V_{OL}	Output Low Voltage(2)	I_{OL} = 16mA, V_{CC} = Min.		–	–	0.5	–	–	0.5	V
V_{OH}	Output High Voltage(2)	I_{OH} = -8mA, V_{CC} = Min.		2.4	–	–	2.4	–	–	V
V_{OL}	Output Low Voltage, BKPT	I_{OL} = 24mA, V_{CC} = Min.		–	–	0.5	–	–	0.5	V

NOTES:
1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.
2. All outputs except BKPT, which is open drain.

DC ELECTRICAL CHARACTERISTICS (1)

V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	POWER	IDT71502S25(2, 4) IDT71502L25(2, 4) COM'L.	IDT71502S35(4) IDT71502L35(4) COM'L.	IDT71502S35(4) IDT71502L35(4) MIL.	IDT71502S45(4) IDT71502L45(4) COM'L.	IDT71502S45(4) IDT71502L45(4) MIL.	IDT71502S55(3, 4) IDT71502L55(3, 4) COM'L.	IDT71502S55(3, 4) IDT71502L55(3, 4) MIL.	UNIT
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = 0	S	155	155	170	155	170	155	170	mA
		L	135	135	150	135	150	135	150	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX} = 1/TRC	S	280	255	270	230	245	220	235	mA
		L	250	225	240	200	215	190	205	

NOTES:
1. All values are guaranteed maximums.
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. Pipelined address access set-up time.

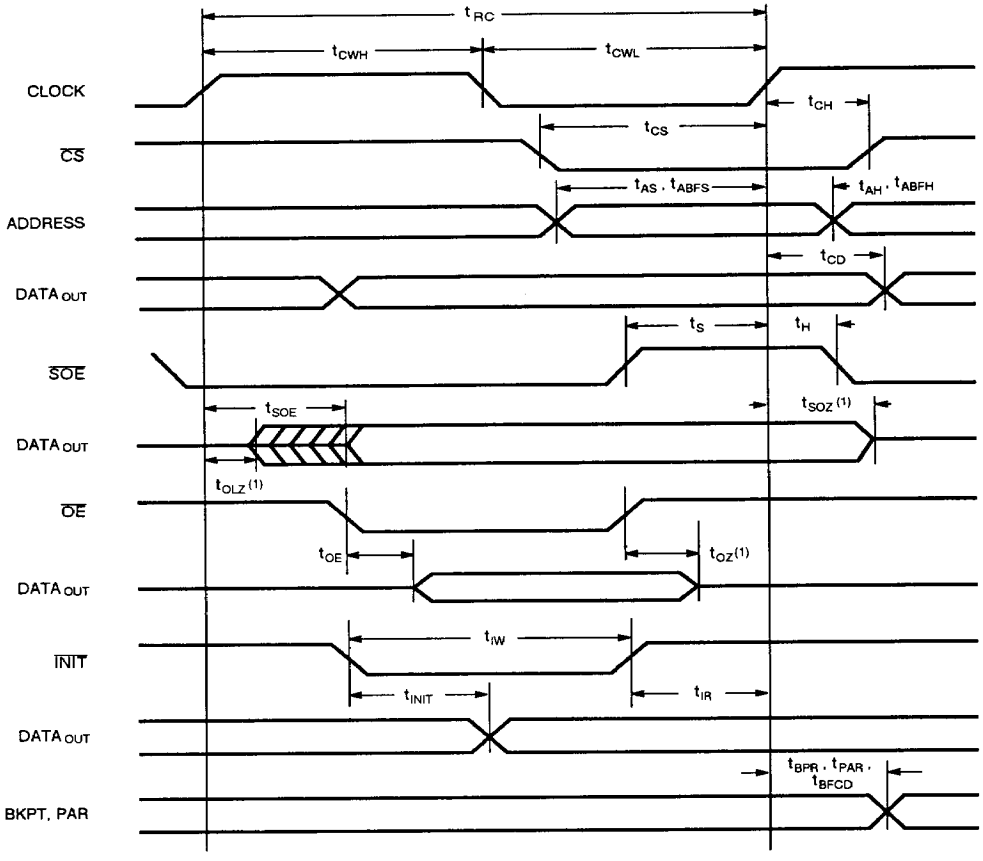
7

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	IDT71502S25[1,4] IDT71502L25[1,4] MIN.	MAX.	IDT71502S35[4] IDT71502L35[4] MIN.	MAX.	IDT71502S45[4] IDT71502L45[4] MIN.	MAX.	IDT71502S55[2,4] IDT71502L55[2,4] MIN.	MAX.	UNIT
READ CYCLE - PIPELINED										
t_{RC}	Read Cycle Time	40	–	50	–	65	–	80	–	ns
t_{AS}	Address Set-up Time	25	–	35	–	45	–	55	–	ns
t_{CS}	Chip Select Set-up Time	10	–	12	–	15	–	20	–	ns
t_S	Set-up Time: $\overline{SOE}$	10	–	12	–	15	–	20	–	ns
t_{AH}	Address Hold Time	0	–	0	–	0	–	0	–	ns
t_{CH}	Chip Select Hold Time	2	–	2	–	2	–	2	–	ns
t_H	Hold Time: $\overline{SOE}$	2	–	2	–	2	–	2	–	ns
t_{CD}	Clock to Output Delay	–	12	–	15	–	20	–	25	ns
t_{CWH}	Clock Width, High	15	–	15	–	20	–	20	–	ns
t_{CWL}	Clock Width, Low	15	–	15	–	20	–	20	–	ns
t_{OE}	Asynchronous Output Enable To Data Valid Time	–	12	–	15	–	20	–	25	ns
t_{OZ}	Asynchronous Output Disable Time[3,5]	–	11	–	14	–	19	–	24	ns
t_{SOE}	Synchronous Output Enable To Data Valid Time	–	12	–	15	–	20	–	25	ns
t_{SOZ}	Synchronous Output Disable Time[3,5]	–	11	–	14	–	19	–	24	ns
t_{INIT}	Initialize to Output Delay	–	45	–	50	–	65	–	80	ns
t_{IR}	Initialize Recovery Time	30	–	35	–	45	–	55	–	ns
t_{IW}	Initialize Pulse Width	30	–	35	–	45	–	55	–	ns
t_{PAR}	Parity Generation Time	–	30	–	35	–	45	–	55	ns
t_{BPR}	Breakpoint Delay From Register	–	35	–	35	–	45	–	55	ns
t_{BPA}	Breakpoint Delay From Address	–	35	–	35	–	45	–	55	ns
t_{ABFS}	Address to BKPT FF Set-up	30	–	35	–	40	–	50	–	ns
t_{ABFH}	Address to BKPT FF Hold	0	–	0	–	0	–	0	–	ns
t_{BFCD}	BKPT FF Clock to Data	–	16	–	20	–	25	–	30	ns
READ CYCLE - NON-PIPELINED										
t_{AAN}	Address Access Time	–	30	–	35	–	65	–	80	ns
t_{OLZ}	Asynchronous Output Enable Time[3,5]	2	–	2	–	2	–	2	–	ns
t_{SOEN}	Synchronous Output Enable To Data Valid Time	–	12	–	15	–	20	–	25	ns
t_{CAN}	Chip Select Access Time	–	15	–	20	–	30	–	35	ns
t_{ASPN}	Address Set-up Parity Time	40	–	50	–	65	–	80	–	ns
t_{AABN}	Address Access to Breakpoint	–	55	–	65	–	80	–	95	ns
t_{AABFS}	Address Access to BKPT FF Set-up	40	–	50	–	65	–	80	–	ns
t_{AABFH}	Address Access to BKPT FF Hold	0	–	0	–	0	–	0	–	ns
t_{PFCD}	Parity Flip-Flop Clock to data	–	12	–	15	–	20	–	25	ns

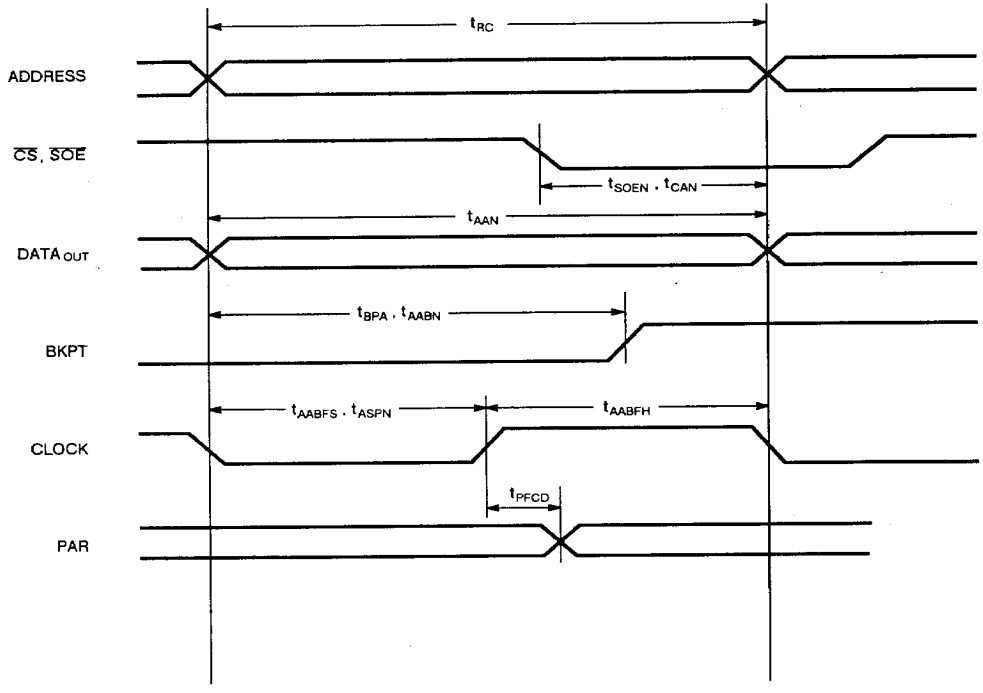
NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.
4. Pipelined address access set-up time.
5. Transition is measured ±500mW from steady state with 5pF load (including scope and jig).

TIMING WAVEFORM OF READ CYCLE NO. 1



NOTE:
1. Transition is measured ±500mV from steady state with 5pF load (including scope and jig).

TIMING WAVEFORM OF READ CYCLE NO. 2 – NON-PIPELINED



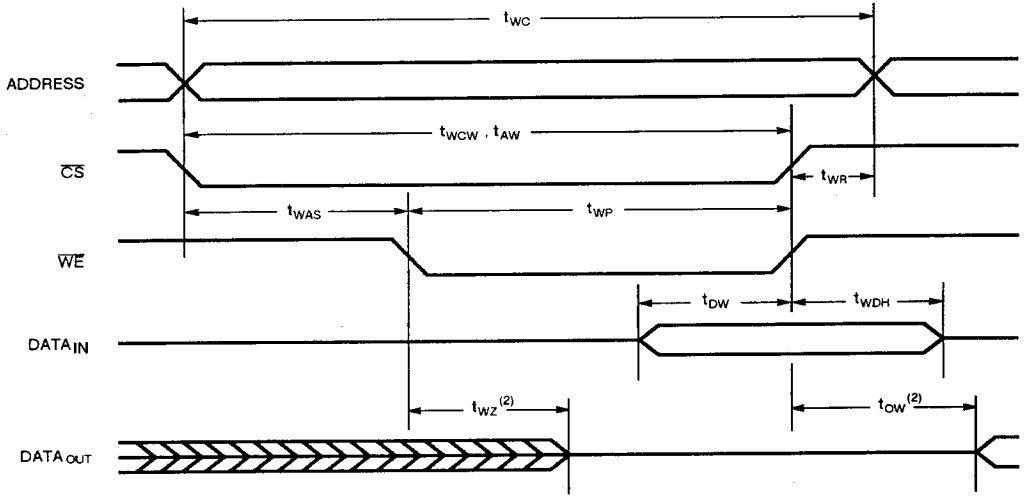
NOTE:
1. Transition is measured ±500mV from steady state with 5pF load (including scope and jig).

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	IDT71502S25 (1, 4) IDT71502L25 (1, 4) MIN.	MAX.	IDT71502S35 (4) IDT71502L35 (4) MIN.	MAX.	IDT71502S45 (4) IDT71502L45 (4) MIN.	MAX.	IDT71502S55 (2, 4) IDT71502L55 (2, 4) MIN.	MAX.	UNIT
RAM WRITE CYCLE										
t_{WC}	RAM Write Cycle Time	40	–	50	–	65	–	80	–	ns
t_{WAS}	RAM Write Address Set-up Time	0	–	0	–	0	–	0	–	ns
t_{WP}	RAM Write Pulse Width (5)	20	–	25	–	35	–	45	–	ns
t_{DW}	RAM Write Data Set-up Before End Of Write	15	–	17	–	25	–	30	–	ns
t_{AW}	Address Valid to End of Write	25	–	30	–	50	–	60	–	ns
t_{WCW}	Chip Select To End Of Write	25	–	30	–	50	–	60	–	ns
t_{WDH}	RAM Write Data Hold Time	0	–	0	–	0	–	0	–	ns
t_{WR}	Write Recovery Time	5	–	5	–	5	–	5	–	ns
t_{WZ}	Write Enable to Output Hi-Z (3, 6)	–	15	–	15	–	20	–	20	ns
t_{OW}	Output Active from End of Write (3, 6)	5	–	5	–	5	–	5	–	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter is guaranteed but not tested.
4. Pipelined address access set-up time.
5. $\overline{OE}$ = V_{IH}.
6. Transition is measured ±500mV from steady state with 5pF load (including scope and jig).

TIMING WAVEFORM OF WRITE CYCLE (1)



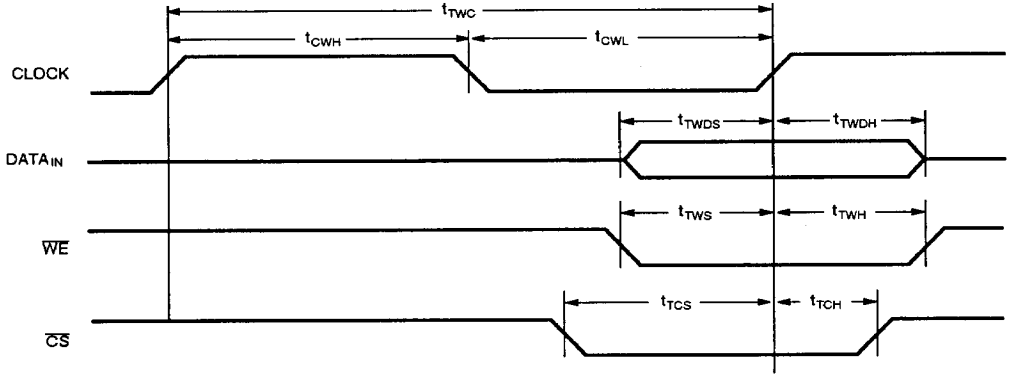
NOTE:
1. A write occurs during the overlap of both $\overline{CS}$ and $\overline{WE}$ low.
2. Transition is measured ±500mV from steady state with 5pF load (including scope and jig).

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	IDT71502S25[1,4] IDT71502L25[1,4] MIN.	MAX.	IDT71502S35[4] IDT71502L35[4] MIN.	MAX.	IDT71502S45[4] IDT71502L45[4] MIN.	MAX.	IDT71502S55[2,4] IDT71502L55[2,4] MIN.	MAX.	UNIT
TRACE WRITE CYCLE										
t_{TWC}	Trace Write Cycle Time	40	–	50	–	65	–	80	–	ns
t_{TWDS}	Trace Write Data Set-up Time	8	–	10	–	12	–	15	–	ns
t_{TWDH}	Trace Write Data Hold Time	2	–	2	–	2	–	2	–	ns
t_{TWS}	Trace Write Enable Set-up Time	8	–	10	–	12	–	15	–	ns
t_{TCS}	Trace Write Chip Select Set-up Time	8	–	10	–	12	–	15	–	ns
t_{TWH}	Trace Write Enable Hold Time	2	–	2	–	2	–	2	–	ns
t_{TCH}	Trace Write Chip Select Hold Time	2	–	2	–	2	–	2	–	ns

NOTES:
1. 0°C to +70°C temperature range only.
2. −55°C to +125°C temperature range only.
3. This parameter is guaranteed but not tested.
4. Pipelined address access set-up time.

TIMING WAVEFORM OF TRACE WRITE CYCLE[1]



NOTE:
1. A write occurs if both $\overline{CS}$ and $\overline{WE}$ are low at the clock low-to-high transition

AC TEST CONDITIONS (Read and Write Cycles)

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

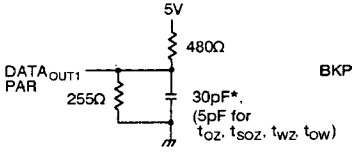


Figure 1. Output Load, Parity Output

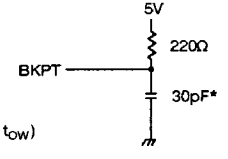


Figure 2. Output Load (for BKPT pin)

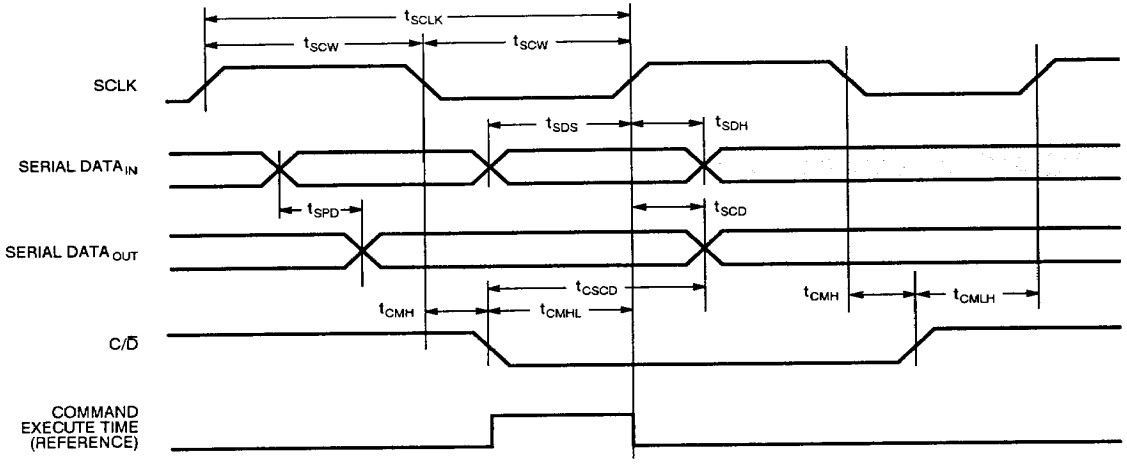
*Includes scope and jig.

SPC AC ELECTRICAL CHARACTERISTICS [1] V_{CC} = 5V ±10%, All Temperature Ranges

SYMBOL	PARAMETER	IDT71502S/L[1] MIN.	MAX.	UNIT
t_{SCLK}	SCLK Period	100	–	ns
t_{SCW}	SCLK Pulse Width	40	–	ns
t_{SDS}	Serial Data Set-up Time	20	–	ns
t_{SDH}	Serial Data Hold Time	2	–	ns
t_{SCD}	Clock to serial Data Output Delay	–	30	ns
t_{SPD}	Serial Data-In-to-Out Delay, Stub Mode	–	20	ns
t_{CMLH}	Command/Data Set-up Time, Low-to-High[2]	20	–	ns
t_{CMHL}	Command Set-up Time, High-to-Low (Execution Time)[2]	35	–	ns
t_{CMH}	Command/Data Hold Time[2]	5	–	ns
t_{CSCD}	Command/Data to Serial Data Output Delay (1st Bit Only)	–	45	ns

NOTES:
1. These specifications apply to all speed grades of the product.
2. C/$\overline{D}$ cannot change while SCLK is high.

TIMING WAVEFORM OF SPC CHANNEL



AC TEST CONDITIONS (SPC)

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 3

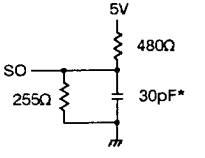
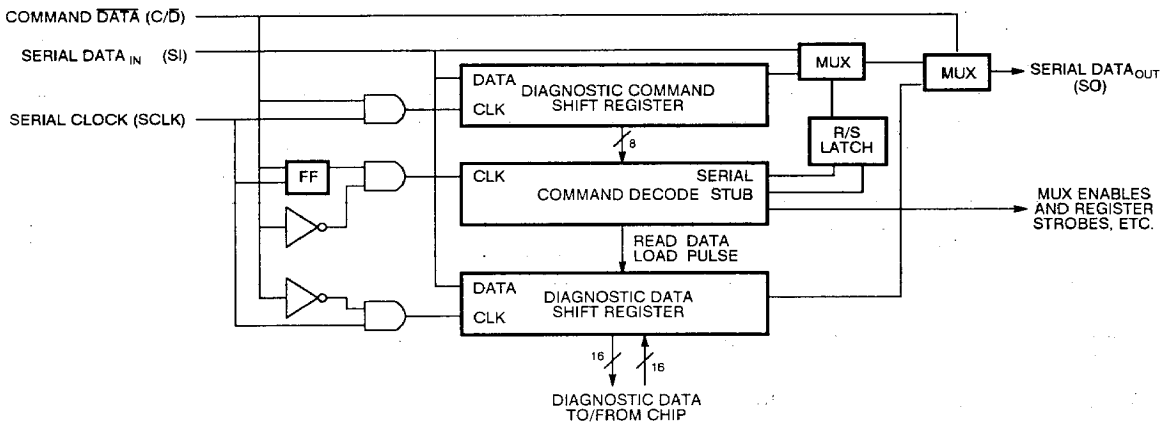


Figure 3. Output Load for Serial Output

*Includes scope and jig.

SPC FUNCTIONAL BLOCK DIAGRAM



SPC COMMAND FORMAT

7 — 4	3 — 0
SPC Command Code 4 bits	SPC Register Code 4 bits

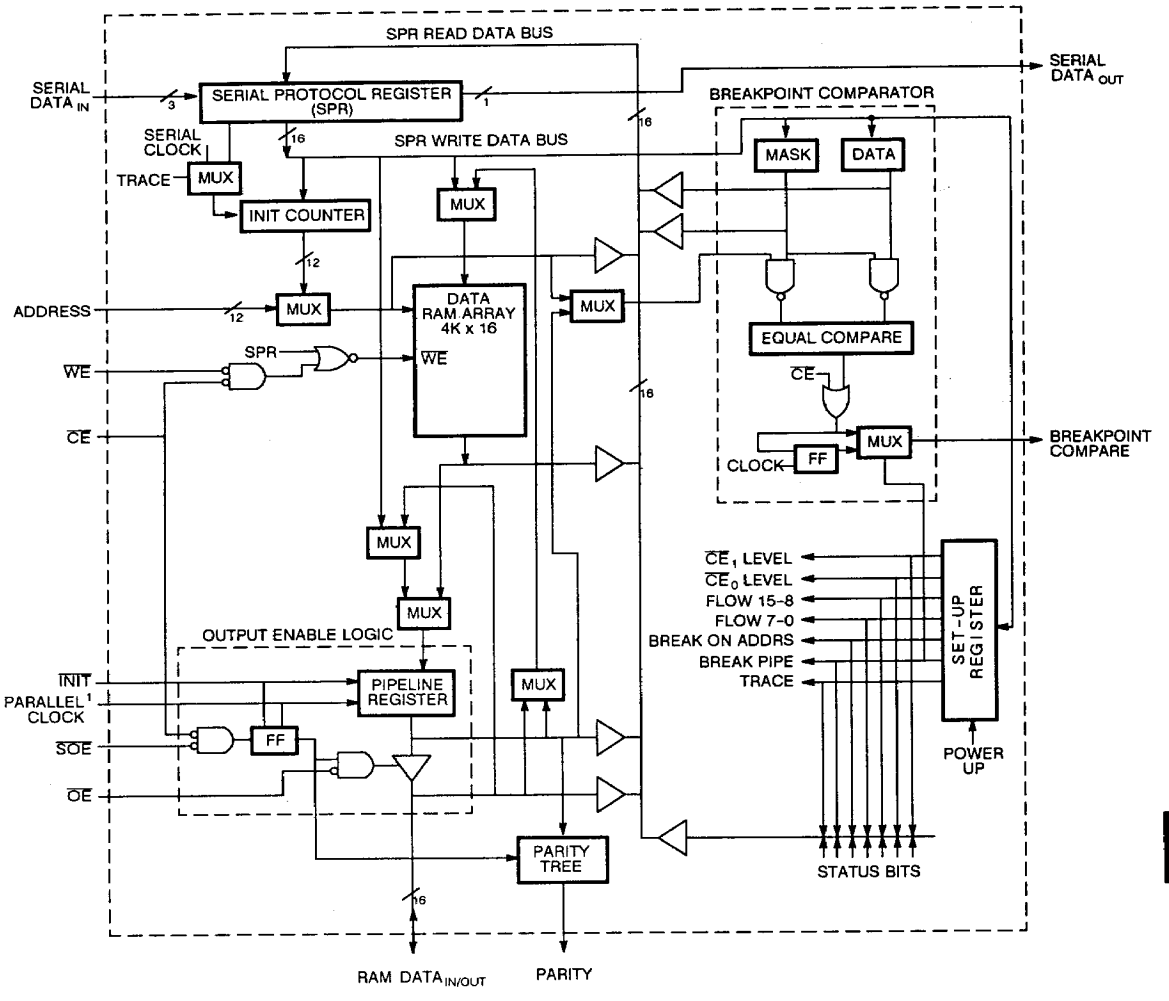
SPC COMMAND CODES

COMMAND CODE	READ/WRITE FUNCTION	ACTION	NOTES
0	Read	Read Register	Uses Register Select Field
1	Write	Write Register	Uses Register Select Field
2	Read	Read Register and Increment Initialize Counter	Serial RAM Read
3	Write	Write Register and Increment Initialize Counter	Serial RAM Write
4-C	–	Reserved (No-Op)	–
D	Write	Stub Diagnostic	Broadcast Commands
E	Write	Serial Diagnostic	Serial Commands
F	–	No-Op	Guaranteed No-Op

SPC REGISTER CODES

REGISTER CODE	READ/WRITE FUNCTION	REGISTER	NOTES
0	R/W	Initialize Counter	–
1	R/W	RAM Output (or Input if reading)	–
2	R/W	Pipeline Register	–
3	R/W	Break Mask Register	–
4	R/W	Break Data Register	–
5	R/W	Set-up + Status Register	Break Multiplexer, Trace Mode, etc.
6	Rd Only	I/O_{15} - I/O_0 (Data Pins)	Data Pins of Chip
7	Rd Only	RAM Address	Address Going into RAM
8-F	–	Reserved (unused)	–

REGISTERED RAM DATA FLOW BLOCK DIAGRAM



NOTE:

1. SPC and RAM accesses are mutually exclusive. Hence, these two operations must not occur simultaneously. During SPC accesses, the content of the pipeline register will change if the parallel clock is active.

SET-UP REGISTER FORMAT

BIT	NAME	TYPE [1]	FUNCTION	POWER-UP VALUE
15	CE	RO	Chip Enable State: NOR of All Chip Enable Pins	0
14	$\overline{SOE}$ FF	RO	$\overline{SOE}$ FF State: 1 = Output Enabled, 0 = Output Disabled	0
13	$\overline{SOE}$ Pin	RO	$\overline{SOE}$ Pin State: 1 = High, 0 = Low	0
12	$\overline{OE}$ Pin	RO	$\overline{OE}$ Pin State: 1 = High, 0 = Low	0
11	$\overline{WE}$ Pin	RO	$\overline{WE}$ Pin State: 1 = High, 0 = Low	0
10	$\overline{INIT}$ Pin	RO	$\overline{INIT}$ Pin State: 1 = High, 0 = Low	0
9	BP Compare	RO	Breakpoint Comparator Output: 1 = Compare Valid	0
8	BP Pin	RO	BP Pin State: 1 = High, 0 = Low	0
7	$\overline{CS}_1$ Level	R/W	0 = $\overline{CS}_1$ is Low Active; 1 = CS_1 is High Active	0
6	$\overline{CS}_0$ Level	R/W	0 = $\overline{CS}_0$ is Low Active; 1 = CS_0 is High Active	0
5	Non-Reg High	R/W	Set Pipeline Register Bits 15-8 to Flow-Through Mode	0
4	Non-Reg Low	R/W	Set Pipeline Register Bits 7-0 to Flow-Through Mode	0
3	–	–	(Unused)	0
2	BC Address	R/W	0 = Breakpoint on Pipeline Register Output, 1 = Breakpoint on RAM Address Inputs	0
1	BC Pipelined	R/W	Set Breakpoint Output MUX for Pipeline FF Output	0
0	Trace Mode	R/W	Set for Trace Mode: I/O_{15-0} to Pipeline Register, Pipeline Register to RAM, Initialize Counter as Address, Write with Clock Pulse	0

NOTE:
1. RO means Read Only. R/W means Read/Write.

GENERAL DESCRIPTION

The IDT71502 Registered RAM consists of a 4K x 16-bit RAM plus a 16-bit pipeline register and is designed for microcode writable control store use. A serial shift register system, the Serial Protocol Channel (SPC), is included on-chip for serial load and read-back of the RAM data. A RAM address counter is also provided to speed up RAM load and read-back. The SPC serial shift register is also configured to be used as a diagnostic register. The shift register can read all status conditions on the chip such as the RAM output, pipeline register output, data output pin state and RAM load/read counter value. A breakpoint comparator is included to support the diagnostic function. This breakpoint comparator can be used to detect a particular bit pattern in the RAM address or pipeline register outputs.

The IDT71502 Registered RAM includes features to support control store applications. These include synchronous output enable and an initialize register for selecting the initial value of the pipeline register. A parity output is provided which indicates the parity of the contents of the pipeline register. The parity output can be used to provide parity check control for high-reliability systems.

The IDT71502 Registered RAM can also be used as a trace RAM for recording external data. In this mode, the data I/O pins are inputs and data is clocked into the RAM using the Initialize register as the address counter. The Trace mode, in combination with the breakpoint comparator, allows the IDT71502 Registered RAM to be used as a one-chip logic analyzer.

RAM Operation

After power up, and in its typical operating mode, the IDT71502 Registered RAM is set for pipelined read and direct (non-pipelined) write. Data may be directly written into the RAM by driving the address and data inputs and strobing the Write Enable input. Data is read from the RAM by driving the address lines and clocking the pipeline register.

The RAM may also be read and written by the Serial Protocol Channel (SPC). This is the typical path for loading the RAM after power up. SPC and RAM accesses are mutually exclusive. Hence, these two operations must not occur simultaneously. During SPC accesses, the content of the pipeline register will change if the parallel clock is active.

Serial Protocol Channel

The Serial Protocol Channel (SPC) logic consists of a 16-bit data shift register, an 8-bit command register and clock logic consisting of gates and a flip-flop. A block diagram of the command decode logic is shown for reference. The command decode logic decodes and executes the command in the command shift register using the clock from the clock logic. The command is divided into two four-bit fields. The most significant four bits of the command register define the command to be executed: read, write, etc. The least significant four bits define the register to be read or written. (NOTE: The data to the SPC is shifted in LSB first.)

The SPC is connected to the outside world through four wires. These wires consist of serial data in and out, a shift clock and a command/$\overline{\text{data}}$ line. When the command/$\overline{\text{data}}$ line is high, commands are shifted from the serial data in to the command register by the clock. When the command/$\overline{\text{data}}$ line is low, data is shifted into the data shift register by the clock. When the command/data line transitions from high (command) to low (data), a clock pulse is generated internally to the command decode logic. This pulse lasts from the beginning of the high-to-low transition to the next serial clock pulse and is used to execute the command in the command register.

Two of the defined commands are Serial and Stub. These commands control a latch which determines the source of the serial data out in the command mode. The Serial command causes the data output to be taken from the last stage of the command shift register. This is the normal operating mode, where all the shift registers in a system are connected into one long shift register. The SPC logic in the IDT71502 is automatically set to the Serial mode by power up. The Stub command sets the latch and causes the serial output data to be taken from the serial input. In this mode, the serial data is passed directly from one chip to the next so that all command registers have the same data at their serial inputs. This allows a broadcast mode where all command registers in a system can be loaded with the same command at the same time.

RAM Load/Readback Logic

The RAM write pulse is generated by an internal one-shot triggered by the clock. Data is written into the RAM immediately following pipeline register load and the Initialize Counter is incremented by the trailing edge of the write pulse. Using an internally generated write pulse makes RAM writing independent of clock high and low times. A timing diagram of the RAM clocking is shown in the Trace Mode Clock Timing Diagram (Figure 5).

A detailed block diagram of the IDT71502 Registered RAM, showing the various internal registers and the load and readback paths, is shown in the Registered RAM Data Flow Block Diagram. In addition to the logic shown in the Functional Block Diagram on the first page of the data sheet, there is an Initialize Counter for loading and initializing the RAM, Break Data and Mask registers for the Breakpoint Comparator and multiplexers at the input to the Pipeline register for allowing data from the data I/O pins to be clocked into the Pipeline register in the Trace mode before being written into the RAM. The data flow block diagram also shows the various multiplexers for routing data for breakpoint and readback use.

Initialize Counter

The Initialize Counter provides the initial address to the RAM after reset of the part. A pulse applied to the Initialize pin causes the Initialize Counter to be gated to the RAM address and the RAM data to be preset into the pipeline register. This provides an initial value in the pipeline register before the first clock pulse arrives. The Initialize Counter can be reset to zero at power up of the chip and can be loaded with a value other than zero by the SPC. Once loaded with a value by the SPC, this value is used in further chip reset operations.

Set-up Register

The Set-up Register is a 16-bit register used to set the chip operating mode and to read back chip operating status conditions. A command word written into the Set-up Register sets 7 latches which control the chip operating conditions. Reading the Set-up Register provides the current status of these 7 latches and various other signals on the chip. At power up, the 7 latches are cleared to zero and the Initialize counter is cleared to zero. The format of the Set-up Register is shown in the Set-up Register Format table.

The Set-up Register has 7 latches which determine the operating mode of the chip. These are $\overline{CS}_1$, $\overline{CS}_0$, Non-Reg High, Non-Reg Low, BC RAM, Break Pipe and Trace. The $\overline{CS}_1$ and $\overline{CS}_0$ bits determine the polarity of the $\overline{CS}_1$ and $\overline{CS}_0$ chip enables. The Non-Reg High and Low bits set the upper and lower bytes of the Pipeline Register to a flow-through mode, respectively. The BC RAM bit determines the source of the data for breakpoint comparison, either the Pipeline Register or the RAM address. The Break Pipe latch switches the breakpoint pin multiplexer from the comparator to the buffer flip-flop. The trace latch sets the chip into the Trace mode.

7

Power Up State

Power up is defined as taking V_{CC} from below 1.0 volts to 5.0 volts nominal. This generates power up reset, an internal signal which resets several registers on the chip. After power up, the IDT71502 is in the following state:

- Set-up Register cleared to zero
- Initialize Counter cleared to zero
- Breakpoint Mask Register cleared to equal (Breakpoint output high)
- $\overline{SOE}$ Flip-Flop cleared to outputs off

Note that taking V_{CC} from 5.0 volts to 2.0 volts and back to 5.0 volts will not cause power up reset.

Set-up Register: Programmable Chip Enable

The chip enable function is programmable by bits in the Set-up Register. The logic for this is shown in Figure 1. The bits in the Set-up Register define the active state of each chip enable: high or low. This allows up to four RAMs to be cascaded in depth with no external decoders required (16K x 16 bits of RAM).

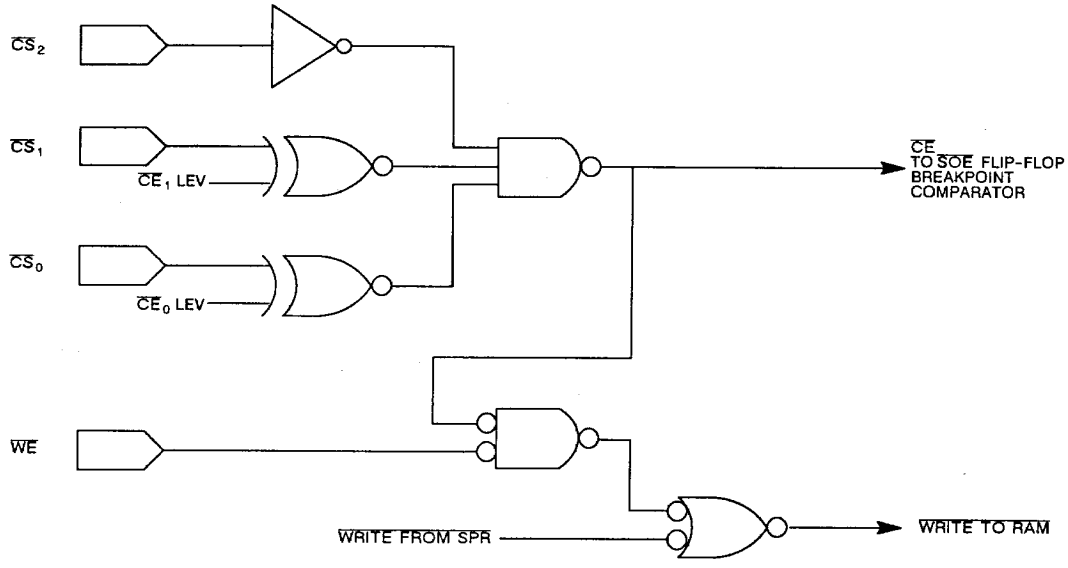


Figure 1. Chip Enable Logic Block Diagram

Set-up Register: Non-Registered Outputs

Two bits of the Set-up Register, Non-Reg Hi and Non-Reg Lo, can be set to cause the Pipeline Register bits 15-9 and 7-0, respectively, to be set to the flow-through mode. In the flow-through mode, both latches of the register are open and the register acts like a simple buffer with its output following its input. This allows the user to have some non-registered bits in microcode applications. The output circuit consisting of the Pipeline Register, the Synchronous Output Enable ($\overline{SOE}$), and the Output Enable ($\overline{OE}$), has some special logic to support this mode, as shown in Figure 2.

Also, activating the Initialize pin causes the Pipeline Register to be put in the flow-through mode. Figure 2 shows the Pipeline Register as two latches operated in the MASTER/SLAVE configuration. The clock input will cause the latch pair to work as a register. If the Initialize pin is activated, both registers will be placed in the flow-through mode by the OR gates. Also, if either Non-Reg bit is set, its corresponding 8-bit portion of the register will be placed in the flow-through mode.

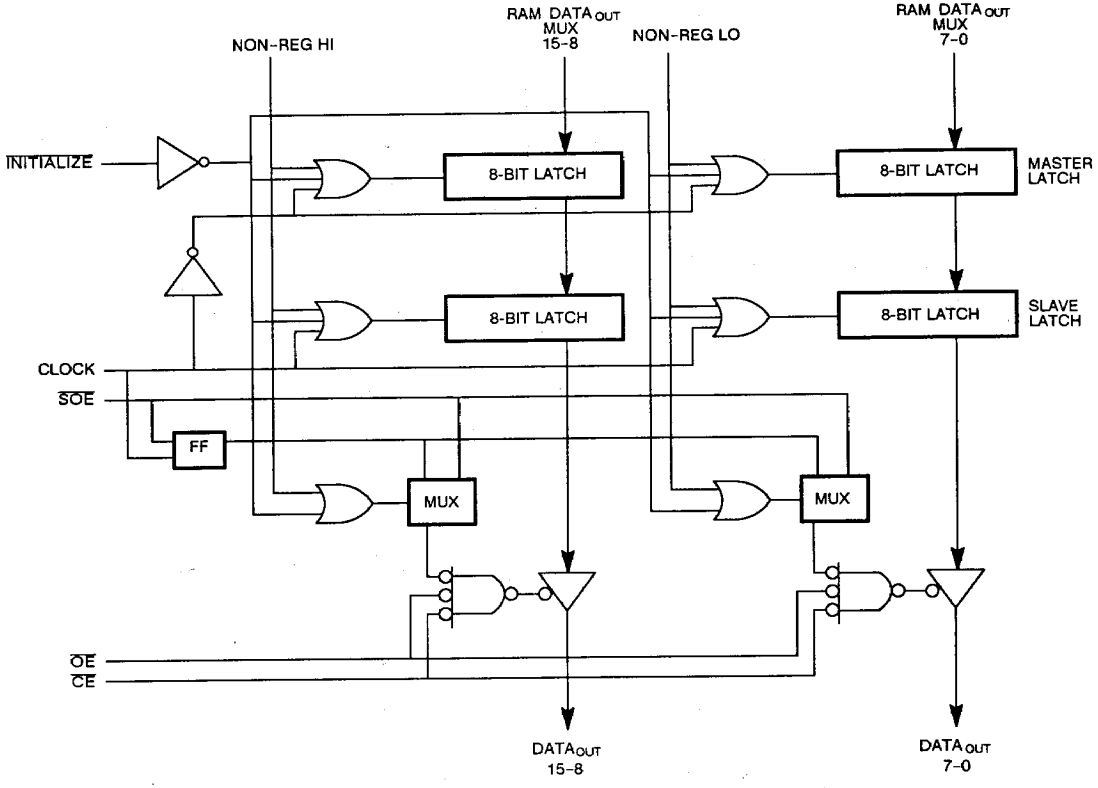


Figure 2. Output Logic Block Diagram

When in the flow-through mode, the output enable flip-flop for that half must also be in the flow-through mode for external chip expansion to work properly. A non-registered RAM bit must be enabled by a non-registered output enable, while a registered bit must be enabled by a synchronous output enable. This is done by using the non-registered bit to control a multiplexer which selects between the $\overline{SOE}$ flip-flop input and output as the source of the output enable.

Set-up Register: Breakpoint Comparator Control

The Breakpoint Comparator (BC) provides a masked 16-bit comparison of the various data paths that can be read by the SPC. It consists of an equal-comparator and the Break Data and Mask registers, as shown in Breakpoint Comparator Logic Block Diagram (Figure 3). The BC compares the data from the chip against the data in the Break Data Register and activates the Breakpoint Compare output if the two are equal. The Mask Register enables comparison: if a bit in the Mask Register is a one, comparison is enabled on the corresponding bit in the Break Data Register. If it is zero, the comparison on the that bit is disabled: i.e., forced to equal.

The Breakpoint output is an open drain type to allow width expansion of the Breakpoint Comparison. For example, if two IDT71502 chips have their breakpoint pins tied together to the same load resistor, both breakpoint comparators must be valid before the output can rise. The result is a 32-bit comparison.

A selectable flip-flop is provided for the Breakpoint Output. This allows pipeline registered bits, non-registered bits and address bits to be used in comparison with the same timing. Breakpoint comparison is commonly performed on the pipeline register outputs. These outputs are valid after the clock; i.e. for the current cycle. Address inputs and non-pipelined outputs are valid before the clock, representing address and data for the next cycle, respectively. If address or non-pipelined outputs are to be used in breakpoint comparison, a flip-flop delay must be added so that they will be valid after the clock in the same manner as pipelined bits. The selectable flip-flop provides this delay so that all breakpoint comparison outputs are valid in the current cycle.

The Breakpoint output driver is enabled by the $\overline{SOE}$ Flip-Flop to allow depth expansion of the comparison. $\overline{SOE}$ must be low prior to clock going high whether in pipelined mode or not.

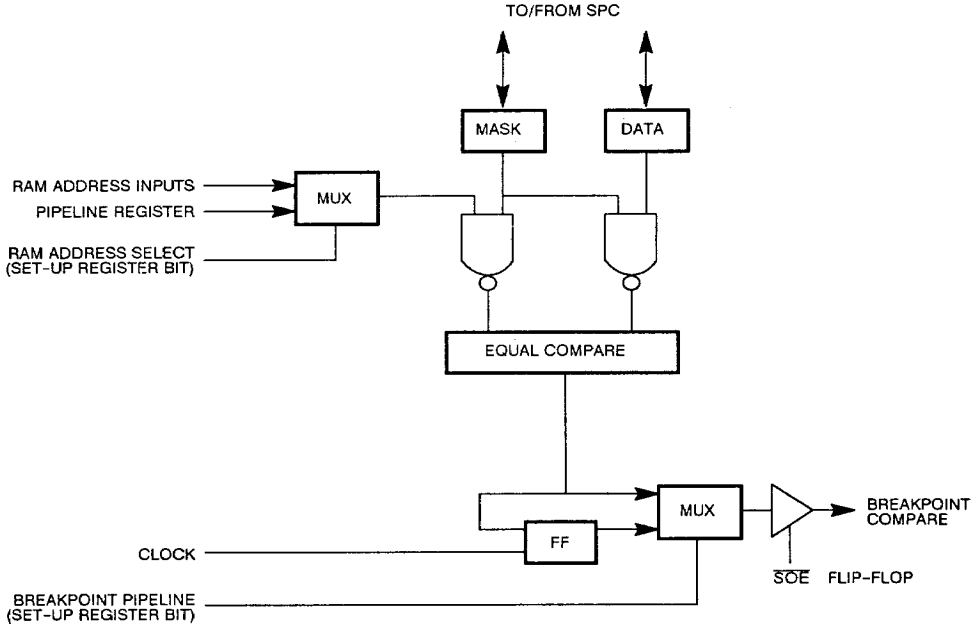


Figure 3. Breakpoint Comparator Logic Block Diagram

Set-up Register: Trace Mode Operation

When the trace bit in the Set-up Register is set, the chip is in the Trace mode. In this mode, data from the chip data pins, I/O_{15} - I/O_0, is written into sequential locations in the RAM . The address for the RAM comes from the Initialize Counter, which is incremented after each RAM write. The Trace mode is used to record external data events in the same manner as a logic analyzer. The Trace mode recording sequence is as follows:

1. Data from the I/O pins is written into the Pipeline Register by the clock.
2. Data in the Pipeline Register is written into the RAM by a one-shot driven by the trailing edge of the clock. The RAM address comes from the Initialize Counter.
3. The Initialize Counter is incremented by the trailing edge of the RAM write pulse.

Trace operation requires both $\overline{WE}$ and $\overline{CS}$ to be active. If either is inactive (high), the Initialize Register will not be incremented and data will not be written into the RAM. The Pipeline Register will be loaded, however. This allows the write enable to be used for skipping words. A timing diagram of this logic is shown in the Trace Mode Sequence Timing Diagram (Figure 4).

The RAM write pulse is generated by an internal one-shot triggered by the clock. Data is written into the RAM immediately following pipeline register load and the Initialize Counter is incremented by the trailing edge of the write pulse. Using an internally generated write pulse makes RAM writing independent of clock high and low times. A timing diagram of the RAM clocking is shown in the Trace Mode Clock Timing Diagram (Figure 5).

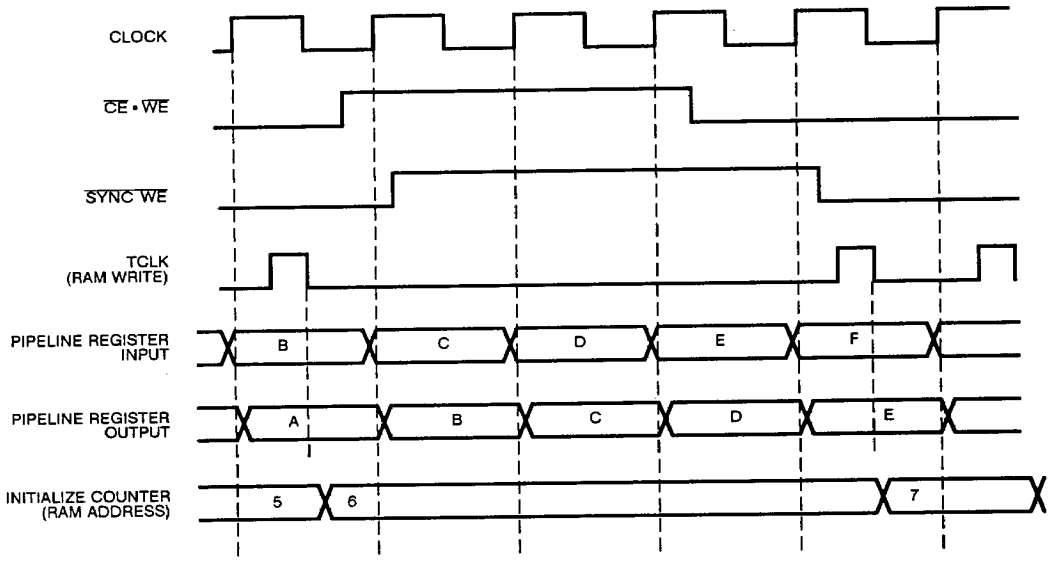


Figure 4. Trace Mode Sequence Timing Diagram

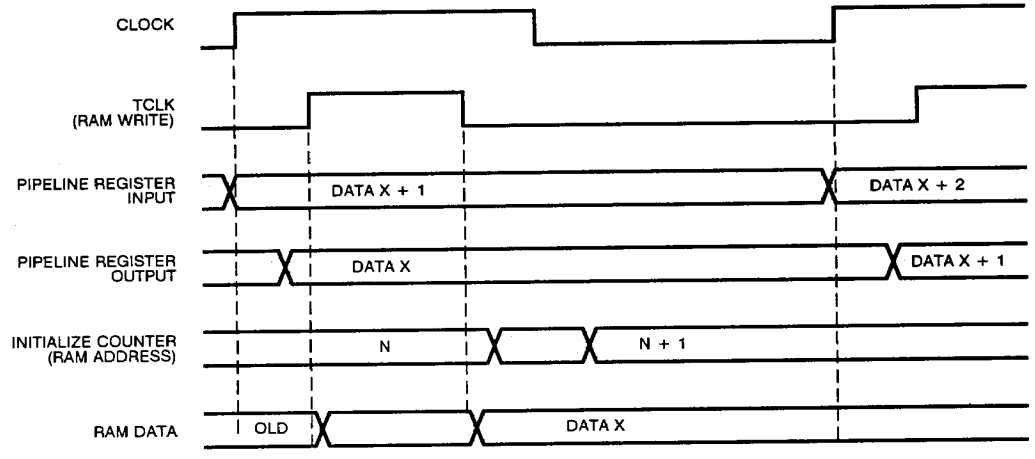


Figure 5. Trace Mode Clock Timing Diagram

Parity Output

The Parity Output pin is generated from a 16-bit parity tree, as shown in the Parity Tree Logic Block Diagram (Figure 6). Even parity is used. Parity is generated on the contents of the Pipeline Register. The parity output driver is three-state and is enabled by the $\overline{SOE}$ Flip-Flop to allow depth expansion of the parity output.

The Parity Output always reflects the parity of the registered value. Additional flip-flops and multiplexers are included in the parity tree to cover the case of non-registered outputs. If one or both bytes of the Pipeline Register are set to the Non-Registered mode, a flip-flop pipeline delay is added to the corresponding byte parity chain to make the result of that byte parity calculation the same as if the Pipeline Register was not in the Non-Pipelined mode. $\overline{SOE}$ must be low prior to the clock going high in pipelined or non-pipelined mode.

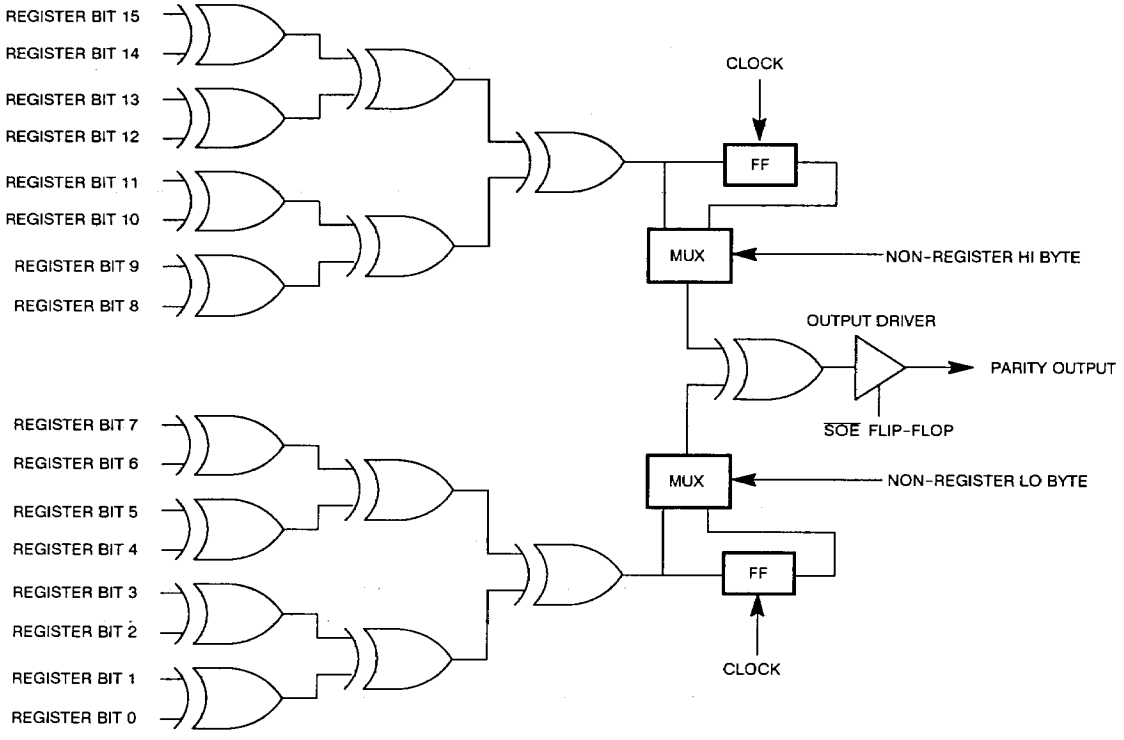


Figure 6. Parity Tree Logic Block Diagram

REGISTERED RAM APPLICATIONS

Using the Registered RAM in Writable Control Stores

The IDT71502 Registered RAM is designed expressly for efficient use in writable control stores. A simplified block diagram of a 16-bit microprogram-controlled system using the IDT71502 is shown in Writable Control Store Using Registered RAM (Figure 7). The system shown uses four IDT71502 Registered RAM chips to provide 4K x 64 bits of microcode writable control store.

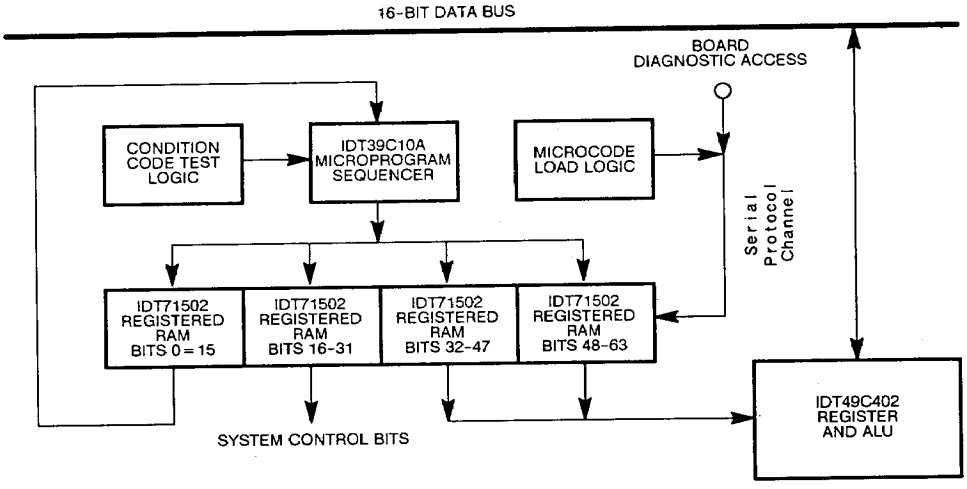


Figure 7. Writable Control Store Using Registered RAM

Using the Parity Output

The parity output can be used in conjunction with an additional IDT71502 Registered RAM to provide parity checking for control stores. This is shown in the Parity Check in a Writable Control Store System (Figure 8) block diagram. The parity output driver is gated by the $\overline{SOE}$ Flip-Flop. This allows simple depth expansion of the parity function by paralleling the parity outputs in the same manner as the data outputs, as shown in the Parity Check in a Depth Expanded Writable Control Store System (Figure 9) block diagram.

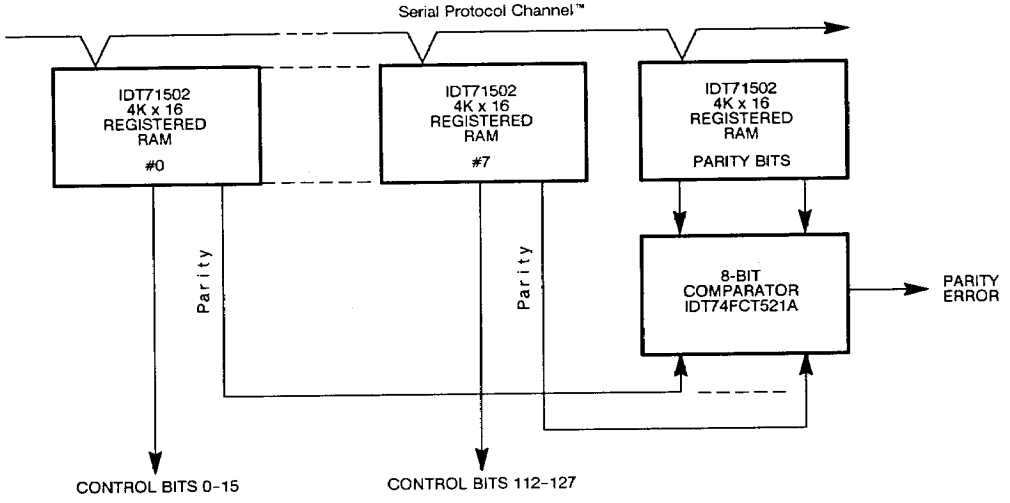


Figure 8. Parity Check in a Writable Control Store System

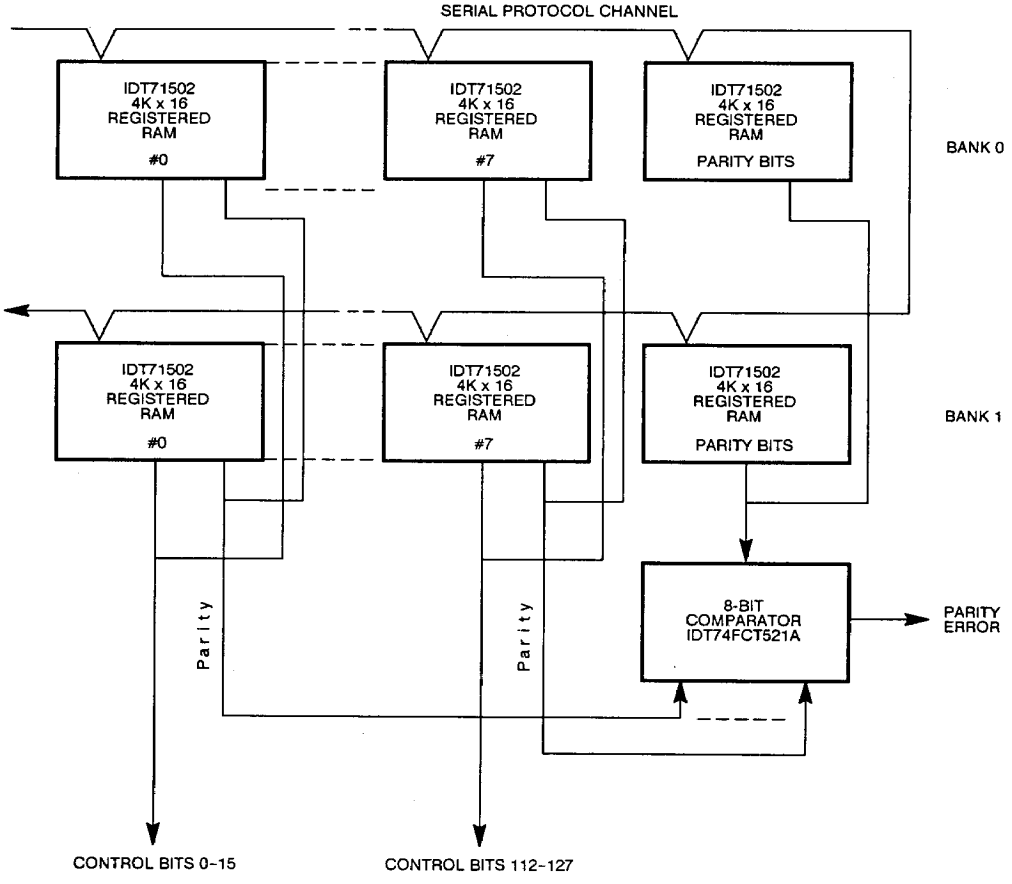


Figure 9. Parity Check in a Depth Expanded Writable Control Store System

Using Trace Mode as a Logic Analyzer

The Trace mode allows the IDT71502 to be used as an on-board logic analyzer for system diagnostics. It is particularly powerful when used in conjunction with the Breakpoint function. In the Trace mode, data is recorded in sequential locations in the RAM as controlled by the Trace Counter. Since the incoming data is clocked into the pipeline register, the set-up and hold times are short and compatible with capturing changing bus data, for example. A block diagram of a system with an IDT71502 used in the Trace mode is shown in Diagnostic Bus Monitoring Using Trace Mode (Figure 10).

The Breakpoint outputs from the IDT71502 devices in a system can be used to control the Trace mode writing. The Breakpoint outputs are open drain types which provide a wire-AND function when connected together to a single pull-up resistor. By tying the Breakpoint outputs for the writable control store RAMs and the trace RAM, a breakpoint comparison can be made over the full microcode word plus the data bus contents. This comparison can be used to enable the trace write so that only data which occurred at the Breakpoint times is recorded. This allows recording the data that was on the bus during each instance of an I/O write, for example.

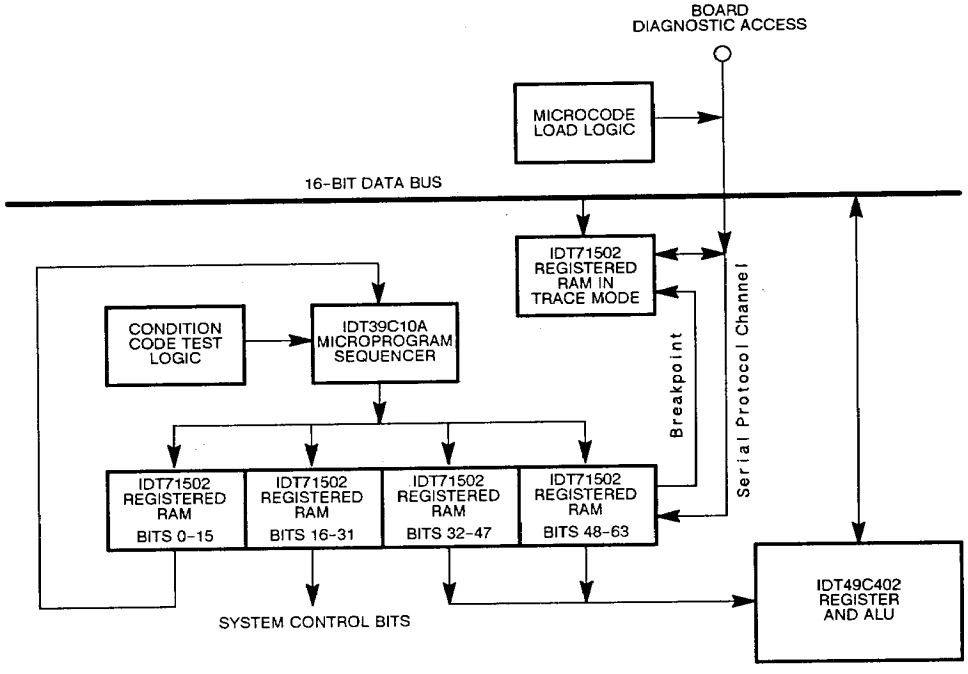


Figure 10. Diagnostic Bus Monitoring Using Trace Mode

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Serial Loading of the IDT71502 Using the SPC

In order to use the IDT71502 in writable control store applications, it must be loaded with the microprogram before use. This is done using the Serial Protocol Channel (SPC). Loading the RAM over the SPC can be done in several ways. The microcode can be loaded from a central microprocessor, which can perform both microcode load and system diagnostics at power up, or it can be loaded using dedicated load logic.

An example of a design of this dedicated load logic is shown in the Microcode Load Logic Example (Figure 11). The purpose of this example is to show how one goes about designing this logic. This example shows an approach which loads the RAMs with data from a single EPROM. The load logic gets the SPC command and data information from the EPROM. It is controlled by single byte instructions from the same EPROM. The format of these instructions is shown in Microcode Load Logic Instruction Formats (Figure 12), and a map of the typical contents of the EPROM is shown in Microcode Load EPROM Memory Map (Figure 13).

The load logic consists of a 16-bit address counter, an 8-bit shift register, a 4-bit byte counter and a PAL containing a 2-bit instruction register. The logic in the PAL interprets the 2-bit load instructions to cause bytes of command or data information to be loaded into the IDT74FCT299 shift register and shifted to the SPC. The two IDT74FCT161 counters are used to count the bytes being sent and the 8 bits in each byte.

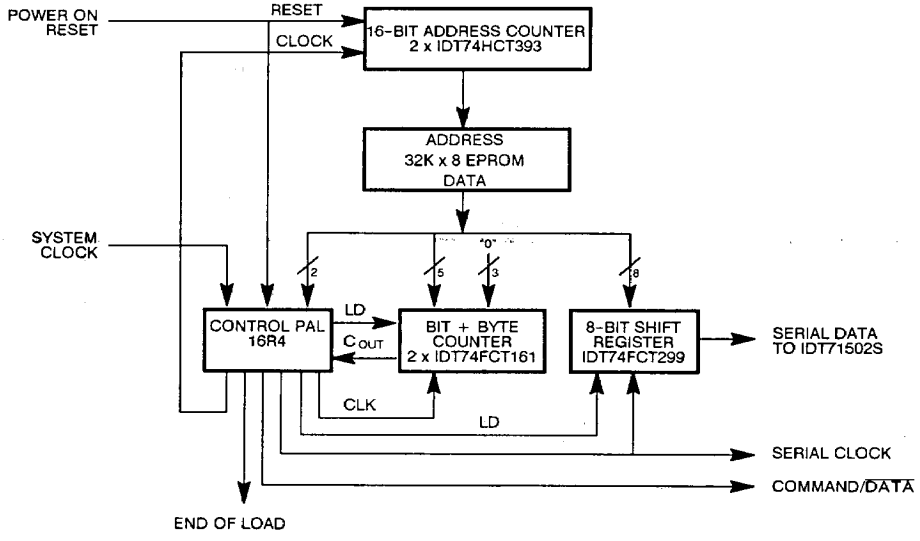


Figure 11. Microcode Load Logic Example

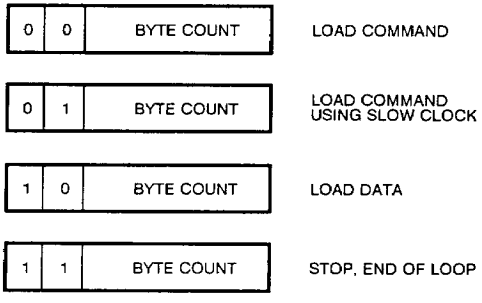


Figure 12. Microcode Load Logic Instruction Formats

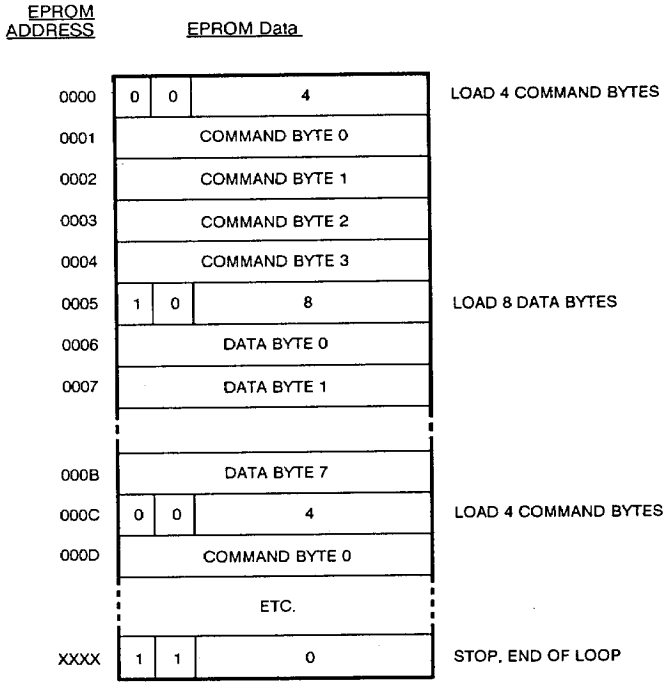
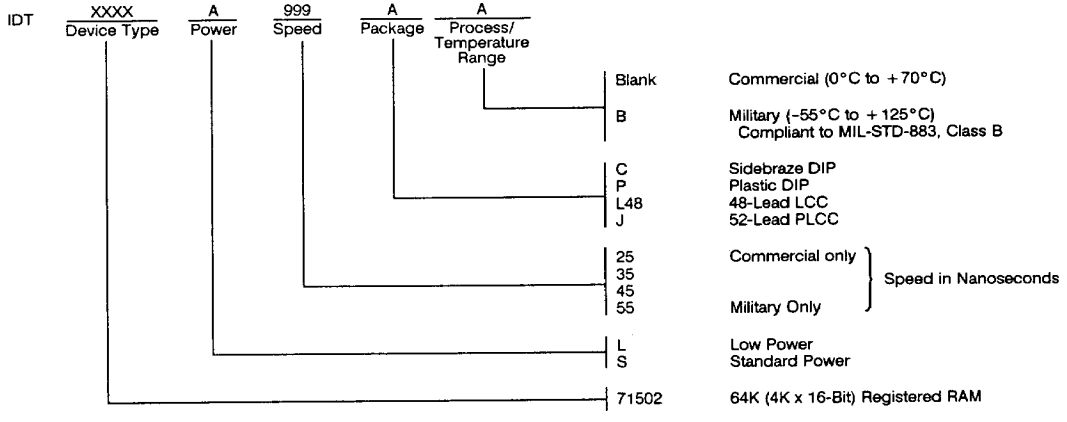


Figure 13. Microcode Load EPROM Memory Map

ORDERING INFORMATION



7