



Integrated Device Technology, Inc.

CMOS STATIC RAM 64K (8K x 8-BIT)

IDT7164S
IDT7164L

FEATURES:

- High-speed address/chip select access time
 - Military: 20/25/30/35/45/55/70/85ns (max.)
 - Commercial: 15/20/25/30/35ns (max.)
- Low power consumption
- Battery backup operation — 2V data retention voltage (L Version only)
- Produced with advanced CMOS high-performance technology
- Inputs and outputs directly TTL-compatible
- Three-state outputs
- Available in:
 - 28-pin DIP, SOIC, SOJ, and CERPACK
 - 32-pin LCC
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7164 is a 65,536 bit high-speed static RAM organized as 8K x 8. It is fabricated using IDT's high-performance, high-reliability CMOS technology.

Address access times as fast as 15ns are available and the circuit offers a reduced power standby mode. When $\overline{CS}_1$ goes HIGH or $\overline{CS}_2$ goes LOW, the circuit will automatically go to, and remain in, a low-power standby mode. The low-power (L) version also offers a battery backup data retention capability at power supply levels as low as 2V.

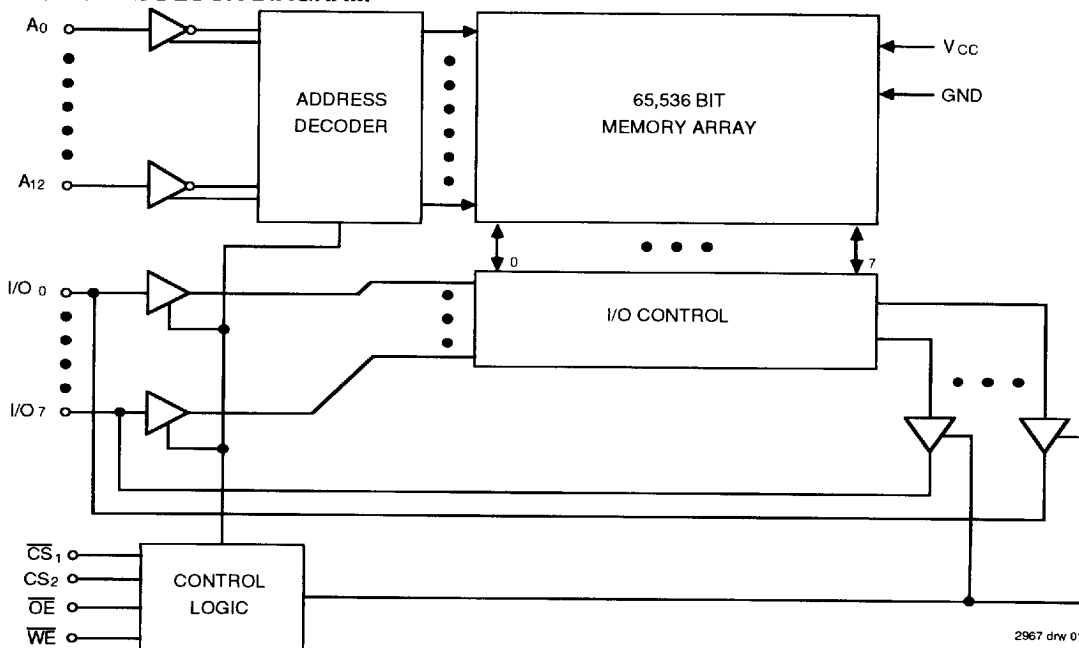
All inputs and outputs of the IDT7164 are TTL-compatible and operation is from a single 5V supply, simplifying system designs. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation.

The IDT7164 is packaged in a 28-pin 300 mil DIP and SOJ; 28-pin 330 mil SOIC; 28-pin 600 mil DIP; 32-pin LCC; and 28-pin CERPACK.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

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FUNCTIONAL BLOCK DIAGRAM



The IDT logo is a registered trademark of Integrated Device Technology, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES

MAY 1994

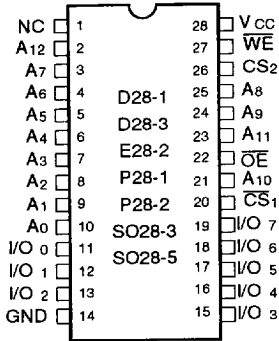
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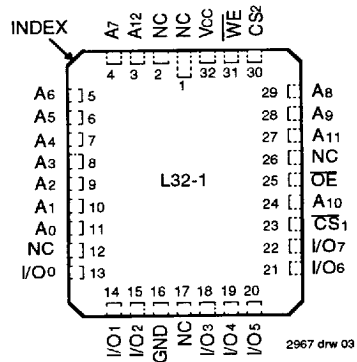
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PIN CONFIGURATIONS



2967 drw 02

DIP/SOIC/SOJ/CERPACK
TOP VIEW



2967 drw 03

32-PIN LCC
TOP VIEW

PIN DESCRIPTIONS

Name	Description
A0-A12	Address
I/O0-I/O7	Data Input/Output
CS1	Chip Select
CS2	Chip Select
WE	Write Enable
OE	Output Enable
GND	Ground
VCC	Power

2967 tbl 01

TRUTH TABLE^(1,2,3)

WE	CS1	CS2	OE	I/O	Function
X	H	X	X	High-Z	Deselected - Standby (ISB)
X	X	L	X	High-Z	Deselected - Standby (ISB)
X	VHC	VHC or VLC	X	High-Z	Deselected - Standby (ISB)
X	X	VLC	X	High-Z	Deselected - Standby (ISB)
H	L	H	H	High-Z	Output Disabled
H	L	H	L	DataOUT	Read Data
L	L	H	X	DataIN	Write Data

NOTES:

- CS2 will power-down CS1, but CS1 will not power-down CS2
- H = VIH, L = VIL, X = don't care.
- VLC = 0.2V, VHC = VCC - 0.2V

2967 tbl 02

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Com'l.	Mil.	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
PT	Power Dissipation	1.0	1.0	W
IOUT	DC Output Current	50	50	mA

2967 tbl 03

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- VTERM must not exceed VCC + 0.5V

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	VCC
Military	-55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2967 tbl 05

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input HIGH Voltage	2.2	—	VCC + 0.5	V
VIL	Input LOW Voltage	-0.5 ⁽¹⁾	—	0.8	V

NOTE:

- VIL (min) = -1.5V for pulse width less than 10ns, once per cycle.

2967 tbl 06

4825771 0015132 915

CAPACITANCE ($T_A = +25^\circ\text{C}$, $f = 1.0\text{MHz}$)

Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	8	pF
C _{I/O}	I/O Capacitance	V _{OUT} = 0V	8	pF

NOTE:

2967 tbl 04

1 This parameter is determined by device characterization, but is not production tested

DC ELECTRICAL CHARACTERISTICS⁽¹⁾(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	7164S15 7164L15		7164S20 7164L20		7164S25 7164L25		7164S30 7164L30		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
ICC1	Operating Power Supply Current, $\overline{\text{CS}}_1 = \text{V}_{\text{IL}}$, $\text{CS}_2 = \text{V}_{\text{IH}}$, Outputs Open, V _{CC} = Max, f = 0 ⁽³⁾	S	110	—	100	110	90	110	90	100	mA
		L	100	—	90	100	80	100	80	90	
ICC2	Dynamic Operating Current $\overline{\text{CS}}_1 = \text{V}_{\text{IL}}$, $\text{CS}_2 = \text{V}_{\text{IH}}$, Outputs Open, V _{CC} = Max, f = f _{MAX} ⁽³⁾	S	180	—	170	180	170	180	160	170	mA
		L	150	—	150	160	150	160	140	150	
ISB	Standby Power Supply Current (TTL Level), $\overline{\text{CS}}_1 \geq \text{V}_{\text{IH}}$ or $\text{CS}_2 \leq \text{V}_{\text{IL}}$, V _{CC} = Max, Outputs Open, f = f _{MAX} ⁽³⁾	S	20	—	20	20	20	20	20	20	mA
		L	3	—	3	5	3	5	3	5	
ISB1	Full Standby Power Supply Current (CMOS Level), f = 0 ⁽³⁾ , V _{CC} = Max 1 $\overline{\text{CS}}_1 \geq \text{V}_{\text{HC}}$ and $\text{CS}_2 \geq \text{V}_{\text{HC}}$, or 2 $\text{CS}_2 \leq \text{V}_{\text{LC}}$	S	15	—	15	20	15	20	15	20	mA
		L	0.2	—	0.2	1	0.2	1	0.2	1	

6

DC ELECTRICAL CHARACTERISTICS⁽¹⁾ (Continued)(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	7164S35 7164L35		7164S45 7164L45		7164S55 7164L55		7164S70/85 ⁽²⁾ 7164L70/85 ⁽²⁾		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
ICC1	Operating Power Supply Current, $\overline{\text{CS}}_1 = \text{V}_{\text{IL}}$, $\text{CS}_2 = \text{V}_{\text{IH}}$, Outputs Open, V _{CC} = Max, f = 0 ⁽³⁾	S	90	100	—	100	—	100	—	100	mA
		L	80	90	—	90	—	90	—	90	
ICC2	Dynamic Operating Current $\overline{\text{CS}}_1 = \text{V}_{\text{IL}}$, $\text{CS}_2 = \text{V}_{\text{IH}}$, Outputs Open, V _{CC} = Max, f = f _{MAX} ⁽³⁾	S	150	160	—	160	—	160	—	160	mA
		L	130	140	—	130	—	125	—	120	
ISB	Standby Power Supply Current (TTL Level), $\overline{\text{CS}}_1 \geq \text{V}_{\text{IH}}$, or $\text{CS}_2 \leq \text{V}_{\text{IL}}$, V _{CC} = Max, Outputs Open, f = f _{MAX} ⁽³⁾	S	20	20	—	20	—	20	—	20	mA
		L	3	5	—	5	—	5	—	5	
ISB1	Full Standby Power Supply Current (CMOS Level), f = 0 ⁽³⁾ , V _{CC} = Max 1 $\overline{\text{CS}}_1 \geq \text{V}_{\text{HC}}$ and $\text{CS}_2 \geq \text{V}_{\text{HC}}$, or 2 $\text{CS}_2 \leq \text{V}_{\text{LC}}$	S	15	20	—	20	—	20	—	20	mA
		L	0.2	1	—	1	—	1	—	1	

NOTES:

2967 tbl 07

1 All values are maximum guaranteed values

2 Also available 100, 120, 150 and 200ns military devices

3 f_{MAX} = 1/trc (all address inputs are cycling at f_{MAX}), f = 0 means no address input lines are changing

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	IDT7164S		IDT7164L		Unit
			Min.	Max.	Min.	Max.	
I _{LI}	Input Leakage Current	V _{CC} = Max , V _{IN} = GND to V _{CC}	MIL. COM'L	— 10 5	— 5 2	— 5 2	μA
I _{LO}	Output Leakage Current	V _{CC} = Max., $\overline{CS}_1 = V_{IH}$, V _{OUT} = GND to V _{CC}	MIL. COM'L	— 10 5	— 5 2	— 5 2	μA
V _{OL}	Output Low Voltage	I _{OL} = 8mA, V _{CC} = Min		0.4	—	0.4	V
		I _{OL} = 10mA, V _{CC} = Min		—	0.5	0.5	
V _{OH}	Output High Voltage	I _{OH} = -4mA, V _{CC} = Min		2.4	—	2.4	V

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) (V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Test Condition	Min.	Typ. ⁽¹⁾ V _{CC} @		Max. V _{CC} @		Unit
				2.0V	3.0V	2.0V	3.0V	
V _{DR}	V _{CC} for Data Retention	—	2.0	—	—	—	—	V
I _{CCDR}	Data Retention Current	MIL. COM'L	— —	10 10	15 15	200 60	300 90	μA
t _{CDR} ⁽³⁾	Chip Deselect to Data Retention Time	1. $\overline{CS}_1 \geq V_{HC}$ CS ₂ ≥ V _{HC} , or	0	—	—	—	—	ns
t _R ⁽³⁾	Operation Recovery Time	2 CS ₂ ≤ V _{LC}	t _{RC} ⁽²⁾	—	—	—	—	ns
I _{LI} ⁽³⁾	Input Leakage Current		—	—	—	2	2	μA

NOTES:

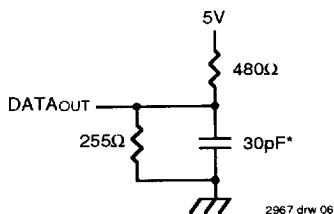
1. T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed by device characterization, but is not production tested

2967 tbl 10

AC TEST CONDITIONS

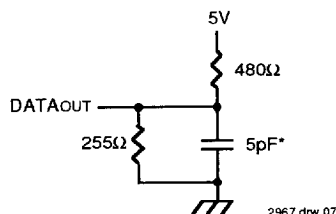
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2967 tbl 08



2967 drw 06

Figure 1. AC Test Load



2967 drw 07

Figure 2. AC Test Load
(for t_{CLZ1}, t_{CLZ2}, t_{OLZ}, t_{CHZ1}, t_{CHZ2}, t_{OHZ}, t_{OW}, and t_{WHZ})

*Includes scope and jig capacitances

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%, All Temperature Ranges)

		7164S15 ⁽¹⁾ 7164L15 ⁽¹⁾		7164S20 7164L20		7164S25 7164L25		7164S30 7164L30		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle										
tRC	Read Cycle Time	15	—	20	—	25	—	30	—	ns
tAA	Address Access Time	—	15	—	19	—	25	—	29	ns
tACS1 ⁽³⁾	Chip Select-1 Access Tim	—	15	—	20	—	25	—	30	ns
tACS2 ⁽³⁾	Chip Select-2 Access Time	—	20	—	25	—	30	—	35	ns
tCLZ1,2 ⁽⁴⁾	Chip Select-1, 2 to Output in Low-Z	5	—	5	—	5	—	5	—	ns
tOE	Output Enable to Output Valid	—	7	—	8	—	12	—	15	ns
tOLZ ⁽⁴⁾	Output Enable to Output in Low-Z	0	—	0	—	0	—	0	—	ns
tCHZ1,2 ⁽⁴⁾	Chip Select-1, 2 to Output in High-Z	—	8	—	9	—	13	—	13	ns
tOHZ ⁽⁴⁾	Output Disable to Output in High-Z	—	7	—	8	—	10	—	12	ns
tOH	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
tPU ⁽⁴⁾	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	ns
tPD ⁽⁴⁾	Chip Deselect to Power Down Time	—	15	—	20	—	25	—	30	ns
Write Cycle										
tWC	Write Cycle Time	15	—	20	—	25	—	30	—	ns
tCW1, 2	Chip Select to End-of-Write	14	—	15	—	18	—	22	—	ns
tAW	Address Valid to End-of-Write	14	—	15	—	18	—	22	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	14	—	15	—	21	—	23	—	ns
tWR1	Write Recovery Time ($\overline{CS_1}$, $\overline{WE}$)	0	—	0	—	0	—	0	—	ns
tWR2	Write Recovery Time ($\overline{CS_2}$)	5	—	5	—	5	—	5	—	ns
tWHZ ⁽⁴⁾	Write Enable to Output in High-Z	—	6	—	8	—	10	—	12	ns
tDW	Data to Write Time Overlap	8	—	10	—	13	—	13	—	ns
tDH1	Data Hold from Write Time ($\overline{CS_1}$, $\overline{WE}$)	0	—	0	—	0	—	0	—	ns
tDH2	Data Hold from Write Time ($\overline{CS_2}$)	5	—	5	—	5	—	5	—	ns
tOW ⁽⁴⁾	Output Active from End-of-Write	4	—	4	—	4	—	4	—	ns

NOTES:

- 1 0° to +70°C temperature range only
- 2 -55°C to +125°C temperature range only Also available 100, 120, 150 and 200ns military devices.
- 3 Both chip selects must be active for the device to be selected
- 4 This parameter is guaranteed by device characterization, but is not production tested

2967 tbl 11

6

AC ELECTRICAL CHARACTERISTICS (Continued) (V_{CC} = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	7164S35 7164L35		7164S45 ⁽²⁾ 7164L45 ⁽²⁾		7164S55 ⁽²⁾ 7164L55 ⁽²⁾		7164S70 ^{(2)/85⁽²⁾} 7164L70 ^{(2)/85⁽²⁾}		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t _{RC}	Read Cycle Time	35	—	45	—	55	—	70/85	—	ns
t _{AA}	Address Access Time	—	35	—	45	—	55	—	70/85	ns
t _{ACS1} ⁽³⁾	Chip Select-1 Access Time	—	35	—	45	—	55	—	70/85	ns
t _{ACS2} ⁽³⁾	Chip Select-2 Access Time	—	40	—	45	—	55	—	70/85	ns
t _{CLZ1,2} ⁽⁴⁾	Chip Select-1, 2 to Output in Low-Z	5	—	5	—	5	—	5	—	ns
t _{OE}	Output Enable to Output Valid	—	18	—	25	—	30	—	35/40	ns
t _{OLZ} ⁽⁴⁾	Output Enable to Output in Low-Z	0	—	0	—	0	—	0	—	ns
t _{CHZ1,2} ⁽⁴⁾	Chip Select-1, 2 to Output in High-Z	—	15	—	20	—	25	—	30/35	ns
t _{OHZ} ⁽⁴⁾	Output Disable to Output in High-Z	—	15	—	20	—	25	—	30/35	ns
t _{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
t _{PU} ⁽⁴⁾	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	ns
t _{PD} ⁽⁴⁾	Chip Deselect to Power Down Time	—	35	—	45	—	55	—	70/85	ns
Write Cycle										
t _{WC}	Write Cycle Time	35	—	45	—	55	—	70/85	—	ns
t _{CW1,2}	Chip Select to End-of-Write	25	—	33	—	50	—	60/75	—	ns
t _{AW}	Address Valid to End-of-Write	25	—	33	—	50	—	60/75	—	ns
t _{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t _{WP}	Write Pulse Width	25	—	25	—	50	—	60/75	—	ns
t _{WR1}	Write Recovery Time ($\overline{CS_1}$, $\overline{WE}$)	0	—	0	—	0	—	0	—	ns
t _{WR2}	Write Recovery Time (CS ₂)	5	—	5	—	5	—	5	—	ns
t _{WHZ} ⁽⁴⁾	Write Enable to Output in High-Z	—	14	—	18	—	25	—	30/35	ns
t _{DW}	Data to Write Time Overlap	15	—	20	—	25	—	30/35	—	ns
t _{DH1}	Data Hold from Write Time ($\overline{CS_1}$, $\overline{WE}$)	0	—	0	—	0	—	0	—	ns
t _{DH2}	Data Hold from Write Time (CS ₂)	5	—	5	—	5	—	5	—	ns
t _{OW} ⁽⁴⁾	Output Active from End-of-Write	4	—	4	—	4	—	4	—	ns

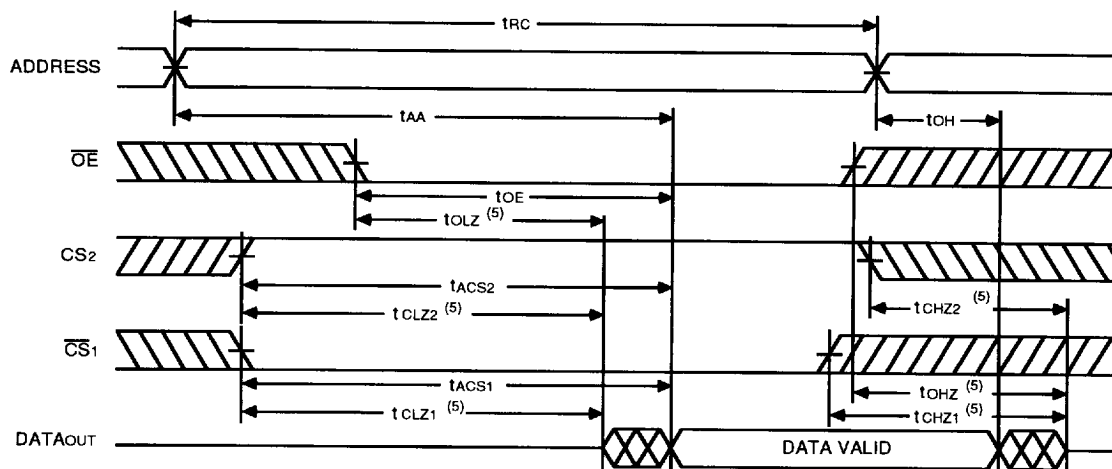
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2967 tbl 11

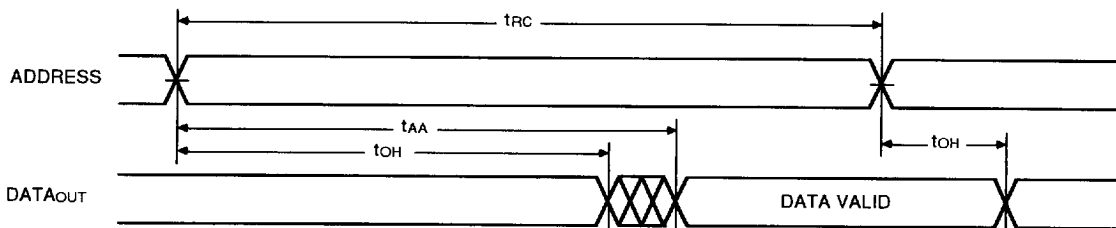
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TIMING WAVEFORM OF READ CYCLE NO. 1⁽¹⁾



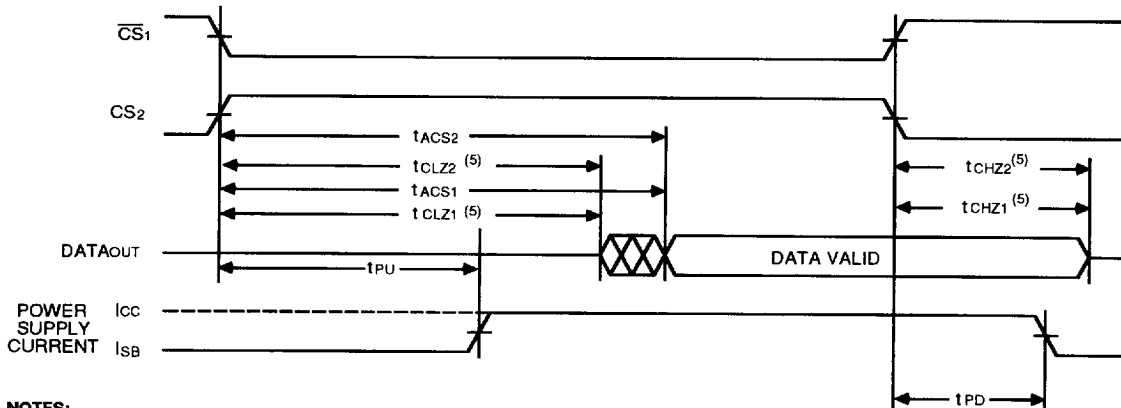
2967 drw 08

TIMING WAVEFORM OF READ CYCLE NO. 2^(1, 2, 4)



2967 drw 09

TIMING WAVEFORM OF READ CYCLE NO. 3^(1, 3, 4)

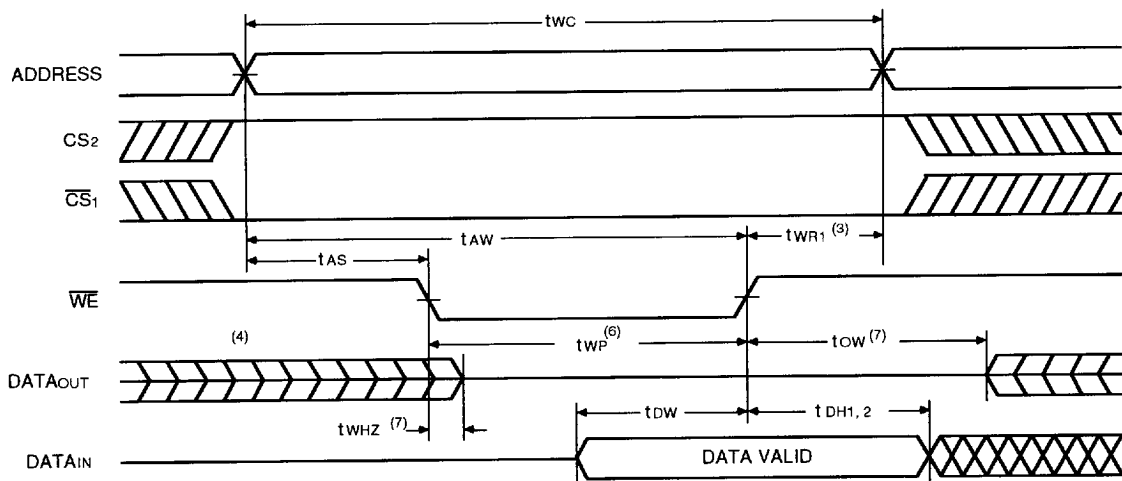


2967 drw 10

NOTES:

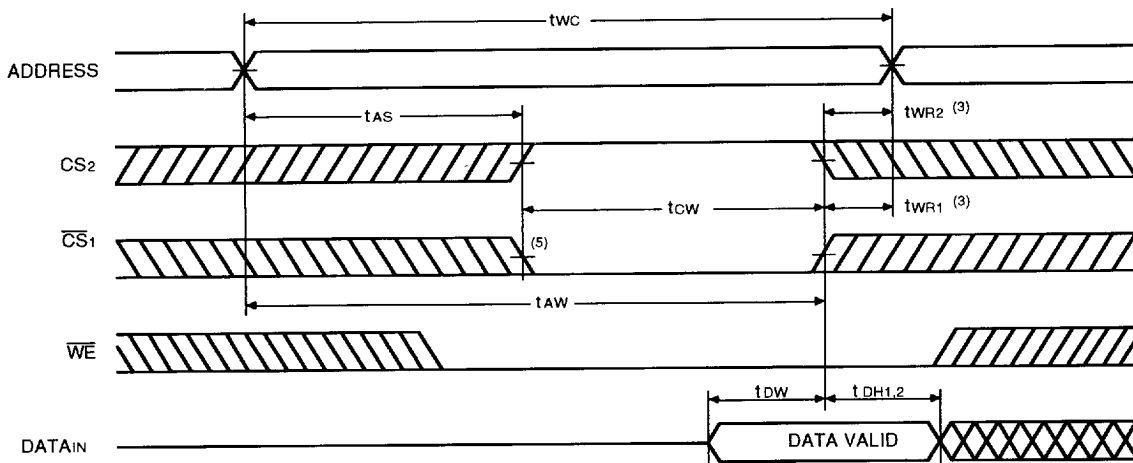
- WE is HIGH for Read cycle
- Device is continuously selected, $\overline{CS}_1$ is LOW CS_2 is HIGH
- Address valid prior to or coincident with $\overline{CS}_1$ transition LOW and CS_2 transition HIGH
- $\overline{OE}$ is LOW
- Transition is measured $\pm 200mV$ from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)^(1, 2, 6)



2967 drw 11

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)^(1, 2)

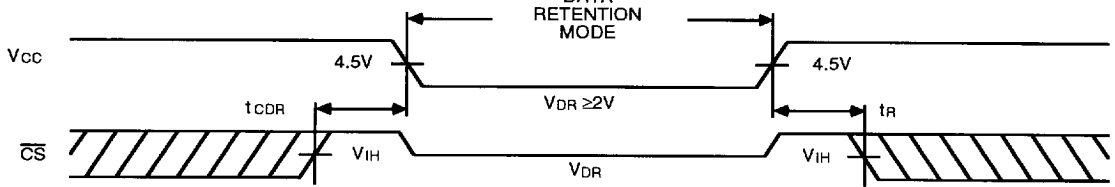


2967 drw 12

NOTES:

- 1 $\overline{WE}$, $\overline{CS1}$ or $\overline{CS2}$ must be inactive during all address transitions.
- 2 A write occurs during the overlap of a LOW $\overline{WE}$, a LOW $\overline{CS1}$ and a HIGH $\overline{CS2}$.
- 3 $t_{WR1,2}$ is measured from the earlier of $\overline{CS1}$ or $\overline{WE}$ going HIGH or $\overline{CS2}$ going LOW to the end of the write cycle.
- 4 During this period, I/O pins are in the output state so that the input signals must not be applied.
- 5 If the $\overline{CS1}$ LOW transition or $\overline{CS2}$ HIGH transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
- 6 $\overline{OE}$ is continuously HIGH. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or $(t_{WHZ} + t_{DW})$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW} . If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse width is as short as the specified t_{WP} .
- 7 Transition is measured $\pm 200mV$ from steady state.

LOW V_{CC} DATA RETENTION WAVEFORM



2967 drw 05

ORDERING INFORMATION

IDT	7164	X	XX	XXX	X	
Device Type	Power	Speed	Package	Process/ Temperature Range		
					Blank	Commercial (0°C to +70°C)
					B	Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B
					Y	300 mil SOJ (SO28-5)
					PE	330 mil SOIC (SO28-3)
					TD	300 mil CERDIP (D28-3)
					D	600 mil CERDIP (D28-1)
					P	600 mil Plastic DIP (P28-1)
					TP	300 mil Plastic DIP (P28-2)
					L32	32 Leadless Chip Carrier (L32-1)
					XE	CERPACK F11 (E28-2)
					15	Commercial Only
					20	
					25	
					30	
					35	Military Only
					45	Military Only
					55	Military Only
					70	Military Only
					85	Military Only
					S	Standard Power
					L	Low Power

Speed in nanoseconds

2967 drw 13