



Integrated Device Technology, Inc.

CMOS STATIC RAMS

16K (4K x 4-BIT)

Separate Data Inputs and Outputs

IDT 71681SA/LA
IDT 71682SA/LA

T-46-23-08

FEATURES:

- Separate data inputs and outputs
- IDT71681SA/LA: outputs track inputs during write mode
- IDT71682SA/LA: high impedance outputs during write mode
- High-speed (equal access and cycle time)
 - Military: 15/20/25/35/45/55/70/85/100ns (max.)
 - Commercial: 12/15/20/25/35/45ns (max.)
- Low power consumption
 - IDT71681/2SA
 - Active: 225mW (typ.)
 - Standby: 100μW (typ.)
 - IDT71681/2LA
 - Active: 225mW (typ.)
 - Standby: 10μW (typ.)
- Battery backup operation—2V data retention (L version only)
- High-density 24-pin 300-mil CERDIP and plastic DIP, 24-pin Flatpack and CERPAC, 24-pin SOIC (gull-wing or J-bend) and 28-pin leadless chip carrier
- Produced with advanced CEMOS™ high-performance technology
- CEMOS process virtually eliminates alpha particle soft-error rates
- Single 5V (±10%) power supply
- Inputs and outputs directly TTL-compatible
- Three-state output
- Static operation: no clocks or refresh required
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT71681/IDT71682 are 16,384-bit high-speed static RAMs organized as 4K x 4. They are fabricated using IDT's high-performance, high-reliability technology—CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective alternative to bipolar and fast NMOS memories.

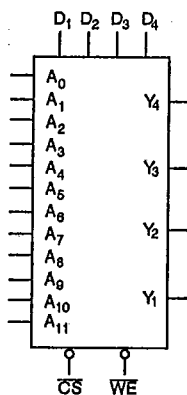
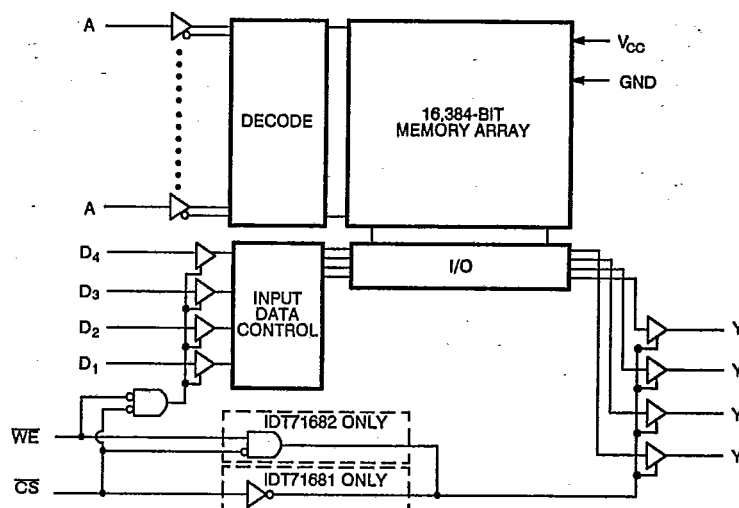
Access times as fast as 12ns are available, with maximum power consumption of only 550mW. These circuits also offer a reduced power standby mode (I_{sa}). When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, this standby mode as long as $\overline{CS}$ remains high. In the ultra-low-power standby mode (I_{se1}), the devices consume less than 10μW, typically. This capability provides significant system-level power and cooling savings. The low-power (L) versions also offer a battery backup data retention capability where the circuit typically consumes only 1μW operating off a 2V battery.

All inputs and outputs of the IDT71681/IDT71682 are TTL-compatible and operate from a single 5V supply, thus simplifying system designs. Fully static asynchronous circuitry is used, which requires no clocks or refreshing for operation, and provides equal access and cycle times for ease of use.

The IDT71681/IDT71682 are packaged in either space-saving 24-pin 300 mil DIPs, SOICs, Flatpacks, CERPACs, or 28-pin leadless chip carriers, providing high board-level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

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LOGIC SYMBOL**FUNCTIONAL BLOCK DIAGRAM**

CEMOS is a trademark of Integrated Device Technology, Inc.

MILITARY AND COMMERCIAL TEMPERATURE RANGES**JANUARY 1989**

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S4-39

DSC-1022-

INTEGRATED DEVICE

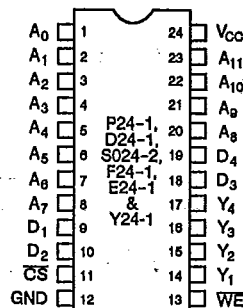
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IDT71681SA/LA AND IDT71682SA/LA
CMOS STATIC RAM 16K (4K x 4-BIT)

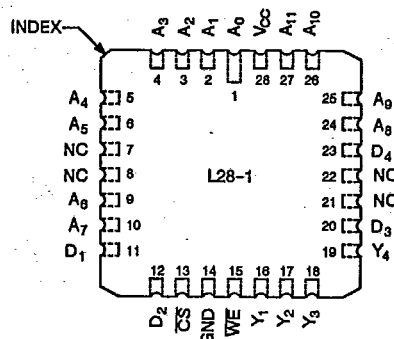
MILITARY AND COMMERCIAL TEMPERATURE RANGES

PIN CONFIGURATIONS

T-46-23-08



DIP/SOIC/FLATPACK/CERPACK
TOP VIEW



LCC
TOP VIEW

PIN NAMES

A ₀ -A ₁₁	Address Inputs	D ₁ - D ₄	DATA _{IN}
CS	Chip Select	Y ₁ - Y ₄	DATA _{OUT}
WE	Write Enable	GND	Ground
V _{CC}	Power		

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V _{IH}	Input High Voltage	2.2	—	6.0	V
V _{IL}	Input Low Voltage	-0.5 ⁽¹⁾	—	0.8	V

NOTE:

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V _{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T _A	Operating Temperature	0 to +70	-55 to +125	°C
T _{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T _{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P _T	Power Dissipation	1.0	1.0	W
I _{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V _{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

IDT71681SA/LA AND IDT71682SA/LA
CMOS STATIC RAM 16K (4K x 4-BIT)

MILITARY AND COMMERCIAL TEMPERATURE RANGES

DC ELECTRICAL CHARACTERISTICS

 $V_{CC} = 5.0V \pm 10\%$

SYMBOL	PARAMETER	TEST CONDITION	MIL COM'L	IDT71681SA IDT71682SA			IDT71681LA IDT71682LA			UNIT
				MIN.	TYP. ⁽¹⁾	MAX.	MIN.	TYP. ⁽¹⁾	MAX.	
I_{IL}	Input Leakage Current	$V_{CC} = \text{Max.}, V_{IN} = \text{GND to } V_{CC}$		—	—	10 5	—	—	5 2	μA
I_{LO}	Output Leakage Current	$V_{CC} = \text{Max.},$ $CS = V_{IH}, V_{OUT} = \text{GND to } V_{CC}$		—	—	10 5	—	—	5 2	μA
V_{OL}	Output Low Voltage	$I_{OL} = 10\text{mA}, V_{CC} = \text{Min.}$		—	—	0.5	—	—	0.5	V
		$I_{OL} = 8\text{mA}, V_{CC} = \text{Min.}$		—	—	0.4	—	—	0.4	V
V_{OH}	Output High Voltage	$I_{OH} = -4\text{mA}, V_{CC} = \text{Min.}$		2.4	—	—	2.4	—	—	V

NOTE:

1. Typical limits are at $V_{CC} = 5.0V, +25^\circ C$ ambient.

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DC ELECTRICAL CHARACTERISTICS⁽¹⁾ $V_{CC} = 5.0V \pm 10\%, V_{LO} = 0.2V, V_{HO} = V_{CC} - 0.2V$

SYMBOL	PARAMETER	POWER	71681x12 71682x12	71681x15 71682x15	71681x20 71682x20	71681x25 71682x25	71681x35 71682x35	71681x45 71682x45	71681x55 ⁽⁶⁾ 71682x55 ⁽⁶⁾	71681x70 ^(2,6) 71682x70 ^(2,6)	UNIT
			COM'L MIL	COM'L MIL	COM'L MIL	COM'L MIL	COM'L MIL	COM'L MIL	COM'L MIL	COM'L MIL	
I_{CC1}	Operating Power Supply Current $CS = V_{IL},$ Outputs Open, $V_{CC} = \text{Max.},$ $f = 0$ ⁽³⁾	SA	110 —	110 120	90 100	90 100	90 100	90 100	— 100	— 100	mA
		LA	— —	— —	70 80	70 80	70 80	70 80	— 80	— 80	
I_{CC2}	Dynamic Operating Current $CS = V_{IL},$ Outputs Open, $V_{CC} = \text{Max.},$ $f = f_{MAX}$ ⁽³⁾	SA	165 —	145 165	120 120	110 120	100 110	100 110	— 110	— 110	mA
		LA	— —	— —	100 110	90 100	80 90	70 80	— 80	— 80	
I_{SB}	Standby Power Supply Current (TTL Level) $CS \geq V_{IH},$ $V_{CC} = \text{Max.},$ Outputs Open $f = f_{MAX}$ ⁽³⁾	SA	65 —	65 65	45 55	35 45	30 35	30 35	— 35	— 35	mA
		LA	— —	— —	30 35	25 30	20 25	20 25	— 20	— 20	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $CS \geq V_{HO},$ $V_{CC} = \text{Max.},$ $V_{IN} \geq V_{HO}$ or $V_{IN} \leq V_{LO}, f = 0$ ⁽³⁾	SA	20 —	20 30	20 30	2 10	2 10	2 10	— 10	— 10	mA
		LA	— —	— —	0.5 5	0.05 0.3	0.05 0.3	0.05 0.3	— 0.3	— 0.3	

NOTES:

1. All values are maximum guaranteed values.
2. Also available: 85ns and 100ns Military devices.
3. At $f = f_{MAX}$ address and data inputs are cycling at the maximum frequency of read cycles of $1/t_{RO}$. $f = 0$ means no input lines change.
4. "x" in part numbers indicates power rating (SA or LA).
5. $0^\circ C$ to $+70^\circ C$ temperature range only.
6. $-55^\circ C$ to $+125^\circ C$ temperature range only.

DATA RETENTION CHARACTERISTICS

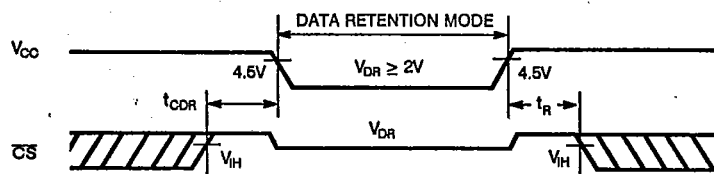
(L Version Only)

T-46-23-08

SYMBOL	PARAMETER	TEST CONDITION	IDT71681LA - IDT71682LA			UNIT
			MIN.	TYP. ⁽¹⁾	MAX.	
V_{DR}	V_{CC} for Data Retention		2.0	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $\leq 0.2V$	MIL. —	0.5 ⁽²⁾	100 ⁽²⁾	μA
			COM'L. —	1.0 ⁽³⁾	150 ⁽³⁾	μA
$t_{CDR}^{(5)}$	Chip Deselect to Data Retention Time		0	—	—	ns
$t_R^{(5)}$	Operation Recovery Time		$t_{RO}^{(4)}$	—	—	ns

NOTES:

1. $T_A = +25^\circ C$
2. at $V_{DD} = 2V$
3. at $V_{DD} = 3V$
4. t_{RO} = Read Cycle Time
5. This parameter is guaranteed but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

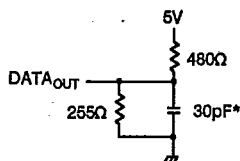
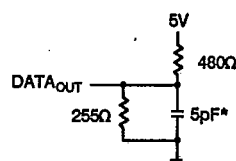


Figure 1. Output Load

Figure 2. Output Load
(for t_{HZ} , t_{LZ} , t_{WZ} and t_{OW})

* Including scope and jig.

IDT71681SA/LA AND IDT71682SA/LA
CMOS STATIC RAM 16K (4K x 4-BIT)

MILITARY AND COMMERCIAL TEMPERATURE RANGES

AC ELECTRICAL CHARACTERISTICS⁽⁴⁾ ($V_{CC} = 5V \pm 10\%$, All Temperature Ranges)

T=46-23-08

SYMBOL	PARAMETER	71681x12 ⁽¹⁾ 71682x12 ⁽¹⁾ MIN. MAX.	71681x15 71682x15 MIN. MAX.	71681x20 71682x20 MIN. MAX.	71681x25 71682x25 MIN. MAX.	71681x35 71682x35 MIN. MAX.	71681x45 71682x45 MIN. MAX.	71681x55 ⁽²⁾ 71682x55 ⁽²⁾ MIN. MAX.	71681x70 ⁽²⁾ 71682x70 ⁽²⁾ MIN. MAX.	UNIT
READ CYCLE										
t_{RO}	Read Cycle Time	12 —	15 —	20 —	25 —	35 —	45 —	55 —	70 —	ns
t_{AA}	Address Access Time	— 12	— 15	— 20	— 25	— 35	— 45	— 55	— 70	ns
t_{ACS}	Chip Select Access Time	— 12	— 15	— 20	— 25	— 35	— 45	— 55	— 70	ns
t_{OH}	Output Hold from Address Change	3 —	5 —	5 —	5 —	5 —	5 —	5 —	5 —	ns
t_{LZ}	Chip Select to Output in Low Z ⁽³⁾	3 —	5 —	5 —	5 —	5 —	5 —	5 —	5 —	ns
t_{HZ}	Chip Deselect to Output in High Z ⁽³⁾	— 7	— 7	— 9	— 10	— 15	— 20	— 25	— 30	ns
t_{PU}	Chip Select to Power Up Time ⁽³⁾	0 —	0 —	0 —	0 —	0 —	0 —	0 —	0 —	ns
t_{PD}	Chip Deselect to Power Down Time ⁽³⁾	— 10	— 15	— 20	— 25	— 35	— 40	— 50	— 60	ns

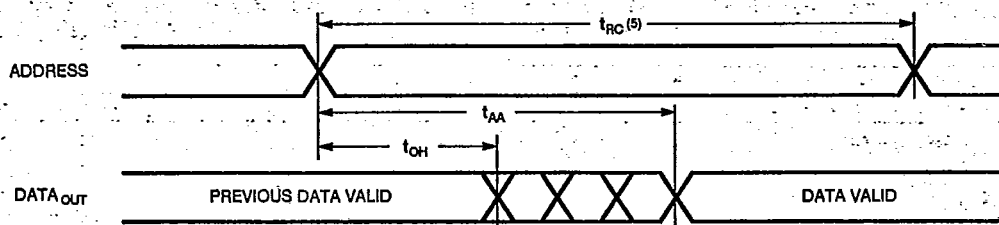
NOTES:

1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.
4. "x" in part numbers represents SA or LA.

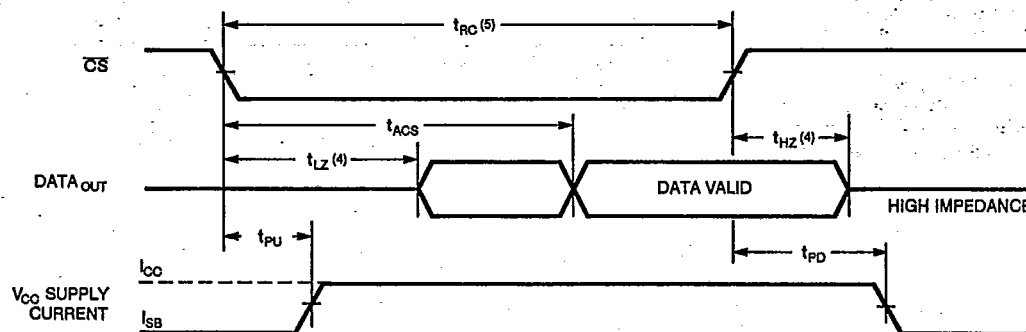
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TIMING WAVEFORM OF READ CYCLE NO. 1^(1,2)

T-46-23-08



TIMING WAVEFORM OF READ CYCLE NO. 2^(1,3)



NOTES:

1. $\overline{WE}$ is High for READ Cycle.
2. $\overline{CS}$ is low for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured $\pm 200mV$ from steady state voltage with specified loading in Figure 2.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.

AC ELECTRICAL CHARACTERISTICS⁽⁴⁾ ($V_{CC} = 5V \pm 10\%$, All Temperature Ranges)

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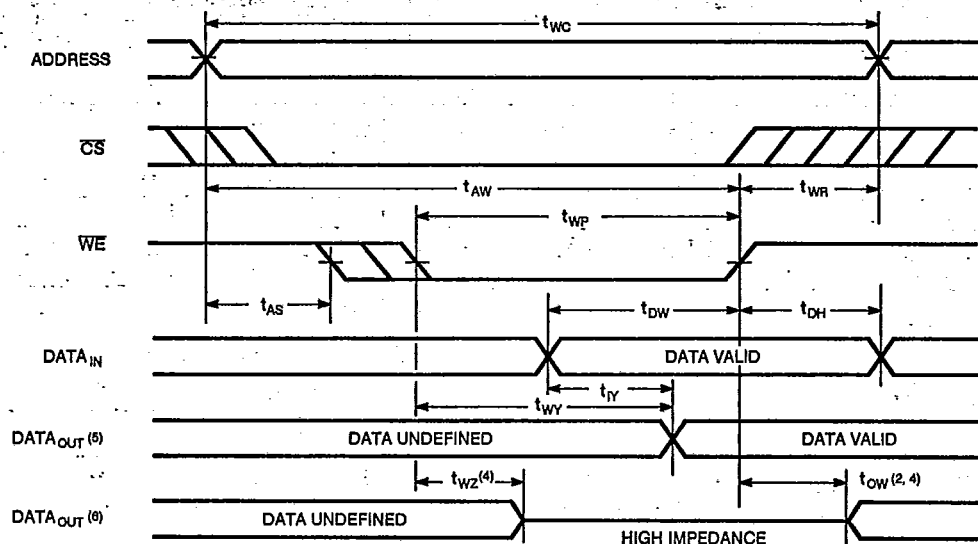
SYMBOL	PARAMETER	71681x12 ⁽¹⁾ 71682x12 ⁽¹⁾ MIN. MAX.	71681x15 71682x15 MIN. MAX.	71681x20 71682x20 MIN. MAX.	71681x25 71682x25 MIN. MAX.	71681x35 71682x35 MIN. MAX.	71681x45 71682x45 MIN. MAX.	71681x55 ⁽²⁾ 71682x55 ⁽²⁾ MIN. MAX.	71681x70 ⁽²⁾ 71682x70 ⁽²⁾ MIN. MAX.	UNIT
WRITE CYCLE										
t_{WC}	Write Cycle Time	12 —	15 —	20 —	20 —	30 —	40 —	50 —	60 —	ns
t_{CW}	Chip Select to End of Write	10 —	15 —	20 —	20 —	25 —	35 —	50 —	60 —	ns
t_{AW}	Address Valid to End of Write	10 —	15 —	20 —	20 —	25 —	35 —	50 —	60 —	ns
t_{AS}	Address Set-up Time	0 —	0 —	0 —	0 —	0 —	0 —	0 —	0 —	ns
t_{WP}	Write Pulse Width	10 —	15 —	20 —	20 —	25 —	30 —	35 —	40 —	ns
t_{WR}	Write Recovery Time	0 —	0 —	0 —	0 —	0 —	0 —	0 —	0 —	ns
t_{DW}	Data Valid to End of Write	8 —	9 —	10 —	10 —	15 —	20 —	20 —	25 —	ns
t_{DH}	Data Hold Time	0 —	0 —	0 —	0 —	3 —	3 —	3 —	3 —	ns
t_{IV}	Data Valid to Output Valid (71681 only) ⁽³⁾	— 12	— 15	— 20	— 25	— 30	— 35	— 35	— 40	ns
t_{WV}	Write Enable to Output Valid (71681 only) ⁽³⁾	— 12	— 15	— 20	— 25	— 30	— 35	— 35	— 40	ns
t_{WZ}	Write Enable to Output in HIGH Z (71682 only) ⁽³⁾	— 5	— 6	— 7	— 7	— 13	— 20	— 25	— 30	ns
t_{OW}	Output Active from End of Write (71682 only) ⁽³⁾	0 —	0 —	0 —	0 —	0 —	0 —	0 —	0 —	ns

NOTES:

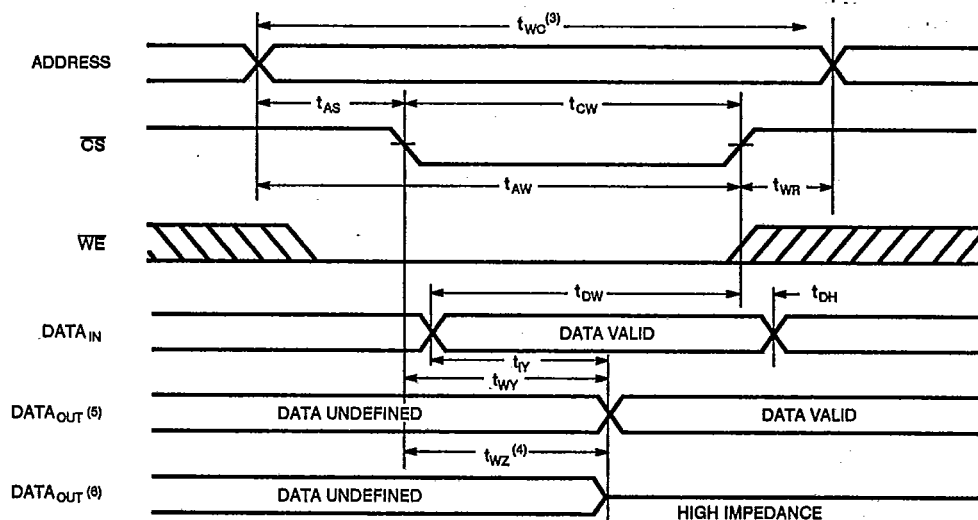
- 0°C to +70°C temperature range only.
- 55°C to +125°C temperature range only.
- This parameter guaranteed but not tested.
- "X" in part numbers represents SA or LA.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)⁽¹⁾

T-46-23-08



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)⁽¹⁾



NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the outputs remain in the high impedance state.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured ± 200 mV from steady state voltage with specified loading in Figure 2.
5. For IDT71681 only.
6. For IDT71682 only.

IDT71681SA/LA AND IDT71682SA/LA
CMOS STATIC RAM 16K (4K x 4-BIT)

MILITARY AND COMMERCIAL TEMPERATURE RANGES

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	High Z	Standby
Read	L	H	D _{OUT}	Active
Write ⁽¹⁾	L	L	D _{IN}	Active
Write ⁽²⁾	L	L	High Z	Active

CAPACITANCE ($T_A = +25^\circ\text{C}$, $f = 1.0\text{MHz}$)

T-46-23-08

SYMBOL	PARAMETER ⁽¹⁾	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = 0V$	8	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	8	pF

NOTE:

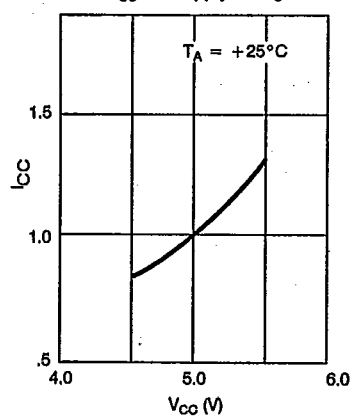
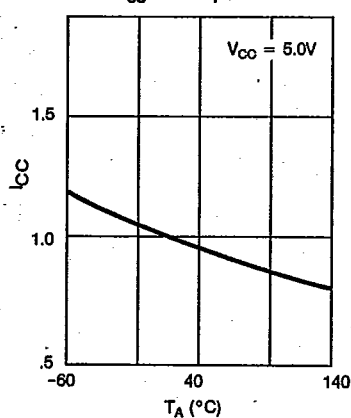
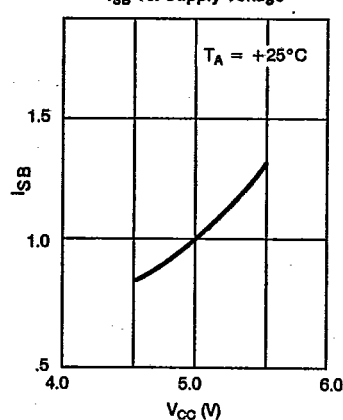
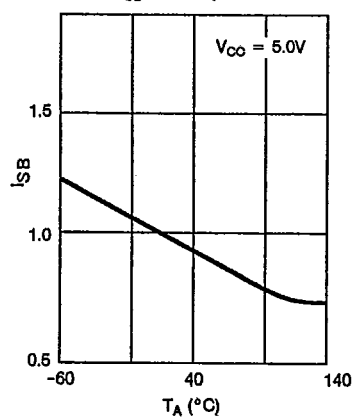
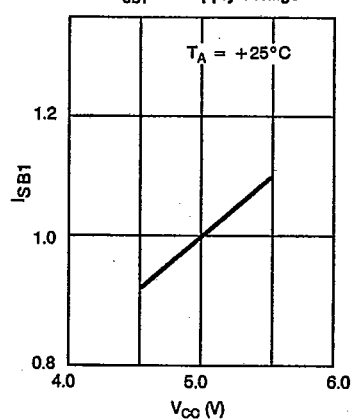
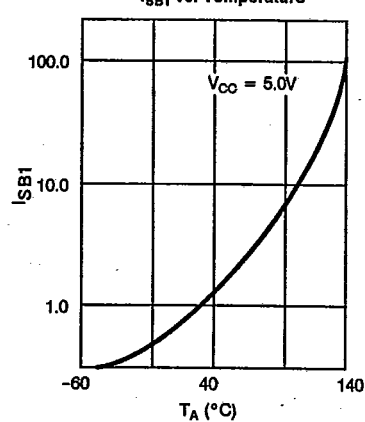
1. This parameter is determined by device characterization but is not production tested.

NOTES:

1. For IDT71681 only.
2. For IDT71682 only.

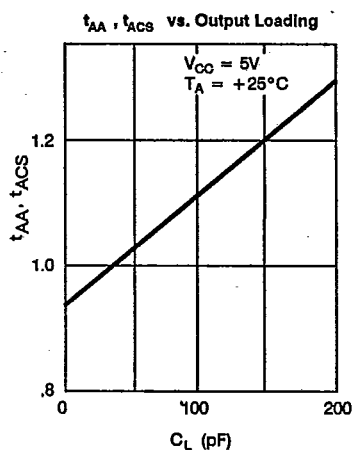
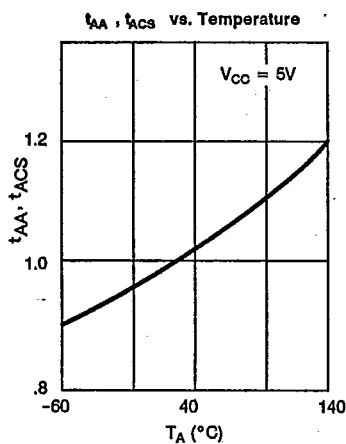
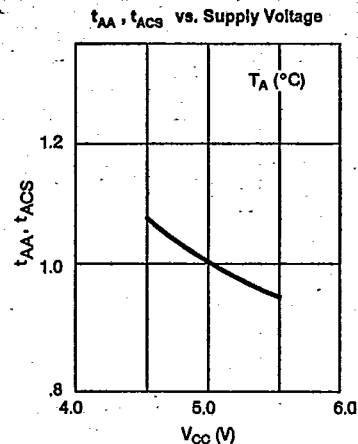
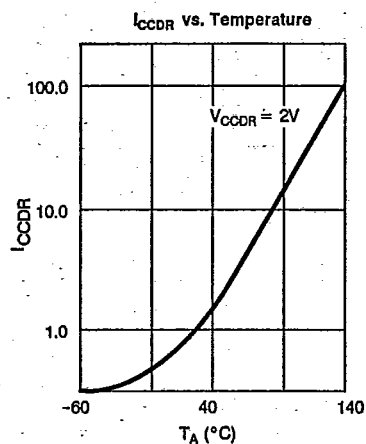
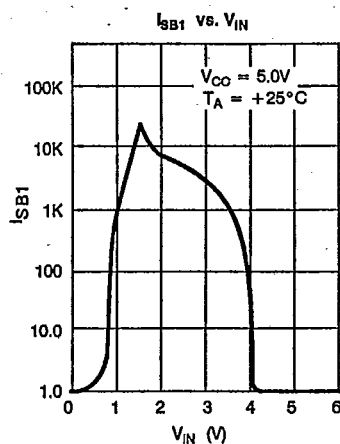
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NORMALIZED TYPICAL DC AND AC CHARACTERISTICS

 I_{CC} vs. Supply Voltage I_{CC} vs. Temperature I_{SB} vs. Supply Voltage I_{SB} vs. Temperature I_{SB1} vs. Supply Voltage I_{SB1} vs. Temperature

NORMALIZED TYPICAL DC AND AC CHARACTERISTICS

T-46-23-08



INTEGRATED DEVICE

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IDT71681SA/LA AND IDT71682SA/LA
CMOS STATIC RAM 16K (4K x 4-BIT)

MILITARY AND COMMERCIAL TEMPERATURE RANGES

ORDERING INFORMATION

T-46-23-08

IDT	XXXXX Device Type	A Power	999 Speed	A Package	A Process/ Temperature Range	
						Blank
						B
						Y
						P
						D
						L
						SO
						E
						F
						12
						15
						20
						25
						35
						45
						55
						70
						85
						100
						SA
						LA
						71681
						71682

Commercial (0°C to +70°C)

Military (-55°C to +125°C)
Compliant to MIL-STD-883, Class B

Small Outline IC (J-Bend)
Plastic DIP
CERDIP
Leadless Chip Carrier
Small Outline IC (Gull-Wing)
CERPACK
Flatpack

Commercial Only

Military Only
Military Only
Military Only
Military Only

Standard Power
Low Power

16K (4K x 4-Bit) Outputs Follow Inputs
16K (4K x 4-Bit) High Impedance Outputs

Speed In Nanoseconds

4