

T-46-23-10



Integrated Device Technology, Inc.

CMOS STATIC RAM
64K (16K x 4-BIT)
IDT7188S
IDT7188L
FEATURES:

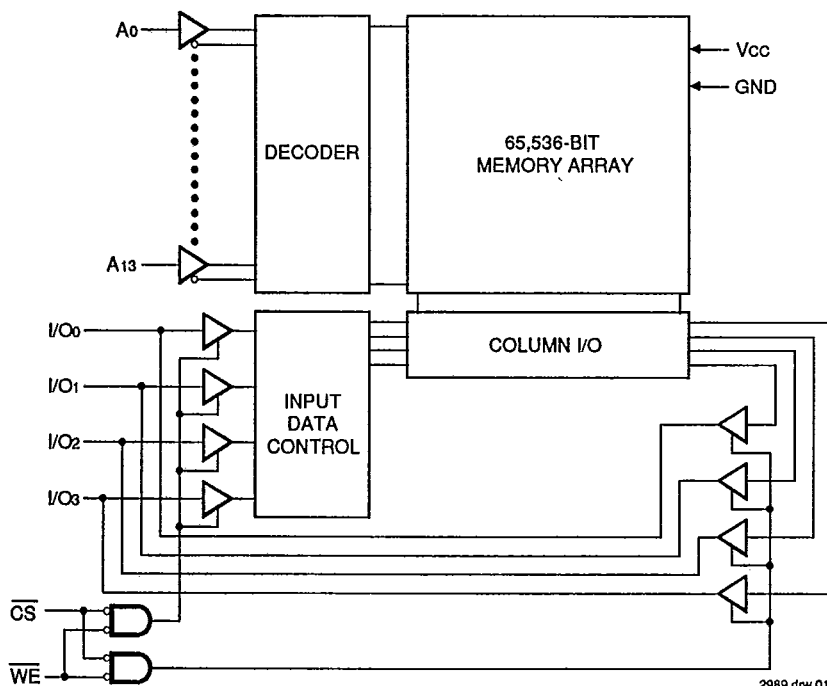
- High-speed (equal access and cycle times)
 - Military: 20/25/35/45/55/70/85ns (max.)
 - Commercial: 15/20/25/35ns (max.)
- Low power consumption
 - IDT7188S
 - Active: 350mW (typ.)
 - Standby: 100μW (typ.)
 - IDT7188L
 - Active: 300mW (typ.)
 - Standby: 30μW (typ.)
- Battery backup operation — 2V data retention (L version only)
- Available in high-density industry standard 22-pin, 300 mil ceramic and plastic DIP, 24-pin SOIC, 24-pin CERPACK
- Produced with advanced CEMOS™ technology
- Single 5V (+ 10%) power supply
- Inputs/outputs TTL-compatible
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7188 is a 65,536-bit high-speed static RAM organized as 16K x 4. It is fabricated using IDT's high-performance, high-reliability technology — CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective approach for memory intensive applications.

Access times as fast as 15ns are available, with typical power consumption of only 300mW. The IDT7188 offers a reduced power standby mode, ISB1, which enables the designer to greatly reduce device power requirements. This capability significantly decreases system power and cooling levels, while greatly enhancing system reliability. The low-power version (L) version also offers a battery backup data retention capability where the circuit typically consumes only 30μW operating from a 2V battery.

All inputs and outputs are TTL-compatible and operate from a single 5V supply. The IDT7188 is packaged in 22-pin, 300 mil ceramic and plastic DIPs, 24-pin SOICs, (gull-wing and J-bend) and CERPACKs, providing excellent board-level packing densities.

FUNCTIONAL BLOCK DIAGRAM

CEMOS is a trademark of Integrated Device Technology, Inc.

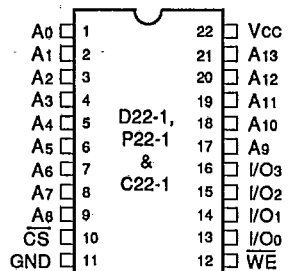
MILITARY AND COMMERCIAL TEMPERATURE RANGES**DECEMBER 1990**

IDT7188S/L
CMOS STATIC RAM 64K (16K x 4-BIT)

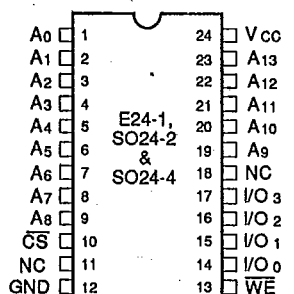
MILITARY AND COMMERCIAL TEMPERATURE RANGES

DESCRIPTION (Continued)

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

PIN CONFIGURATIONS

DIP
TOP VIEW



CERPACK/SOIC/SOJ
TOP VIEW

PIN DESCRIPTIONS

Name	Description
A0-A13	Address Inputs
CS	Chip Select
WE	Write Enable
I/O0-3	Data Input/Output
Vcc	Power
GND	Ground

2989 tbl 01

TRUTH TABLE⁽¹⁾

Mode	CS	WE	I/O	Power
Standby	H	X	High Z	Standby
Read	L	H	DOUT	Active
Write	L	L	DIN	Active

NOTE:

1. H = V_{IH}, L = V_{IL}, X = don't care.

2989 tbl 02

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
PT	Power Dissipation	1.0	1.0	W
IOUT	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2989 tbl 03

CAPACITANCE (TA = +25°C, f = 1.0MHz, Vcc = 0V)

Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
CIN	Input Capacitance	V _{IN} = 0V	6	pF
COUT	Output Capacitance	V _{OUT} = 0V	6	pF

NOTE:

1. This parameter is determined by device characterization, but is not production tested.

2989 tbl 04

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V _{IH}	Input High Voltage	2.2	—	6.0	V
V _{IL}	Input Low Voltage	-0.5 ⁽¹⁾	—	0.8	V

NOTE:

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

2989 tbl 05

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2989 tbl 06

IDT7188S/L
CMOS STATIC RAM 64K (16K x 4-BIT)

MILITARY AND COMMERCIAL TEMPERATURE RANGES

DC ELECTRICAL CHARACTERISTICS

VCC = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT7188S		IDT7188L		Unit
			Min.	Max.	Min.	Max.	
I _{LI}	Input Leakage Current	VCC = Max., VIN = GND to VCC	MIL. COM'L.	— 10 5	— 5 2	— 5 2	μA
I _{LO}	Output Leakage Current	VCC = Max., $\overline{CS}$ = VIH, VOUT = GND to VCC	MIL. COM'L.	— 10 5	— 5 2	— 5 2	μA
VOL	Output Low Voltage	IOL = 10mA, VCC = Min.		0.5	—	0.5	V
		IOL = 8mA, VCC = Min.		—	0.4	0.4	
VOH	Output High Voltage	IOL = -4mA, VCC = Min.	2.4	—	2.4	—	V

2989 tkl 07

DC ELECTRICAL CHARACTERISTICS⁽¹⁾(VCC = 5V ± 10%, V_{LC} = 0.2V, V_{HC} = VCC - 0.2V)

Symbol	Parameter	Power	7188S15 7188L15		7188S20 7188L20		7188S25 7188L25		7188S35 7188L35		7188S45 7188L45		7188S55/70 7188L55/70		7188S85 7188L85		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
Icc1	Operating Power Supply Current $\overline{CS}$ = VIL, Outputs Open VCC = Max., f = 0 ⁽²⁾	S	90	—	110	110	100	105	100	110	—	110	—	110	—	110	mA
		L	75	—	70	80	70	80	85	95	—	95	—	95	—	95	
Icc2	Dynamic Operating Current $\overline{CS}$ = VIL, Outputs Open VCC = Max., f = fMAX ⁽²⁾	S	135	—	130	160	135	155	125	140	—	140	—	140	—	140	mA
		L	125	—	115	130	105	120	105	115	—	110	—	110	—	105	
ISB	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ VIH, VCC = Max., Outputs Open, f = fMAX ⁽²⁾	S	60	—	55	70	55	60	45	50	—	50	—	50	—	50	mA
		L	45	—	40	50	35	40	35	40	—	35	—	35	—	35	
ISB1	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ VHC, VCC = Max., VIN ≥ VHC or VIN ≤ VLC, f = 0 ⁽²⁾	S	20	—	15	25	15	20	15	20	—	20	—	20	—	20	mA
		L	1.5	—	0.5	1.5	0.5	1.5	0.5	1.5	—	1.5	—	1.5	—	1.5	

NOTES:

2989 tkl 08

- All values are maximum guaranteed values.
- At f = fMAX address and data inputs are cycling at the maximum frequency of read cycles of 1/trc. f = 0 means no input lines change.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

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(L Version Only) $V_{HC} = V_{CC} - 0.2V$

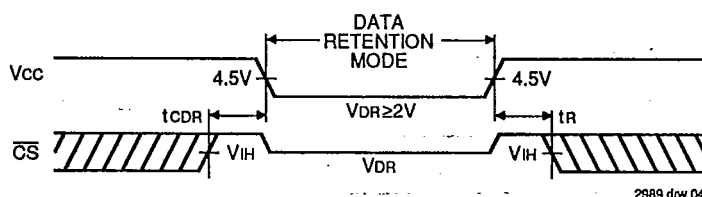
Symbol	Parameter	Test Condition	Min.	Typ. ⁽¹⁾ V _{CC} @		Max. V _{CC} @		Unit
				2.0V	3.0V	2.0V	3.0V	
V _{DR}	V _{CC} for Data Retention	—	2.0	—	—	—	—	V
I _{CCDR}	Data Retention Current	MIL. COM'L.	— —	10 10	15 15	600 150	900 225	μA
t _{CDR} ⁽³⁾	Chip Deselect to Data Retention Time	$\overline{CS} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	0	—	—	—	—	ns
t _R ⁽³⁾	Operation Recovery Time		t _{RC} ⁽²⁾	—	—	—	—	ns
I _L ⁽³⁾	Input Leakage Current		—	—	—	2	2	μA

NOTES:

1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed, but not tested.

2989 tdx 09

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2989 tdx 10

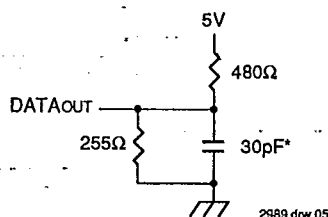


Figure 1. Output Load

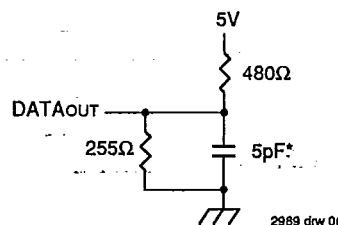


Figure 2. Output Load
(for tHZ, tLZ, tWZ, tOHZ and tOW)

*Includes scope and jig capacitances

IDT7188S/L
CMOS STATIC RAM 64K (16K x 4-BIT)

MILITARY AND COMMERCIAL TEMPERATURE RANGES

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%, All Temperature Ranges)

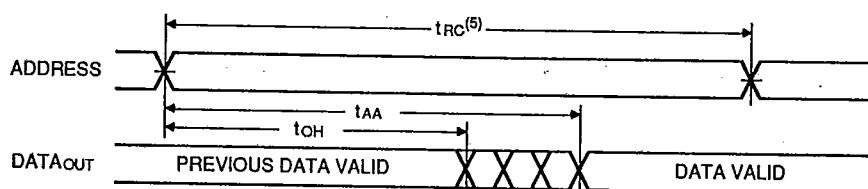
T-46-23-10

		7188S15 ⁽¹⁾ 7188L15 ⁽¹⁾		7188S20 7188L20		7188S25 7188L25		7188S35/45 7188L35/45		7188S55/70 ⁽²⁾ 7188L55/70 ⁽²⁾		7188S85 ⁽²⁾ 7188L85 ⁽²⁾		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
Read Cycle														
t _{RC}	Read Cycle Time	15	—	20	—	25	—	35/45	—	55/70	—	85	—	ns
t _{AA}	Address Access Time	—	15	—	20	—	25	—	35/45	—	55/70	—	85	ns
t _{ACS}	Chip Select Access Time	—	15	—	20	—	25	—	35/45	—	55/70	—	85	ns
t _{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	5	—	ns
t _{LZ}	Output Selection to Output in Low Z ⁽³⁾	5	—	5	—	5	—	5	—	5	—	5	—	ns
t _{HZ}	Chip Deselect to Output in High Z ⁽³⁾	—	7	—	8	—	10	—	14	—	20/25	—	30	ns
t _{PU}	Chip Select to Power Up Time ⁽³⁾	0	—	0	—	0	—	0	—	0	—	0	—	ns
t _{PD}	Chip Deselect to Power Down Time ⁽³⁾	—	15	—	20	—	25	—	35/45	—	55/70	—	85	ns

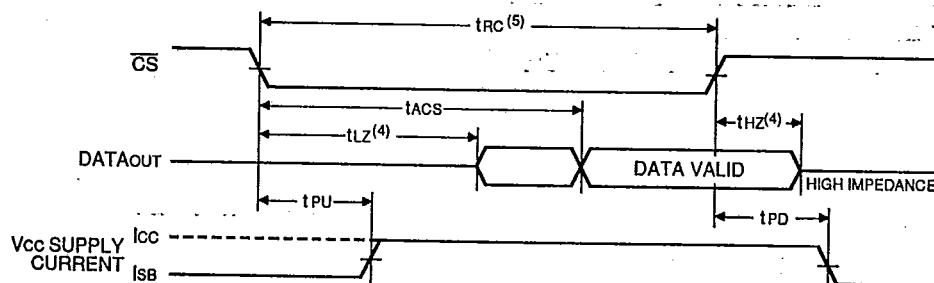
NOTES:

- 0° to +70°C temperature range only.
- 55°C to +125°C temperature range only.
- This parameter guaranteed but not tested.

2989 tbl 11

TIMING WAVEFORM OF READ CYCLE NO. 1^(1, 2)

2989 drw 07

TIMING WAVEFORM OF READ CYCLE NO. 2^(1, 3)

2971 drw 08

NOTES:

- WE is high for read cycle.
- CS is low for READ cycle.
- Address valid prior to or coincident with CS transition low.
- Transition is measured ±200mV from steady state voltage.
- All READ cycle timings are referenced from the last valid address to the first transitioning address.

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MILITARY AND COMMERCIAL TEMPERATURE RANGES

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%, All Temperature Ranges) T-46-23-10

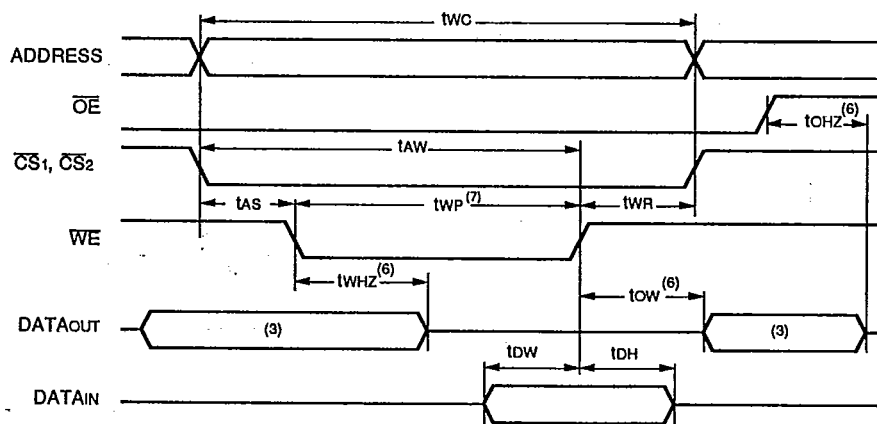
Symbol	Parameter	7188S15 ⁽¹⁾ 7188L15 ⁽¹⁾		7188S20 7188L20		7188S25 7188L25		7188S35/45 ⁽²⁾ 7188L35/45 ⁽²⁾		7188S55/70 ⁽²⁾ 7188L55/70 ⁽²⁾		7188S85 ⁽²⁾ 7188L85 ⁽²⁾		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle														
tWC	Write Cycle Time	14	—	17	—	20	—	30/40	—	50/60	—	75	—	ns
tcw	Chip Select to End of Write	14	—	17	—	20	—	25/35	—	50/60	—	75	—	ns
tAW	Address Valid to End of Write	14	—	17	—	20	—	25/35	—	50/60	—	75	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	14	—	17	—	20	—	25/35	—	50/60	—	75	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tdw	Data Valid to End of Write	10	—	10	—	13	—	15/20	—	25/30	—	35	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tWZ	Write Enable to Output in High Z ⁽³⁾	—	5	—	6	—	7	—	10/15	—	25/30	—	40	ns
tOW	Output Active from End of Write ⁽³⁾	5	—	5	—	5	—	5	—	5	—	5	—	ns

NOTES:

- 0° to +70°C temperature range only.
- 55°C to +125°C temperature range only.
- This parameter guaranteed but not tested.

2989 lbt 12

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (WE CONTROLLED TIMING)^(1, 2, 3)



NOTES:

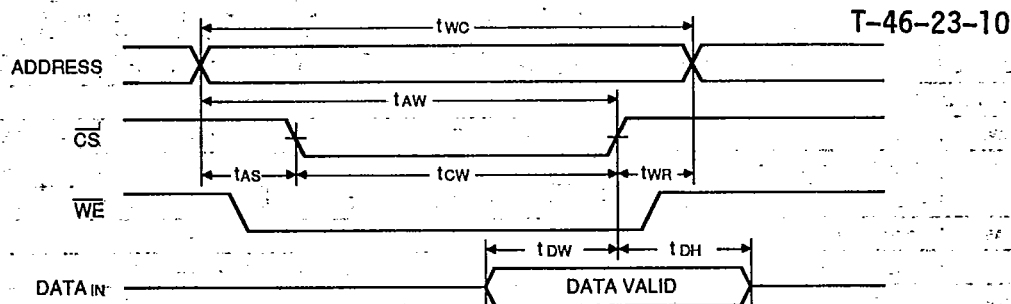
- WE or CS must be high during all address transitions.
- A write occurs during the overlap (t_{WP}) of a low CS and a low WE.
- t_{WR} is measured from the earlier of CS or WE going high to the end of the write cycle.
- During this period, I/O pins are in the output state so that the input signals should not be applied.
- If the CS low transition occurs simultaneously with or after the WE low transition, the outputs remain in the high impedance state.
- Transition is measured ±200mV from steady state.

2999 drw 06

IDT7188S/L
CMOS STATIC RAM 64K (16K x 4-BIT)

MILITARY AND COMMERCIAL TEMPERATURE RANGES

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)^(1,2,3,5)



NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals should not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured $\pm 200\text{mV}$ from steady state.

ORDERING INFORMATION

IDT	XXXX	X	XX	XX	X	
Device Type	Power	Speed	Package	Process/ Temperature Range		
				Blank	Commercial (0°C to +70°C)	
				B	Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B	
				C	Sidebrazed DIP	
				D	Ceramic DIP	
				P	Plastic DIP	
				SO	Small Outline IC (Gull Wing)	
				Y	Small Outline IC (J-Bend)	
				E	CERPACK	
				15	Commercial Only	} Speed in Nanoseconds
				20		
				25		
				35		
				45	Military Only	
				55	Military Only	
				70	Military Only	
				85	Military Only	
				S	Standard Power	
				L	Low Power	
				7188	64K (16K x 4-Bit)	

2989 drw 11