



IDT7198L

Added Chip Select and Output Controls

T.46-23-10

- Fast Output Enable (\overline{OE}) pin available for added system flexibility
- Multiple Chip Selects (\overline{CS}_1 , \overline{CS}_2) simplify system design and operation
- High speed (equal access and cycle times)
 - Military: 20/25/35/45/55/70/85ns (max.)
 - Commercial: 15/20/25/35ns (max.)
- Low power consumption
- Battery back-up operation—2V data retention (L version only)
- 24-pin Cerdip, 24-pin plastic DIP, high-density 28-pin leadless chip carrier, 24-pin SOJ and CERPACK
- Produced with advanced CMOS technology
- Bidirectional data inputs and outputs
- Inputs/outputs TTL-compatible
- Military product compliant to MIL-STD-883, Class B

The IDT7198 is a 65,536 bit high-speed static RAM organized as 16K x 4. It is fabricated using IDT's high-perfor-

Access times as fast as 15ns are available. The IDT7198 offers a reduced power standby mode, ISB1, which is activated when CS1 or CS2 goes high. This capability decreases power, while enhancing system reliability. The low-power version (L) also offers a battery backup data retention capability where the circuit typically consumes only 30µW when operating from a 2V battery.

All inputs and outputs are TTL-compatible and operate from a single 5 volt supply.

The IDT7198 is packaged in either a 24-pin ceramic DIP, 24-pin plastic DIP, 28-pin leadless chip carrier, 24-pin SOJ and 24-pin CERPACK.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

2985 drw 01

MILITARY AND COMMERCIAL TEMPERATURE RANGES

SEPTEMBER 1992

IDT7198S/L CMOS STATIC RAMS

64K (16K x 4-BIT) Added Chip Select and Output Enable Controls

MILITARY AND COMMERCIAL TEMPERATURE RANGES

MEMORY CONTROL

The IDT7198 64K high-speed CMOS static RAM incorporates two additional memory control features (an extra chip select and an output enable pin) which offer additional benefits in many system memory applications.

The dual chip select feature (\overline{CS}_1 , \overline{CS}_2) now brings the convenience of improved system speeds to the large memory designer by reducing the external logic required to perform decoding.

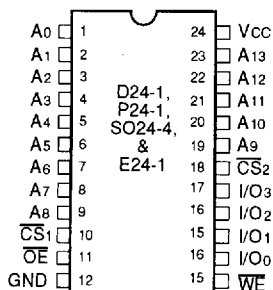
Both chip selects, Chip Select 1 (\overline{CS}_1) and Chip Select 2 (\overline{CS}_2), must be in the active-low state to select the memory. If either chip select is pulled high, the memory will be deselected and remain in the standby mode.

PIN DESCRIPTIONS

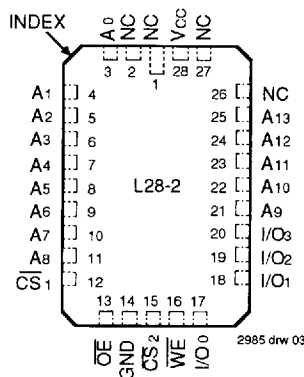
Name	Description
A0-A13	Address Inputs
\overline{CS}_1	Chip Select 1
\overline{CS}_2	Chip Select 2
WE	Write Enable
\overline{OE}	Output Enable
I/O0-I/O3	Data I/O
VCC	Power
GND	Ground

2985 tbi/01

PIN CONFIGURATIONS



2985 drw 02

DIP/SOJ/CERPACK
TOP VIEW

2985 drw 03

LCC
TOP VIEWTRUTH TABLE⁽¹⁾

Mode	\overline{CS}_1	\overline{CS}_2	WE	\overline{OE}	I/O	Power
Standby	H	X	X	X	High Z	Standby
Standby	X	H	X	X	High Z	Standby
Read	L	L	H	L	DOUT	Active
Write	L	L	L	X	DIN	Active
Read	L	L	H	H	High Z	Active

NOTE:

1. H = V_{IH} , L = V_{IL} , X = don't care.

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IDT7198S/L CMOS STATIC RAMS
64K (16K x 4-BIT) Added Chip Select and Output Enable Controls

MILITARY AND COMMERCIAL TEMPERATURE RANGES

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Com'l.	MIL.	Unit
V _{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T _A	Operating Temperature	0 to +70	-55 to +125	°C
T _{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T _{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P _T	Power Dissipation	1.0	1.0	W
I _{OUT}	DC Output Current	50	50	mA

NOTE:

2985 tbl 03

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz, V_{CC} = 0V)

Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	7	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	7	pF

NOTE:

2985 tbl 04

- This parameter is determined by device characterization, but is not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V _{IH}	Input High Voltage	2.2	—	6.0	V
V _{IL}	Input Low Voltage	-0.5 ⁽¹⁾	—	0.8	V

NOTE:

2985 tbl 05

- V_{IL} (min.) = -3.0V for pulse width less than 20ns, once per cycle.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	V _{CC}
Military	-55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2985 tbl 06

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT7198S		IDT7198L		Unit
			Min.	Max.	Min.	Max.	
I _{LI}	Input Leakage Current	V _{CC} = Max., V _{IN} = GND to V _{CC}	MIL. COM'L.	— 10 5	— 5 2	— 5 2	μA
I _{LO}	Output Leakage Current	V _{CC} = Max., \overline{CS} = V _{IH} , V _{OUT} = GND to V _{CC}	MIL. COM'L.	— 10 5	— 5 2	— 5 2	μA
V _{OL}	Output Low Voltage	I _{OL} = 10mA, V _{CC} = Min. I _{OL} = 8mA, V _{CC} = Min.	— —	0.5 0.4	— —	0.5 0.4	V
V _{OH}	Output High Voltage	I _{OH} = -4mA, V _{CC} = Min.	2.4	—	2.4	—	V

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IDT7198S/L CMOS STATIC RAMS

64K (16K x 4-BIT) Added Chip Select and Output Enable Controls

MILITARY AND COMMERCIAL TEMPERATURE RANGES

DC ELECTRICAL CHARACTERISTICS⁽¹⁾(VCC = 5V ± 10%, V_{LC} = 0.2V, V_{HC} = VCC - 0.2V)

Symbol	Parameter	Power	7198S15 7198L15		7198S20 7198L20		7198S25 7198L25		7198S35 7198L35		7198S45 7198L45		7198S55/70 7198L55/70		7198S85 7198L85		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
ICC1	Operating Power Supply Current, \overline{CS}_1 and $\overline{CS}_2 \leq V_{IL}$, Outputs Open VCC = Max., f = 0 ⁽²⁾	S	100	—	100	105	100	105	100	105	—	105	—	105	—	105	mA
		L	75	—	70	80	70	80	70	80	—	80	—	80	—	80	
ICC2	Dynamic Operating Current, \overline{CS}_1 and $\overline{CS}_2 \leq V_{IL}$, Outputs Open VCC = Max., f = f _{MAX} ⁽²⁾	S	135	—	130	160	125	155	125	140	—	140	—	140	—	140	mA
		L	125	—	115	130	105	120	105	115	—	110	—	110	—	105	
ISB	Standby Power Supply Current (TTL Level), \overline{CS}_1 or $\overline{CS}_2 \geq V_{IH}$, VCC = Max., Outputs Open, f = f _{MAX} ⁽²⁾	S	60	—	55	70	50	60	45	50	—	50	—	50	—	50	mA
		L	45	—	40	50	35	40	30	35	—	35	—	35	—	35	
ISB1	Full Standby Power Supply Current (CMOS Level) \overline{CS}_1 or $\overline{CS}_2 \geq V_{HC}$, VCC = Max., V _{IN} ≥ V _{HC} or V _{IN} ≤ V _{LC} , f = 0 ⁽²⁾	S	20	—	15	25	15	20	15	20	—	20	—	20	—	20	mA
		L	1.5	—	0.5	1.5	0.5	1.5	0.5	1.5	—	1.5	—	1.5	—	1.5	

NOTES:

1. All values are maximum guaranteed values.
2. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of 1/trc. f = 0 means no input lines change.

2985 tbl 06

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) V_{LC} = 0.2V, V_{HC} = VCC - 0.2V

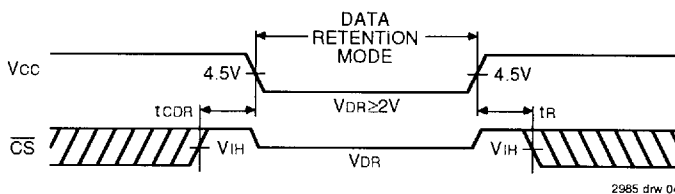
Symbol	Parameter	Test Condition	Min.	Typ. ⁽¹⁾ VCC @		Max. VCC @		Unit
				2.0V	3.0V	2.0V	3.0V	
VDR	VCC for Data Retention	—	2.0	—	—	—	—	V
ICCDR	Data Retention Current	\overline{CS}_1 or $\overline{CS}_2 \geq V_{HC}$ V _{IN} ≥ V _{HC} or ≤ V _{LC}	MIL.	—	10	15	600	900
			COM'L.	—	10	15	150	225
t _{CDR} ⁽³⁾	Chip Deselect to Data Retention Time		0	—	—	—	—	ns
t _{IR} ⁽³⁾	Operation Recovery Time		t _{RC} ⁽²⁾	—	—	—	—	ns
I _{IL} ⁽³⁾	Input Leakage Current		—	—	—	2	2	μA

NOTES:

1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed by device characterization but is not production tested.

2985 tbl 09

LOW VCC DATA RETENTION WAVEFORM



IDT7198S/L CMOS STATIC RAMS
64K (16K x 4-BIT) Added Chip Select and Output Enable Controls

MILITARY AND COMMERCIAL TEMPERATURE RANGES

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

2985 tbl 10

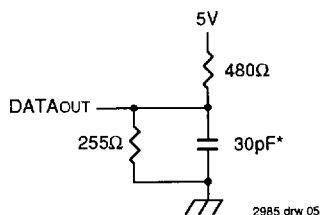


Figure 1. AC Test Load

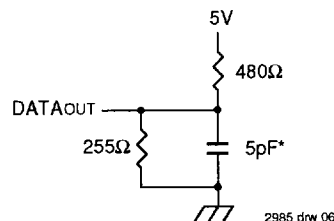


Figure 2. AC Test Load
(for tCLZ1, 2, tOLZ, tCHZ1, 2, tOHZ, tOW and tWHZ)

*Includes scope and jig capacitances

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%, All Temperature Ranges)

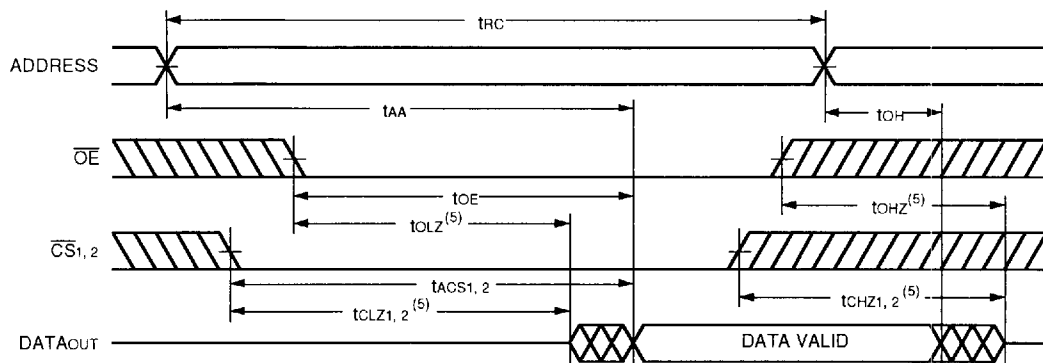
Symbol	Parameter	7198S15 ⁽¹⁾ /20 7198L15 ⁽¹⁾ /20		7198S25 7198L25		7198S35/45 ⁽²⁾ 7198L35/45 ⁽²⁾		7198S55 ⁽²⁾ 7198L55 ⁽²⁾		7198S70 ⁽²⁾ 7198L70 ⁽²⁾		7198S85 ⁽²⁾ 7198L85 ⁽²⁾		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle														
tRC	Read Cycle Time	15/20	—	25	—	35/45	—	55	—	70	—	85	—	ns
tAA	Address Access Time	—	15/19	—	25	—	35/45	—	55	—	70	—	85	ns
tACS1,2	Chip Select-1,2 Access Time ⁽³⁾	—	15/20	—	25	—	35/45	—	55	—	70	—	85	ns
tCLZ1,2	Chip Select-1,2 to Output in Low Z ⁽⁴⁾	5	—	5	—	5	—	5	—	5	—	5	—	ns
tOE	Output Enable to Output Valid	—	8/9	—	11	—	20/25	—	35	—	45	—	55	ns
tOLZ	Output Enable to Output in Low Z ⁽⁴⁾	5	—	5	—	5	—	5	—	5	—	5	—	ns
tCHZ1,2	Chip Select 1,2 to Output in High Z ⁽⁴⁾	—	7/8	—	10	—	14	—	20	—	25	—	30	ns
tOHZ	Output Disable to Output in High Z ⁽⁴⁾	—	7/8	—	9	—	15	—	20	—	25	—	30	ns
tOH	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	5	—	ns
tPU	Chip Select to Power Up Time ⁽⁴⁾	0	—	0	—	0	—	0	—	0	—	0	—	ns
tPD	Chip Deselect to Power Down Time ⁽⁴⁾	—	15/20	—	25	—	35/45	—	55	—	70	—	85	ns

NOTES:

- 0°C to +70°C temperature range only.
- −55°C to +125°C temperature range only.
- Both chip selects must be active low for the device to be selected.
- This parameter is guaranteed by device characterization but is not production tested.

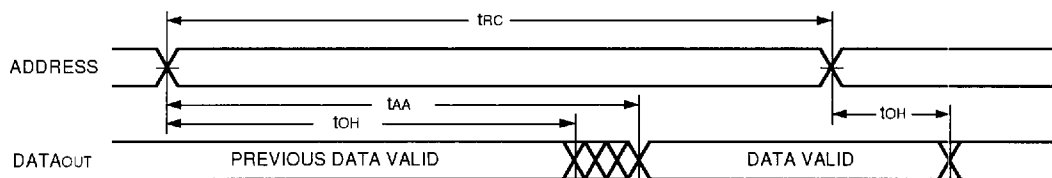
2985 tbl 11

TIMING WAVEFORM OF READ CYCLE NO. 1⁽¹⁾



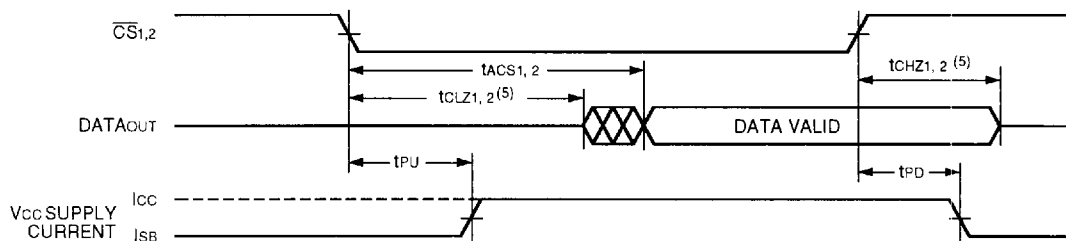
2985 drw 07

TIMING WAVEFORM OF READ CYCLE NO. 2^(1, 2, 4)



2985 drw 08

TIMING WAVEFORM OF READ CYCLE NO. 3^(1, 3, 4)



2985 drw 09

NOTES:

- WE is HIGH for READ cycle.
- Device is continuously selected, CS1 = VIL, CS2 = VIL.
- Address valid prior to or coincident with CS1 and or CS2 transition low.
- OE = VIL.
- Transition is measured $\pm 200\text{mV}$ from steady state voltage.

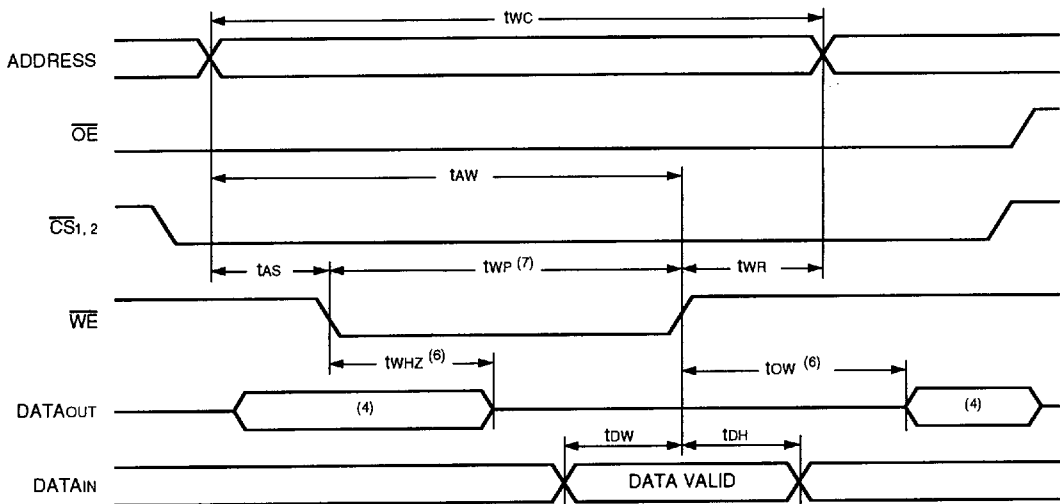
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	7198S15 ⁽¹⁾ /20 7198L15 ⁽¹⁾ /20		7198S25 7198L25		7198S35/45 ⁽²⁾ 7198L35/45 ⁽²⁾		7198S55 ⁽²⁾ 7198L55 ⁽²⁾		7198S70 ⁽²⁾ 7198L70 ⁽²⁾		7198S85 ⁽²⁾ 7198L85 ⁽²⁾		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle														
tWC	Write Cycle Time	14/17	—	20	—	30/40	—	50	—	60	—	75	—	ns
tCW1,2	Chip Select to End-of-Write ⁽³⁾	14/17	—	20	—	25/35	—	50	—	60	—	75	—	ns
tAW	Address Valid to End-of-Write	14/17	—	20	—	25/35	—	50	—	60	—	75	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	14/17	—	20	—	25/35	—	50	—	60	—	75	—	ns
tWR1,2	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tWHZ	Write Enable to Output in High-Z ⁽⁴⁾	—	5/6	—	7	—	10/15	—	25	—	30	—	40	ns
tDW	Data Valid to End-of-Write	10	—	13	—	15/20	—	25	—	30	—	35	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	0	—	ns
tOW	Output Active from End-of-Write ⁽⁴⁾	5	—	5	—	5	—	5	—	5	—	5	—	ns

NOTES:

- 0° to +70°C temperature range only.
- 55°C to +125°C temperature range only.
- Both chip selects must be active low for the device to be selected.
- This parameter is guaranteed by device characterization but is not production tested.

2985 tbl 12

TIMING WAVEFORM OF WRITE CYCLE NO. 1 (WE CONTROLLED TIMING)^(1, 2, 3, 7)

2985 drw 10

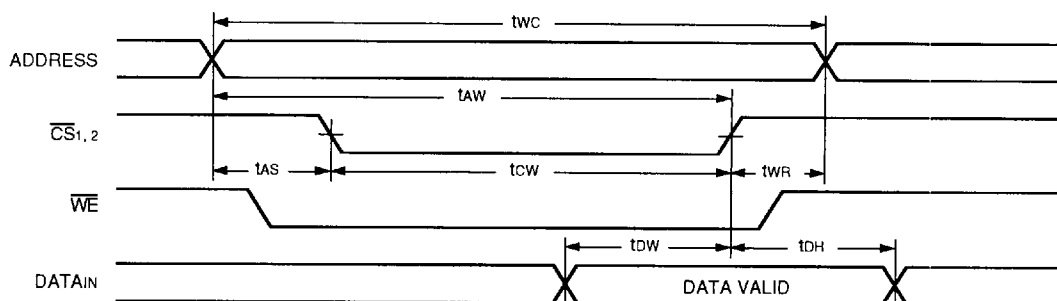
NOTES:

- WE, CS₁ or CS₂ must be HIGH during all address transitions.
- A write occurs during the overlap (t_{WP}) of a LOW WE, a low CS₁ and a LOW CS₂.
- t_{WR} is measured from the earlier of CS₁, CS₂ or WE going HIGH to the end of the write cycle.
- During this period, the I/O pins are in the output state, and input signals must not be applied.
- If the CS low transition occurs simultaneously with or after the WE low transition, outputs remain in the high-impedance state.
- Transition is measured ±200mV from steady state.
- If OE is LOW during a WE controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the required t_{OW}. If OE is HIGH during a WE controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

IDT7198S/L CMOS STATIC RAMS

64K (16K x 4-BIT) Added Chip Select and Output Enable Controls

MILITARY AND COMMERCIAL TEMPERATURE RANGES

TIMING WAVEFORM OF WRITE CYCLE NO. 2 (\overline{CS} CONTROLLED TIMING)⁽¹⁾

2985 drw 11

NOTES:

1. \overline{WE} , \overline{CS}_1 or \overline{CS}_2 must be HIGH during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a LOW \overline{WE} , a LOW \overline{CS}_1 and a LOW \overline{CS}_2 .
3. t_{WR} is measured from the earlier of \overline{CS}_1 , \overline{CS}_2 or \overline{WE} going HIGH to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and input signals must not be applied.
5. If the \overline{CS} low transition occurs simultaneously with or after the \overline{WE} low transition, outputs remain in the high-impedance state.
6. Transition is measured $\pm 200\text{mV}$ from steady state.
7. If \overline{OE} is LOW during a \overline{WE} controlled write cycle, the write pulse width must be the larger of t_{WP} or ($t_{WHZ} + t_{DW}$) to allow the I/O drivers to turn off and data to be placed on the required t_{OW} . If \overline{OE} is HIGH during a \overline{WE} controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP} .

ORDERING INFORMATION

IDT7198	X	XX	X	X	
Device Type	Power	Speed	Package	Process/ Temperature Range	
				Blank	Commercial (0°C to +70°C)
				B	Military (-55°C to +125°C) Compliant to MIL-STD-883, Class B
				D	300 mil Ceramic DIP (D24-1)
				P	300 mil Plastic DIP (P24-1)
				L	Leadless Chip Carrier (L28-2)
				Y	Small Outline IC, J-Bend (SO24-4)
				E	CERPACK (E24-1)
				15	Commercial Only
				20	
				25	
				35	
				45	Military Only
				55	Military Only
				70	Military Only
				85	Military Only
				S	Standard Power
				L	Low Power

Speed in nanoseconds

2985 drw 12