



Integrated Device Technology, Inc.

BiCMOS STATIC RAM 1 MEG (128K x 8-BIT) REVOLUTIONARY PINOUT

**ADVANCE
INFORMATION
IDT71B124**

FEATURES:

- 128K x 8 advanced high-speed BiCMOS static RAM
- JEDEC revolutionary pinout (center power/GND) for reduced noise
- Equal access and cycle times
 - Commercial: 10/12/15ns
- One Chip Select plus one Output Enable pin
- Bidirectional inputs and outputs directly TTL-compatible
- Low power consumption via chip deselect
- Available in JEDEC 32-pin Plastic DIP and SOJ packages

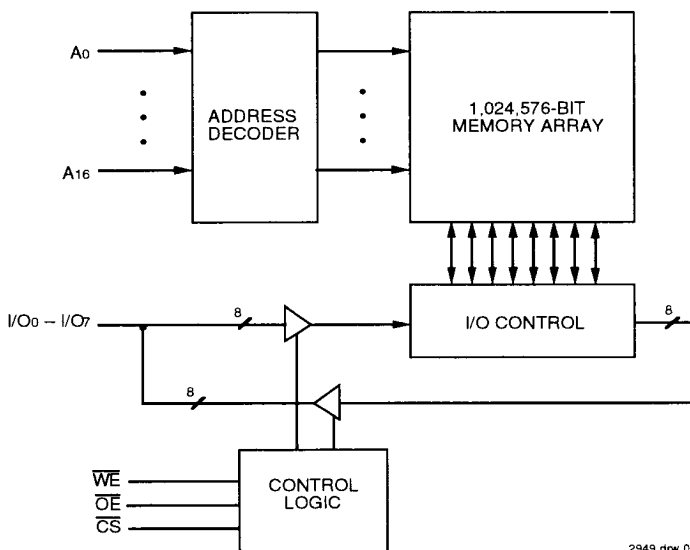
DESCRIPTION:

The IDT71B124 is a 1,024,576-bit high-speed Static RAM organized as 128Kx8. It is fabricated using IDT's high-performance, high-reliability BiCMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs. The JEDEC center pin power/GND pinout reduces noise generation and improves high speed system performance.

The IDT71B124 has an output enable pin which operates as fast as 5ns, with address access times as fast as 10ns available. All bidirectional inputs and outputs of the IDT71BR024 are TTL-compatible and operation is from a single 5V supply. Fully static asynchronous circuitry is used; no clocks or refresh are required for operation.

The IDT71B124 is packaged in 32-pin 400 mil Plastic DIP and 32-pin 400 mil Plastic SOJ packages.

FUNCTIONAL BLOCK DIAGRAM



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COMMERCIAL TEMPERATURE RANGE

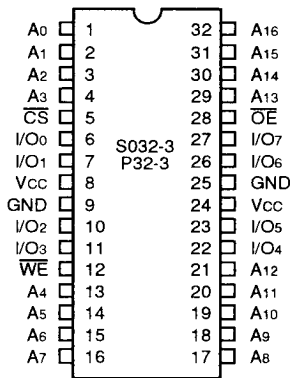
SEPTEMBER 1992

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PIN CONFIGURATION

DIP/SOJ
TOP VIEWABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Com'l.	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	-55 to +125	°C
TSTG	Storage Temperature	-55 to +125	°C
Pt	Power Dissipation	1.0	W
IOUT	DC Output Current	50	mA

NOTES:

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- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- VTERM must not exceed VCC + 0.5V.

TRUTH TABLE^(1,2)

CS	OE	WE	I/O	Function
L	L	H	DATAOUT	Read Data
L	X	L	DATAin	Write Data
L	H	H	High-Z	Outputs Disabled
H	X	X	High-Z	Deselected - Standby (Isb)
VHC ⁽³⁾	X	X	High-Z	Deselected - Standby (Isb1)

NOTES:

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- H = VIH, L = VIL, X = Don't care.
- VLC = 0.2V, VHC = VCC - 0.2V.
- Other inputs ≥ VHC or ≤ VLC.

CAPACITANCE

(TA = +25°C, f = 1.0MHz, SOJ package)

Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
Cin	Input Capacitance	VIN = 3dV	8	pF
CIO	I/O Capacitance	VOUT = 3dV	8	pF

NOTE:

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- This parameter is guaranteed by device characterization, but not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	VCC+0.5	V
VIL	Input Low Voltage	-0.5 ⁽¹⁾	—	0.8	V

NOTE:

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- VIL (min.) = -1.5V for pulse width less than 10ns, once per cycle.

DC ELECTRICAL CHARACTERISTICS

VCC = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT71B124		Unit
			Min.	Max.	
ILI	Input Leakage Current	VCC = Max., VIN = GND to VCC	—	5	μA
ILO	Output Leakage Current	VCC = Max., CS = VIH, VOUT = GND to VCC	—	5	μA
VOL	Output Low Voltage	IOL = 8mA, VCC = Min.	—	0.4	V
VOH	Output High Voltage	IOH = -4mA, VCC = Min.	2.4	—	V

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DC ELECTRICAL CHARACTERISTICS⁽¹⁾

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	71B124S10		71B124S12		71B124S15		Unit
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I _{CC}	Dynamic Operating Current, CS ≤ V _{IL} , Outputs Open, V _{CC} = Max., f = f _{MAX} ⁽²⁾	175	—	165	—	155	—	mA
I _{SB}	Standby Power Supply Current (TTL Level) CS ≥ V _{IH} , Outputs Open, V _{CC} = Max., f = f _{MAX} ⁽²⁾	35	—	30	—	30	—	mA
I _{SB1}	Full Standby Power Supply Current (CMOS Level) CS ≥ V _{HC} , Outputs Open, V _{CC} = Max., f = 0 ⁽²⁾ , V _{IN} ≤ V _{LC} or V _{IN} ≥ V _{HC}	12	—	12	—	12	—	mA

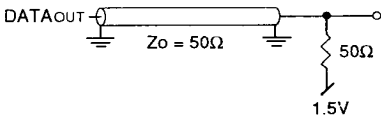
- NOTES:
1. All values are maximum guaranteed values.
2. f_{MAX} = 1/trc (all address inputs are cycling at f_{MAX}). f = 0 means no address input lines are changing.

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AC TEST CONDITIONS

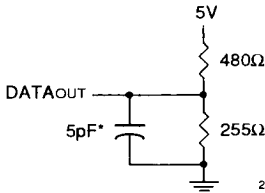
Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1, 2, and 3

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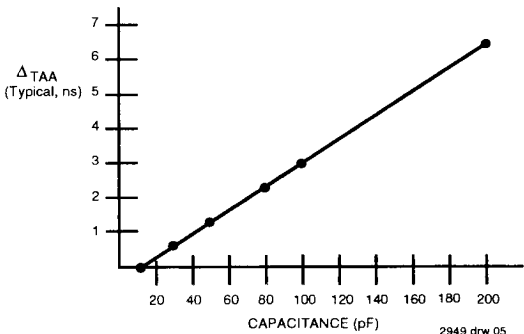
Figure 1. AC Test Load



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*Including jig and scope capacitance.

Figure 2. AC Test Load
(for tCLZ, tOLZ, tCHZ, tOHZ, tOW, and tWHZ)



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Figure 3. Lumped Capacitive Load, typical Derating

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%)

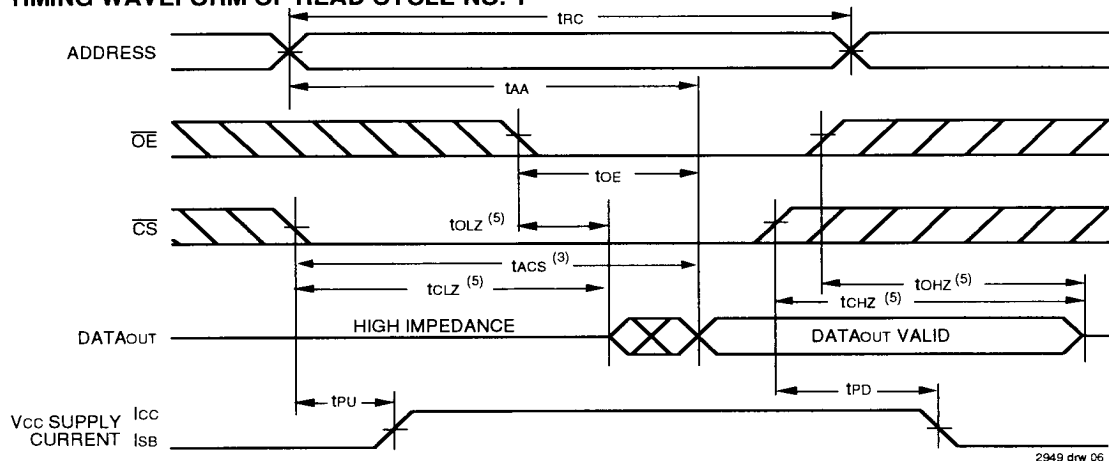
Symbol	Parameter	71B124S10		71B124S12		71B124S15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
tRC	Read Cycle Time	10	—	12	—	15	—	ns
tAA	Address Access Time	—	10	—	12	—	15	ns
tACS	Chip Select Access Time	—	10	—	12	—	15	ns
tCLZ ⁽¹⁾	Chip Select to Output in Low-Z	2	—	3	—	3	—	ns
tCHZ ⁽¹⁾	Chip Deselect to Output in High-Z	0	5	0	6	0	7	ns
tOE	Output Enable to Output Valid	—	5	—	6	—	7	ns
tOLZ ⁽¹⁾	Output Enable to Output in Low-Z	0	—	0	—	0	—	ns
tOHZ ⁽¹⁾	Output Disable to Output in High-Z	0	5	0	6	0	7	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	ns
tPU ⁽¹⁾	Chip Select to Power Up Time	0	—	0	—	0	—	ns
tPD ⁽¹⁾	Chip Deselect to Power Down Time	—	10	—	12	—	15	ns
Write Cycle								
tWC	Write Cycle Time	10	—	12	—	15	—	ns
tAW	Address Valid to End of Write	8	—	9	—	10	—	ns
tCW	Chip Select to End of Write	8	—	9	—	10	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWP	Write Pulse Width	8	—	9	—	10	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tDW	Data Valid to End of Write	6	—	7	—	8	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	ns
tOW ⁽¹⁾	Output Active from End of Write	3	—	3	—	3	—	ns
tWHZ ⁽¹⁾	Write Enable to Output in High-Z	0	5	0	6	0	7	ns

NOTE:

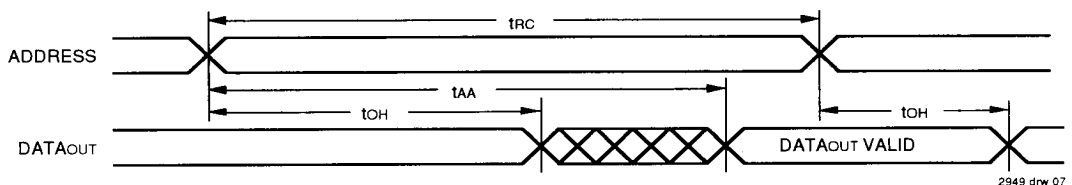
1. This parameter guaranteed with the AC load (Figure 2) by device characterization, but is not production tested.

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TIMING WAVEFORM OF READ CYCLE NO. 1⁽¹⁾



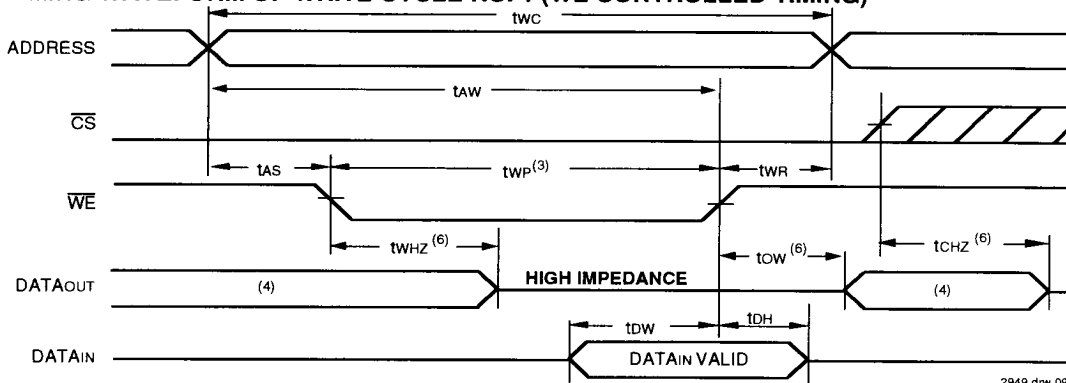
TIMING WAVEFORM OF READ CYCLE NO. 2^(1, 2, 4)



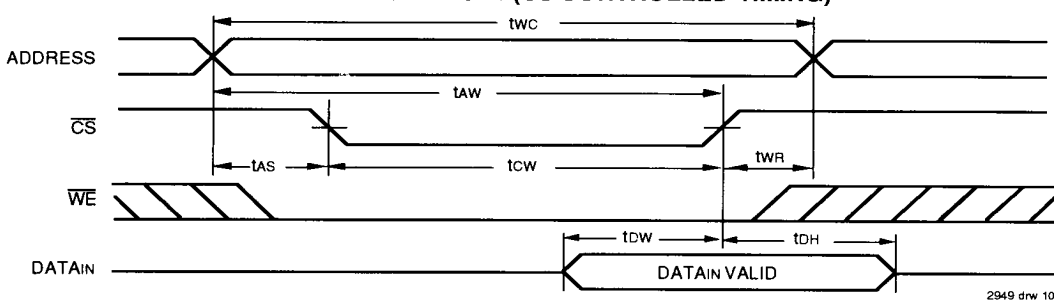
NOTES:

1. WE is HIGH for Read Cycle.
2. Device is continuously selected, CS is LOW.
3. Address must be valid prior to or coincident with the later of CS transition LOW; otherwise tAA is the limiting parameter.
4. OE is LOW.
5. Transition is measured $\pm 200\text{mV}$ from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)^(1, 2, 3, 5)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)^(1, 2, 5)



NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. $\overline{OE}$ is continuously HIGH. If during a $\overline{WE}$ controlled write cycle $\overline{OE}$ is LOW, t_{WP} must be greater than or equal to $t_{WHZ} + t_{OW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW} . If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse is the specified t_{WP} .
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high impedance state.
6. Transition is measured $\pm 200\text{mV}$ from steady state.

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ORDERING INFORMATION

IDT 71B124	S	XX	X	X	
Device Type	Power	Speed	Package	Process/ Temperature Range	
				Blank	Commercial (0°C to +70°C)
				P	400-mil Plastic DIP (P32-3)
				Y	400-mil SOJ (SO32-3)
				10	} Speed in nanoseconds
				12	
				15	

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