Integrated Device Technology, Inc.

BiCMOS STATIC RAM 64K (8K x 8-BIT)

IDT71B64

FEATURES:

- 8K x 8 organization
- JEDEC standard 28-pin DIP and SOJ
- Fast access time and cycle time
  — Commercial: 8/10/12 (max.)
- Produced with advanced BiCMOS high-performance technology
- Bidirectional inputs and outputs directly TTL compatible

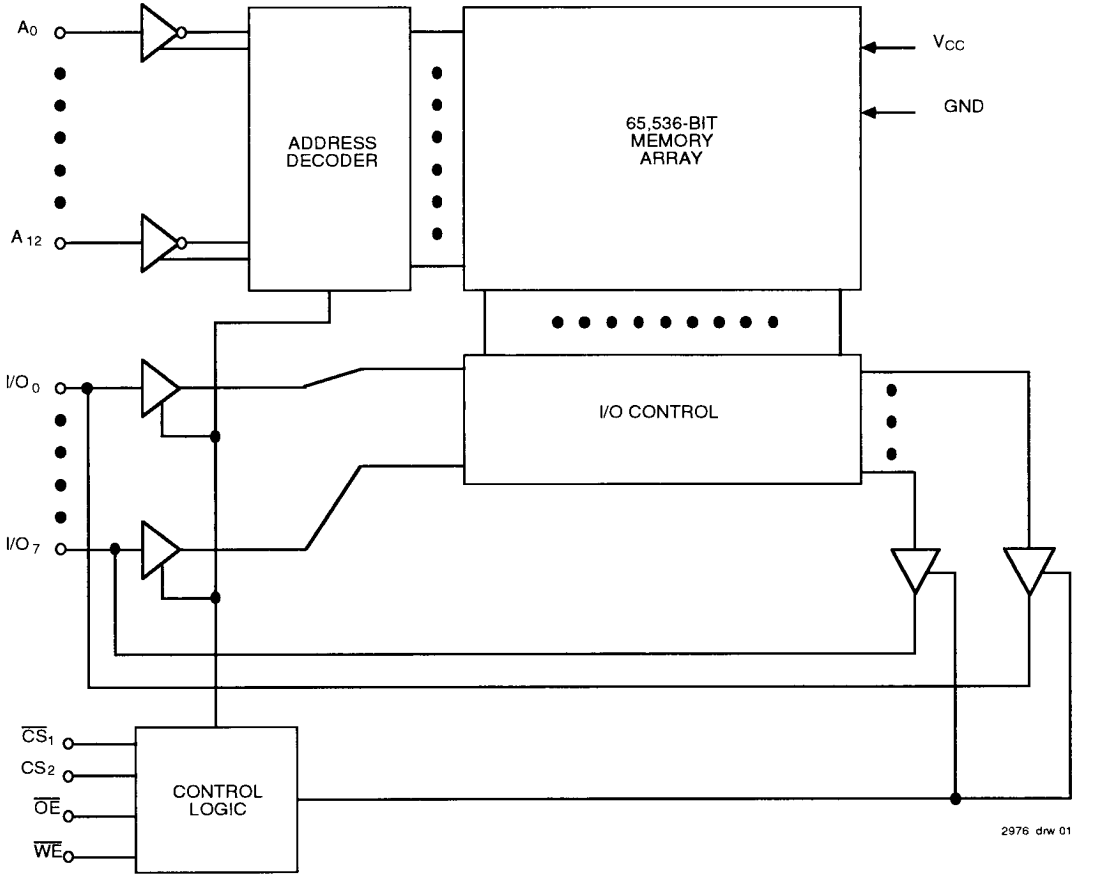
DESCRIPTION:

The IDT71B64 is a 65,536-bit high-speed static RAM organized as 8K x 8. It is fabricated using IDT's high-performance, high-reliability BiCMOS technology.

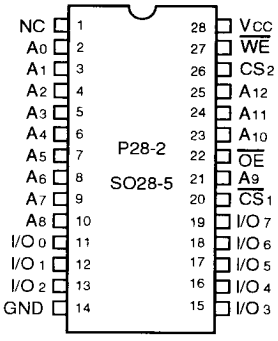
The IDT71B64 offers address access times as fast as 8ns. All inputs and outputs of the IDT71B64 are TTL-compatible. The device has 2 chip selects for simplified address decoding.

The IDT71B64 is packaged in JEDEC standard 300-mil 28-pin plastic DIP and SOJ packages.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS



DIP/SOJ
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Unit
VTERM(2)	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	–55 to +125	°C
TSTG	Storage Temperature	–55 to +125	°C
IOUT	DC Output Current	50	mA

NOTE: 2976 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VTERM must not exceed VCC + 0.5V.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	8	pF
COUT	Output Capacitance	VOUT = 0V	8	pF

NOTE: 2976 tbl 03

1. This parameter is determined by device characterization, but is not production tested.

6

TRUTH TABLE(1,2)

INPUTS				I/O	FUNCTION
WE	CS1	CS2	OE		
X	H	X	X	High-Z	Deselected–Standby (ISB)
X	VHC(3)	X	X	High-Z	Deselected–Standby (ISB1)
X	X	L	X	High-Z	Deselected–Standby (ISB)
X	X	VLC(3)	X	High-Z	Deselected–Standby (ISB1)
H	L	H	H	High-Z	Outputs Disabled
H	L	H	L	DATAOUT	Read Data
L	L	H	X	DATAIN	Write Data

NOTES: 2976 tbl 01

1. H = VIH, L = VIL, X = Don't care.
2. VLC = 0.2V, VHC = VCC -0.2V.
3. Other inputs ≥VHC or ≤VLC.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	VCC
Commercial	0°C to +70°C	0V	5V ± 10%

2976 tbl 04

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	VCC+0.5	V
VIL	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE: 2976 tbl 04

1. VIL (min.) = –1.5V for pulse width less than 10ns, once per cycle.

DC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} – 0.2V)

Symbol	Parameter	71B64S8[3] Com'l.	71B64S10 Com'l.	71B64S12 Com'l.	Unit
ICC	Dynamic Operating Current, $\overline{CS}_1 \geq V_{IH}$ and $\overline{CS}_1 \leq V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	180	170	170	mA
ISB	Standby Power Supply Current (TTL Level) $\overline{CS}_1 \geq V_{IH}$ or $CS_2 \leq V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	50	50	50	mA
ISB1	Full Standby Power Supply Current (CMOS Level) $\overline{CS}_1 \geq V_{HC}$ or $CS_2 \leq V_{LC}$, Outputs Open, V_{CC} = Max., f = 0[2], $V_{IN} \leq V_{LC}$ or $V_{IN} \geq V_{HC}$	20	20	20	mA

NOTES:
1. All values are maximum guaranteed values.
2. $f_{MAX} = 1/t_{RC}$ (all address inputs are cycling at f_{MAX}); f = 0 means no address input lines are changing.
3. Preliminary only.

2896 tbl 06

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1, 2 and 3

2976 tbl 06

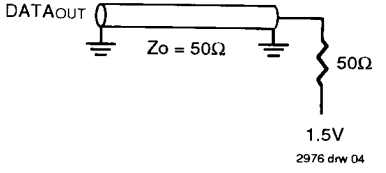
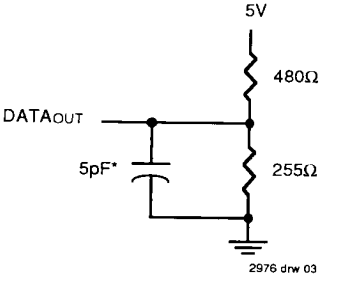


Figure 1. AC Test Load



*Includes jig and scope capacitance.

Figure 2. AC Test Load
(for t_{CLZ} 1,2, t_{OLZ}, t_{CHZ} 1, 2, t_{OHZ}, t_{WHZ}, t_{OW})

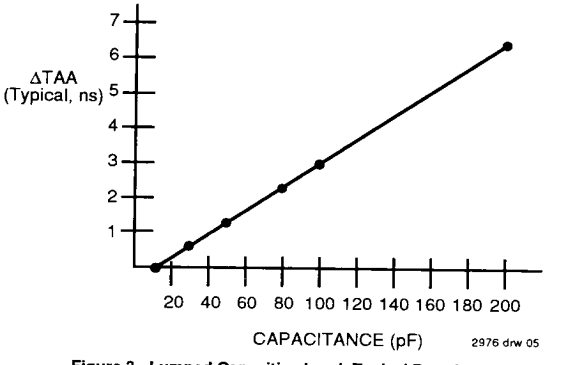


Figure 3. Lumped Capacitive Load, Typical Derating

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT71B64S		Unit
			Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS_1}$ = VIH, CS_2 = VIL, V_{OUT} = GND to V_{CC}	—	5	µA
V_{OL}	Output LOW Voltage	I_{OL} = 10mA, V_{CC} = Min.	—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.	—	0.4	
V_{OH}	Output HIGH Voltage	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	V

2976 tbl 07

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0V ± 10%, Commercial Temperature Ranges)

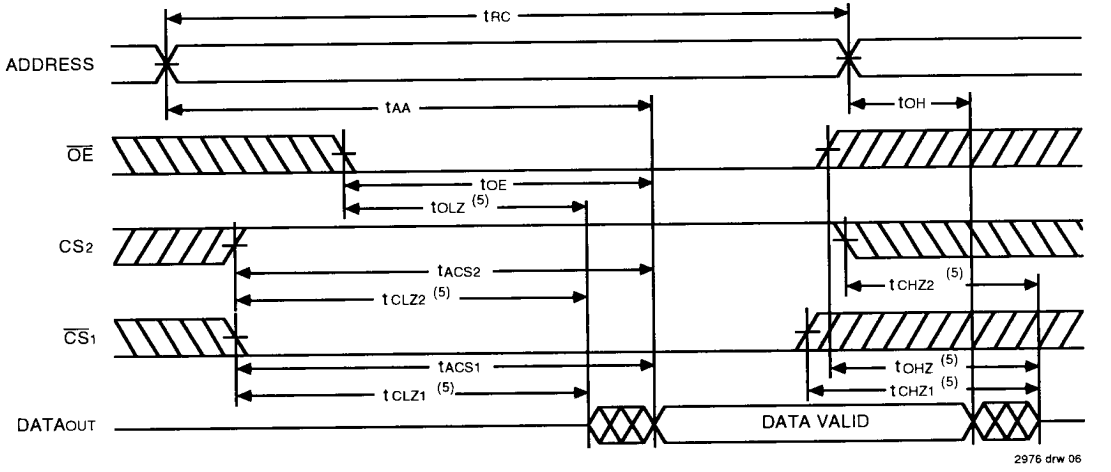
Symbol	Parameter	71B64S8[3]		71B64S10		71B64S12		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
tRC	Read Cycle Time	8	—	10	—	12	—	ns
tAA	Address Access Time	—	8	—	10	—	12	ns
tACS1,2	Chip Select-1, 2 Access Time[1]	—	8	—	10	—	12	ns
tCLZ1,2[2]	Chip Select-1, 2 to Output in Low-Z	2	—	2	—	2	—	ns
tOE	Output Enable to Output Valid	—	4	—	5	—	6	ns
tOLZ[2]	Output Enable to Output in Low-Z[2]	2	—	2	—	2	—	ns
tCHZ1,2[2]	Chip Deselect-1, 2 to Output in High-Z[2]	—	4	—	5	—	6	ns
tOHZ[2]	Output Disable to Output in High-Z[2]	—	4	—	4	—	5	ns
tOH	Output Hold from Address Change	2	—	2	—	3	—	ns
tPU[2]	Chip Select to Power-Up Time	0	—	0	—	0	—	ns
tPD[2]	Chip Deselect to Power-Up Time	—	8	—	10	—	12	ns
Write Cycle								
tWC	Write Cycle Time	8	—	10	—	12	—	ns
tAW	Address Valid to End-of-Write	7	—	8	—	10	—	ns
tCW1	Chip Select to End-of-Write ($\overline{CS1}$)	7	—	8	—	10	—	ns
tCW2	Chip Select to End-of-Write (CS2)	7	—	7	—	9	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	ns
tWP	Write Pulse Width	7	—	7	—	9	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	ns
tWHZ[2]	Write Enable to Output in High-Z[2]	—	4	—	5	—	6	ns
tDW	Data Valid to End-of-Write	5	—	5	—	6	—	ns
tDH	Data Hold from Write Time	0	—	0	—	0	—	ns
tOW[2]	Output Active from End-of-Write[2]	2	—	2	—	2	—	ns

2976 tbl 08

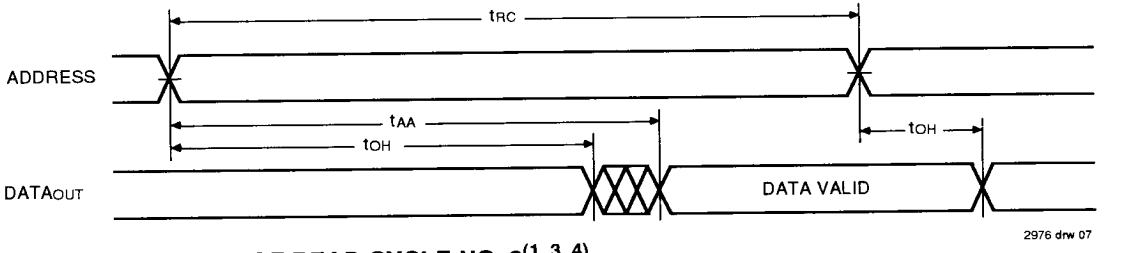
NOTES:
1. Both chip selects must be active for the device to be selected.
2. This parameter is guaranteed by device characterization, but is not production tested.
3. Preliminary only.

6

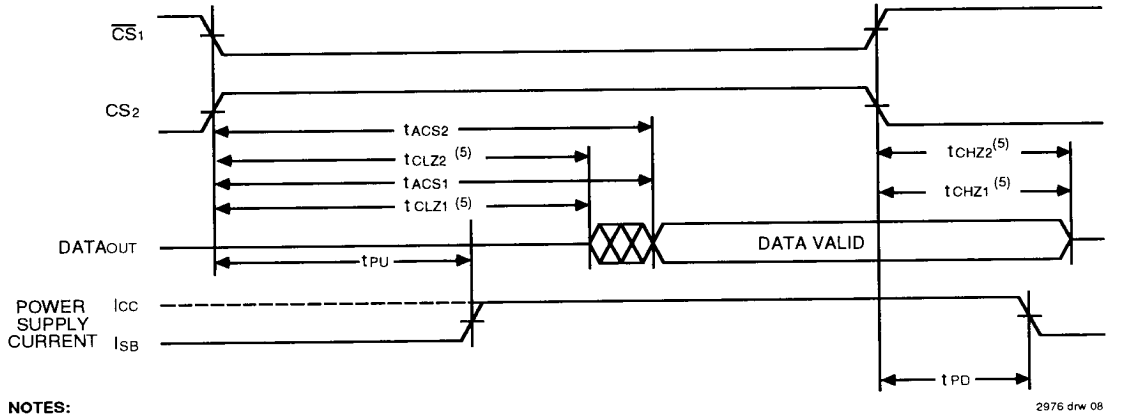
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)

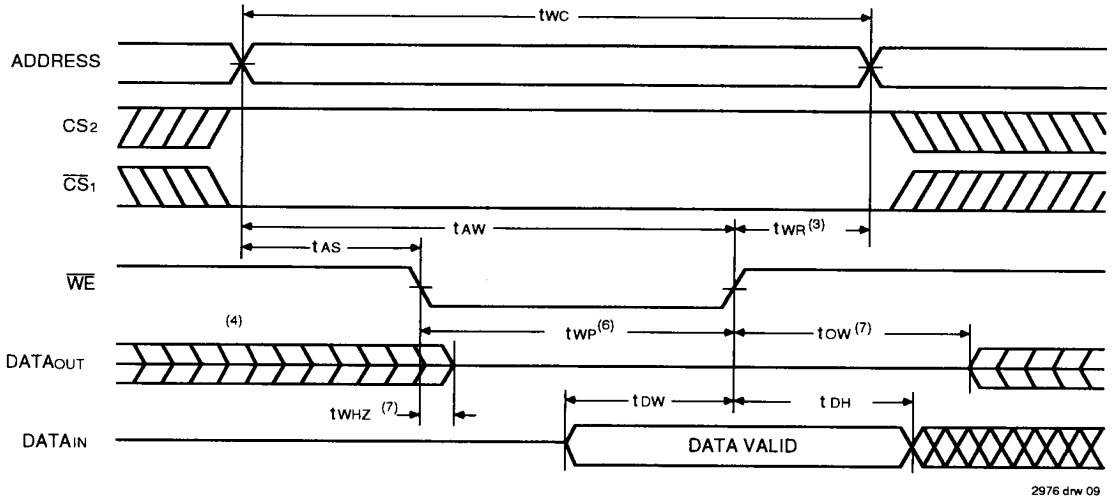


TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)

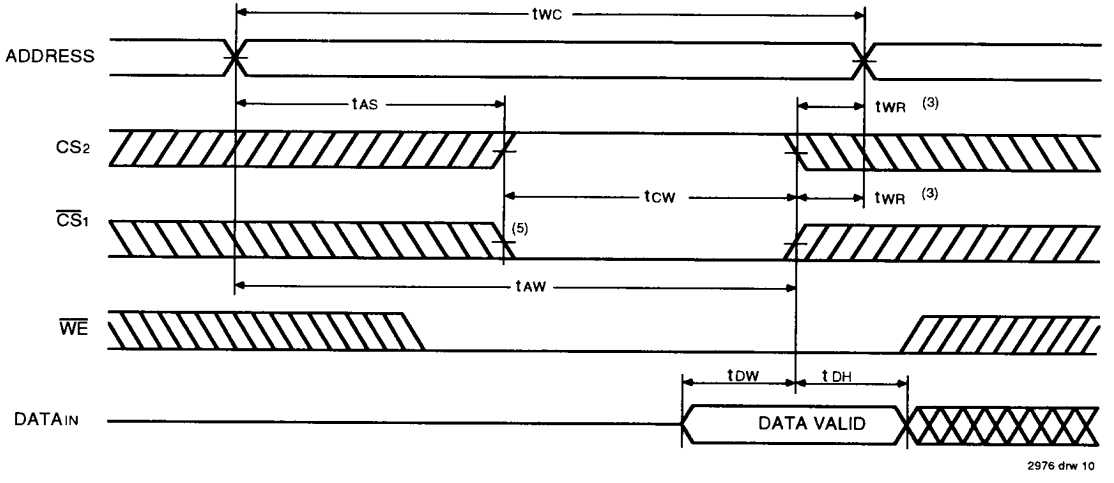


NOTES:
1. $\overline{WE}$ is HIGH for read cycle.
2. Device is continuously selected, $\overline{CS_1}$ = V_{IL}, CS_2 = V_{IH}.
3. Address valid prior to or coincident with $\overline{CS_1}$ transition LOW and CS_2 transition HIGH.
4. $\overline{OE}$ is LOW.
5. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 6)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2)



NOTES:
1. $\overline{WE}$, $\overline{CS_1}$ or CS_2 must be inactive during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{WE}$, a LOW $\overline{CS_1}$ and a HIGH CS_2.
3. $t_{WR1,2}$ is measured from the earlier of $\overline{CS_1}$ or $\overline{WE}$ going HIGH or CS_2 going LOW to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals must not be applied.
5. If the $\overline{CS_1}$ LOW transition or CS_2 HIGH transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
6. $\overline{OE}$ is continuously HIGH. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be greater than or equal to $t_{WHZ} + t_{DW}$ to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the minimum write pulse width is as short as the specified t_{WP}.
7. Transition is measured ±200mV from steady state.

ORDERING INFORMATION