



Integrated Device Technology, Inc.

BiCMOS STATIC RAM 64K (16K x 4-BIT)

IDT71B88

FEATURES:

- 16K x 4 BiCMOS static RAM
- High-speed address/chip select time
 - Commercial: 10/12ns
- Single chip select
- Single 5V ($\pm 10\%$) power supply
- Input and output directly TTL-compatible
- Available in 22-pin, 300 mil plastic DIP; and 24-pin, 300 mil plastic SOJ packages

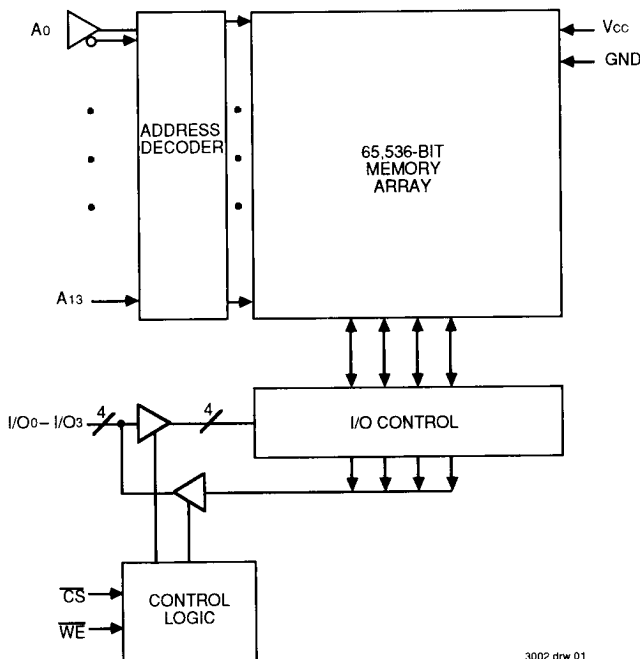
DESCRIPTION:

The IDT71B88 is a 65,536-bit high-speed static RAM organized as 16K x 4. It is fabricated using IDT's high-performance, high-reliability BiCMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs.

Address access times as fast as 8ns are available with power consumption of only 400mW (typ.). All inputs and outputs of the IDT71B88 are TTL-compatible, and operation is from a single 5V supply.

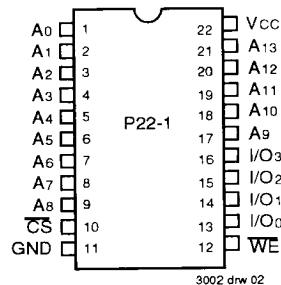
The IDT71B88 is packaged in a 22-pin, 300 mil plastic DIP and a 24-pin, 300 mil SOJ.

FUNCTIONAL BLOCK DIAGRAM



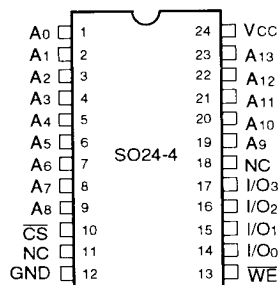
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PIN CONFIGURATIONS



3002 drw 02

DIP
TOP VIEW



3002 drw 02a

SOJ
TOP VIEW

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COMMERCIAL TEMPERATURE RANGES

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ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Com'l.	Mil.	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T _A	Operating Temperature	0 to +70	-55 to +125	°C
T _{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T _{STG}	Storage Temperature	-55 to +125	-65 to +125	°C
P _T	Power Dissipation	1.0	1.0	W
I _{OUT}	DC Output Current	50	50	mA

NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{IN} must not exceed V_{CC} + 0.5V.

TRUTH TABLE

CS	WE	I/O	Function
L	H	DATA _{OUT}	Read
L	L	DATA _{IN}	Write
H	X	High-Z	Deselect Chip

NOTE:

- H = V_{IH}, L = V_{IL}, X = Don't care.

CAPACITANCE (T_A = +25°C, f = 1.0MHz, SOJ package only)

Symbol	Parameter ⁽¹⁾	Conditions	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 3dV	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 3dV	7	pF

NOTE:

- This parameter is guaranteed by device characterization, but is not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V _{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V _{IH}	Input High Voltage	2.2	—	V _{CC} + 0.5	V
V _{IL}	Input Low Voltage	-0.5	—	0.8	V

NOTE:

- V_{IL} (Min.) = -1.5V for pulse width less than 10ns, once per cycle.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT71B88		Unit
			Min.	Max.	
I _{LI}	Input Leakage Current	V _{CC} = Max., V _{IN} = GND to V _{CC}	—	10	μA
I _{LO}	Output Leakage Current	V _{CC} = Max., \overline{CS} = V _{IH} , V _{OUT} = GND to V _{CC}	—	10	μA
V _{OL}	Output Low Voltage	I _{OL} = 10mA, V _{CC} = Min.	—	0.5	V
		I _{OL} = 8mA, V _{CC} = Min.	—	0.4	
V _{OH}	Output High Voltage	I _{OH} = -4mA, V _{CC} = Min.	2.4	—	V

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DC ELECTRICAL CHARACTERISTICS⁽¹⁾

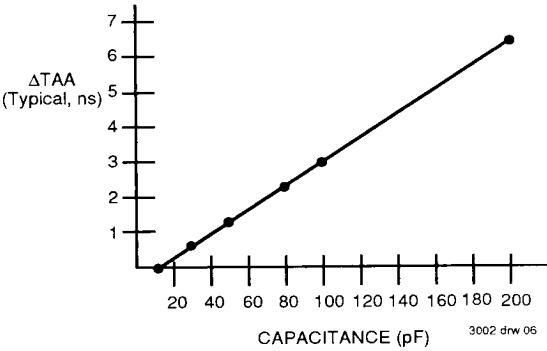
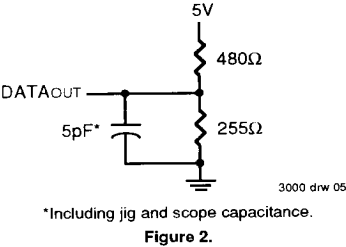
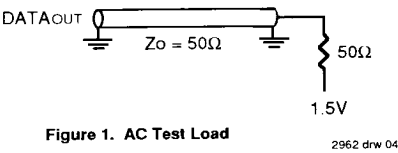
(V_{CC} = 5.0V ± 10%)

Symbol	Parameter	71B88S10	71B88S12	Unit
		Com'l.	Com'l.	
I _{CC}	Dynamic Operating Current, $\overline{CS} \leq V_{IL}$, Outputs Open, V _{CC} = Max., f = f _{MAX} ⁽²⁾	180	160	mA

NOTES:

- All values are maximum guaranteed values.
- f_{MAX} = 1/10RC, all Address inputs are cycling at f_{MAX}.

3002 tbl 05



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1, 2 & 3

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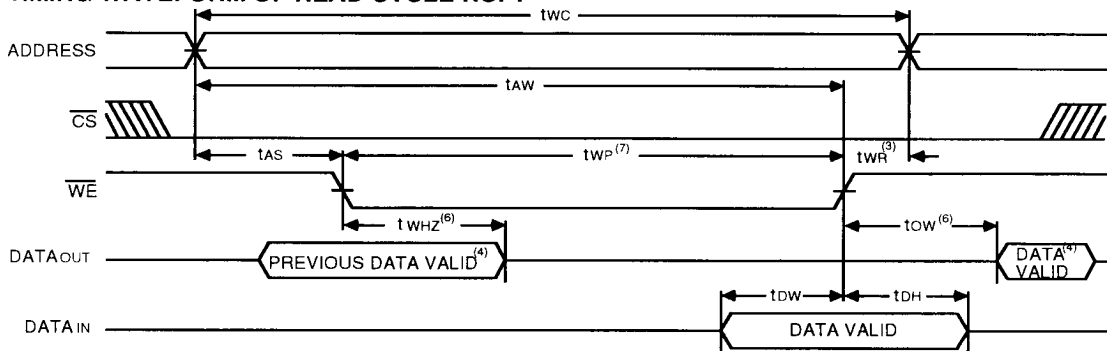
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71B88S10		71B88S12		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
tRC	Read Cycle Time	10	—	12	—	ns
tAA	Address Access Time	—	10	—	12	ns
tACS	\overline{CS} Access Time	—	6	—	7	ns
tCLZ ⁽¹⁾	\overline{CS} to Output in Low-Z	1	—	1	—	ns
tCHZ ⁽¹⁾	\overline{CS} to Output in High-Z	—	6	—	7	ns
tOH	Out Hold from Address Change	3	—	3	—	ns
Write Cycle						
tWC	Write Cycle Time	10	—	12	—	ns
tCW	Chip Select to End-of-Write	8	—	9	—	ns
tAW	Address Valid to End-of-Write	8	—	9	—	ns
tAS	Address Set-up Time	0	—	0	—	ns
tWP	Write Pulse Width	8	—	9	—	ns
tWR	Write Recovery Time	0	—	0	—	ns
tWHZ ⁽¹⁾	\overline{WE} to Output in High-Z	—	3	—	4	ns
tDW	Data Set-Up Time	5	—	6	—	ns
tDH	Data Hold from Write	0	—	0	—	ns
tOW ⁽¹⁾	Out Active from End-of- \overline{WE}	3	—	3	—	ns

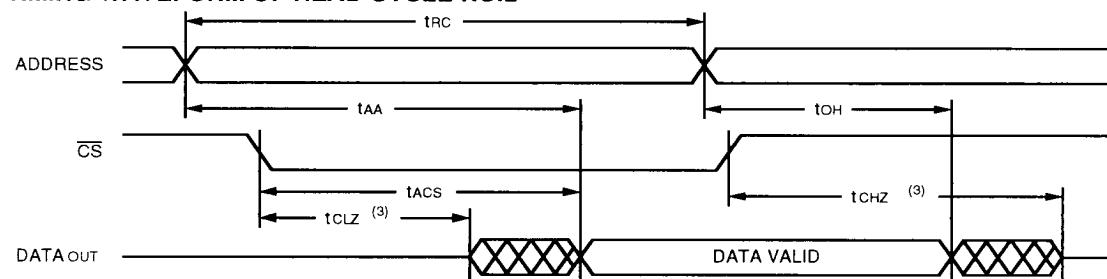
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NOTES:
1. This parameter is guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.

TIMING WAVEFORM OF READ CYCLE NO. 1 (1,2)



TIMING WAVEFORM OF READ CYCLE NO.2 (1,2,3)

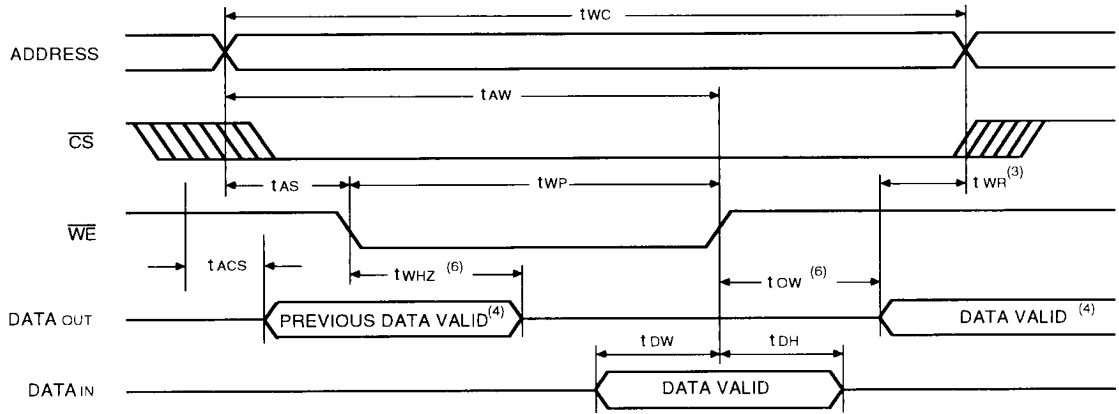


NOTES:

1. \overline{WE} is HIGH for read cycle, $\overline{WE} \geq V_{IH}$.
2. Address valid prior to or coincident with \overline{CS} transition LOW.
3. Transition is measured $\pm 200\text{mV}$ from steady state.

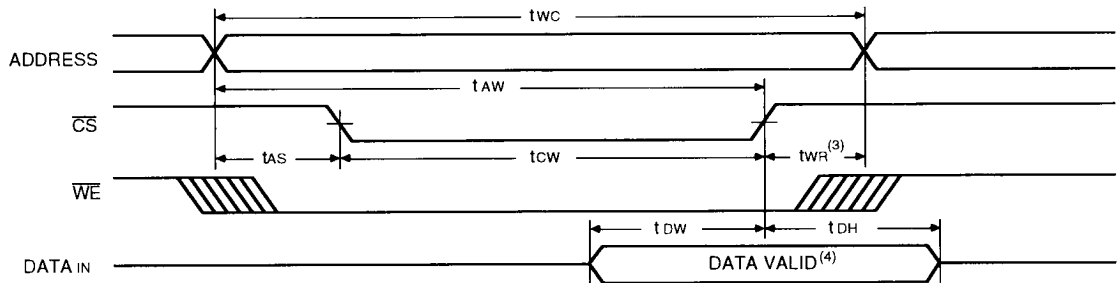
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TIMING WAVEFORM OF WRITE CYCLE NO.1 (\overline{WE} CONTROLLED TIMING)^(1,2,5)



3002 drw 09

TIMING WAVEFORM OF WRITE CYCLE NO.2 (\overline{CS} CONTROLLED TIMING)^(1,2,4)



3002 drw 10

NOTES:

1. \overline{WE} or \overline{CS} must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW \overline{CS} and a LOW \overline{WE} .
3. t_{WR} is measured from the earlier of \overline{CS} or \overline{WE} going HIGH to the end of the write cycle.
4. If \overline{CS} low transition occurs simultaneously with or after the \overline{WE} low transition, the outputs remain in the high-impedance state. If \overline{CS} high transition occurs simultaneously with or before \overline{WE} high transition, the outputs remain in the high-impedance state.
5. Transition is measured $\pm 200\text{mV}$ from steady state.

ORDERING INFORMATION

