Integrated Device Technology, Inc.

CMOS STATIC RAM 64K (8K x 8-BIT) RESETTABLE RAM

IDT7165S
IDT7165L
NOT RECOMMENDED FOR NEW DESIGNS (1)

FEATURES:

- High-speed asynchronous RAM clear on Pin 1 (clears all RAM bits to 0, reset cycle time = 2 x tAA)
- High-speed address access time
  - — Military: 35/45/55ns (max.)
  - — Commercial: 30/35/45ns (max.)
- High-speed chip select ($\overline{CS}_1$) time
  - — Military: 20/25/30 (max.)
  - — Commercial: 15/20/25ns (max.)
- Low-power operation
  - — IDT7165S
    Active: 300mW (typ.)
    Standby: 100µW (typ.)
  - — IDT7165L
    Active: 250mW (typ.)
    Standby: 30µW (typ.)
- Battery backup operation — 2V data retention voltage (IDT7165L only)
- Produced with CEMOS™ high-performance technology
- Single 5V(+10%) power supply
- Input and output directly TTL-compatible
- Standard 28-pin, 600 mil DIP, 300 mil DIP, 28-pin SOIC, 32-pin LCC and PLCC
- Military product is compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT7165 is a high-speed 65,536-bit static RAM, organized 8K x 8, with reset function. The $\overline{RESET}$ pin provides a single RAM clear control which clears all words in the internal RAM to zero when activated. This allows the memory bits for all locations to be cleared at power-on or system reset, or for a fast clear to be available to graphics, histogramming and other designs where a byte-by-byte RAM clear would cause noticeable system speed degradation.

This product is fabricated using IDT's high-performance, high-reliability CEMOS technology. Address access time of 20ns and chip select ($\overline{CS}_1$) time of 15ns are available with maximum power consumption of only 770mW. This circuit also offers a reduced power standby mode. When CS_2 goes low, the circuit will automatically go to and remain in a low-power standby mode. In the full standby mode, the low-power device typically consumes less than 30µW. The low-power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 10µW operating from a 2V battery.

The IDT7165 is packaged in a 28-pin 300 or 600 mil DIP, 28-pin gull-wing SOIC, and 32-pin LCC and PLCC, providing high board level densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to the military temperature applications which require instant destruction of sensitive RAM data and demand the highest level of performance and reliability.

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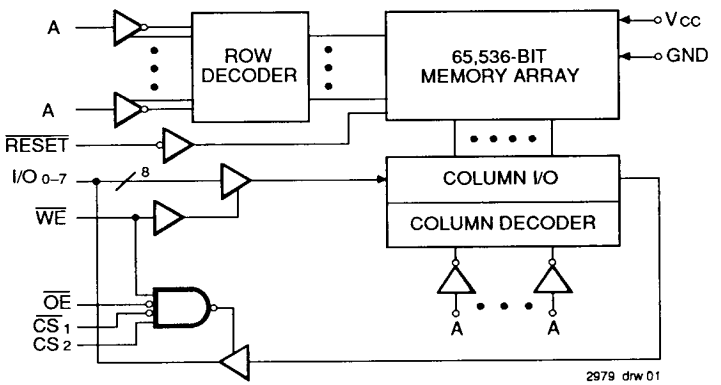
FUNCTIONAL BLOCK DIAGRAM



NOTE:
1. Not recommended for new designs. Contact marketing.

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DSC-1021/2
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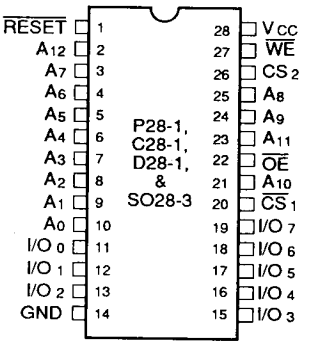
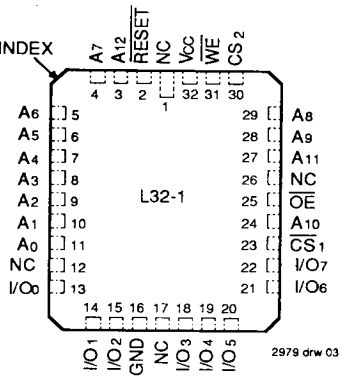
PIN CONFIGURATIONS



DIP/SOIC
TOP VIEW



LCC/PLCC
TOP VIEW

TRUTH TABLE (VCC = 0.2V, VHC = VCC - 0.2V)(1,2)

WE	CS1	CS2	OE	RESET	I/O	Function
X	X	X	X	L	—	Reset all bits to low
X	H	X	X	H	Z	Deselect chip
X	X	L	X	H	Z	Deselect power down(1)
X	VHC	X	X	H	Z	Deselect chip
X	X	VLC	X	VHC	Z	CMOS deselect power down(1)
H	L	H	H	H	Z	Output disable
H	L	H	L	H	DOUT	Read
L	L	H	X	H	DIN	Write

NOTE:
2979 tbl 01

1. CS2 will power down $\overline{CS_1}$, but $\overline{CS_1}$ will not power down CS2.
2. H = VIH, L = VIL, X = don't care.

PIN DESCRIPTIONS

A0–12	Address
I/O0-7	Data Input/Output
$\overline{CS_1}$, CS2	Chip Select
$\overline{RESET}$	Memory Reset
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
GND	Ground
VCC	Power

2979 tbl 02

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
PT	Power Dissipation	1.0	1.0	W
IOUT	DC Output Current	50	50	mA

NOTE:
2979 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	8	pF
COUT	Output Capacitance	VOUT = 0V	8	pF

NOTE:
2979 tbl 04

1. This parameter is determined by device characterization, but is not production tested.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

2979 tbl 05

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IHR}	$\overline{RESET}$ Input Voltage	2.5	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

2979 tbl 06

NOTE:
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS(1, 2)

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	7165S30		7165S/L35		7165S/L45		7165S/L55		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC1}	Operating Power Supply Current $\overline{CS_1}$ = V_{IL}, CS_2 = V_{IH} Outputs Open, V_{CC} = Max., f = 0	S	110	—	110	125	110	125	110	125	mA
		L	—	—	90	—	90	110	90	110	
I_{CC2}	Dynamic Operating Current $\overline{CS_1}$ = V_{IL}, CS_2 = V_{IH} Outputs Open, V_{CC} = Max., f = f_{MAX}	S	160	—	150	160	150	160	150	160	mA
		L	—	—	130	—	120	130	115	125	
I_{SB}	Standby Power Supply Current (TTL Level) f = f_{MAX} $\overline{CS_1}$ ≥ V_{IH}, CS_2 ≤ V_{IL}, $\overline{RESET}$ ≥ V_{IH} Outputs Open, V_{CC} = Max.	S	20	—	20	20	20	20	20	20	mA
		L	—	—	3	—	3	5	3	5	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) f = 0 CS_2 ≤ V_{LC} and $\overline{RESET}$ ≥ V_{HC} V_{CC} = Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC}	S	15	—	15	20	15	20	15	20	mA
		L	—	—	0.2	—	0.2	1.0	0.2	1.0	

2979 tbl 07

NOTES:
1. All values are maximum guaranteed values.
2. At f = f_{MAX} address and data are cycling at maximum frequency of read cycles f = 1/t_{RC}. f = 0 means no inputs change.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition		IDT7165S		IDT7165L		Unit
				Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	—	10	—	5	µA
			COM'L.	—	5	—	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	—	10	—	5	µA
			COM'L.	—	5	—	2	
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.		—	0.5	—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		—	0.4	—	0.4	
V_{OH}	Output High Voltage	I_{OL} = -4mA, V_{CC} = Min.		2.4	—	2.4	—	V

2979 tbl 08

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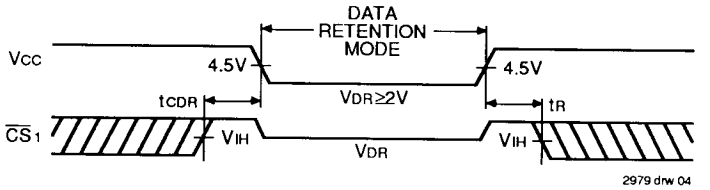
LOW Vcc DATA RETENTION WAVEFORM



DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Condition		Min.	Typ. (1) Vcc @ 2.0v	Typ. (1) Vcc @ 3.0V	Max. Vcc @ 2.0V	Max. Vcc @ 3.0V	Unit
V_{DR}	Vcc for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current		MIL.	—	10	15	200	300	µA
			COM'L.	—	10	15	60	90	
t_{CDR}(3)	Chip Deselect to Data Retention Time	$\overline{CS_2} \le V_{LC}$, $\overline{CS_1} \ge V_{HC}$ $\overline{RESET} \ge V_{HC}$		0	—	—	—	—	ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	—	—	—	—	ns
$\|I_{LI}\|$(3)	Input Leakage Current			—	—	—	2	2	µA

NOTES:
1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed, but not tested.

2979 tbl 08

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2979 tbl 09

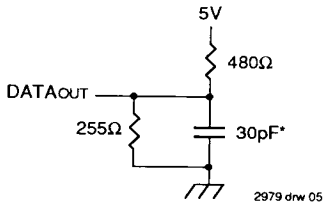


Figure 1. Output Load

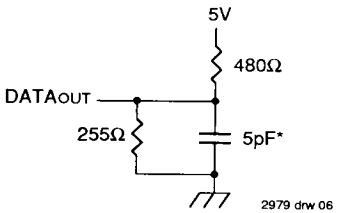


Figure 2. Output Load
(for $t_{CLZ1, 2}$, t_{OLZ}, $t_{CHZ1, 2}$, t_{OHZ}, t_{OW}, t_{WHZ})

*Includes scope and jig.

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	7165S30[1] Min.	7165S30[1] Max.	7165S35 7165L35[1] Min.	7165S35 7165L35[1] Max.	7165S45 7165L45 Min.	7165S45 7165L45 Max.	7165S55[3] 7165L55[3] Min.	7165S55[3] 7165L55[3] Max.	Unit
Read Cycle										
tRC	Read Cycle Time	30	—	35	—	45	—	55	—	ns
tAA	Address Access Time	—	30	—	35	—	45	—	55	ns
tACS1	Chip Select-1 Access Time[2]	—	15	—	20	—	25	—	30	ns
tACS2	Chip Select-2 Access Time[2]	—	35	—	40	—	45	—	55	ns
tCLZ1	Chip Select-1 to Output in Low Z[4]	0	—	0	—	0	—	0	—	ns
tCLZ2	Chip Select-2 to Output in Low Z[4]	5	—	5	—	5	—	5	—	ns
tOE	Output Enable to Output Valid	—	15	—	20	—	25	—	30	ns
tOLZ	Output Enable to Output in Low Z[4]	3	—	3	—	3	—	3	—	ns
tCHZ1	Chip Select-1 to Output in High Z[4]	—	13	—	15	—	20	—	25	ns
tCHZ2	Chip Select-2 to Output in High Z[4]	—	13	—	15	—	20	—	25	ns
tOHZ	Output Disable to Output in High Z[4]	—	14	—	15	—	20	—	25	ns
tOH	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
tPU	Chip Select to Power Up Time[4]	0	—	0	—	0	—	0	—	ns
tPD	Chip Select to Power Down Time[4]	—	30	—	35	—	45	—	55	ns
Write Cycle										
tWC	Write Cycle Time	30	—	35	—	45	—	55	—	ns
tCW1	Chip Select-1 to End of Write ($\overline{CS_1}$)	20	—	20	—	25	—	30	—	ns
tCW2	Chip Select-2 to End of Write (CS_2)	22	—	25	—	33	—	50	—	ns
tAW	Address Valid to End of Write	22	—	25	—	33	—	50	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	23	—	25	—	25	—	50	—	ns
tWR1	Write Recovery Time ($\overline{CS_1}$, $\overline{WE}$)	0	—	0	—	0	—	0	—	ns
tWR2	Write Recovery Time (CS_2)	5	—	5	—	5	—	5	—	ns
tWHZ	Write Enable to Output in High Z[4]	—	12	—	14	—	18	—	25	ns
tDW	Data to Write Time Overlap	13	—	15	—	20	—	25	—	ns
tDH1	Data Hold from Write Time ($\overline{CS_1}$)	3	—	3	—	3	—	3	—	ns
tDH2	Data Hold from Write Time (CS_2)	5	—	5	—	5	—	5	—	ns
tOW	Output Active from End of Write[4]	5	—	5	—	5	—	5	—	ns

NOTES:
1. 0° to +70°C temperature range only.
2. Both chip selects must be active for the device to be selected.
3. -55°C to +125°C temperature range only.
4. This parameter is guaranteed, but not tested.

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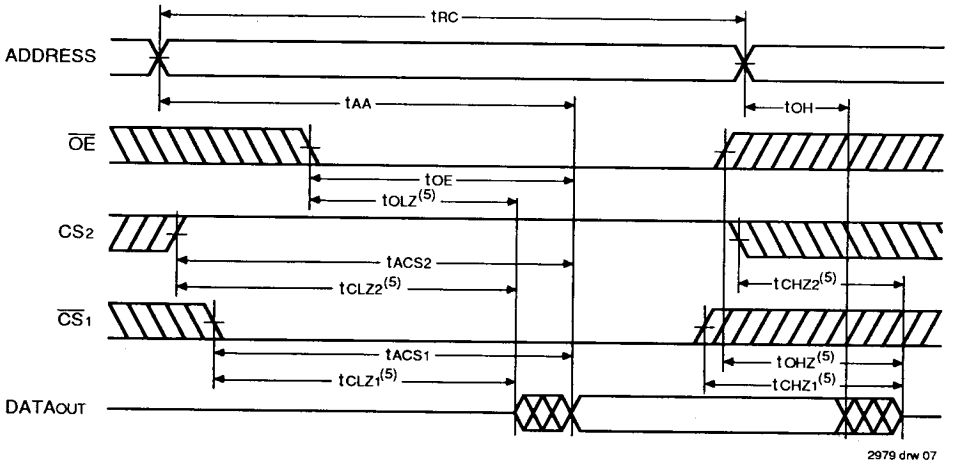
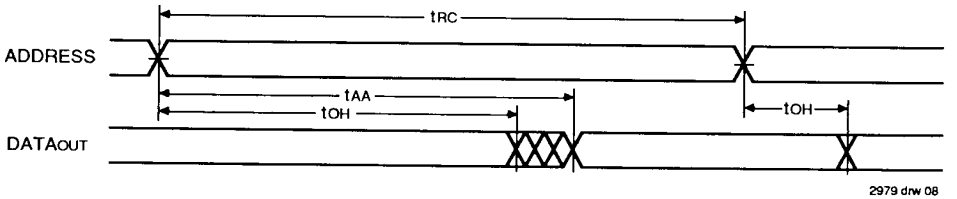
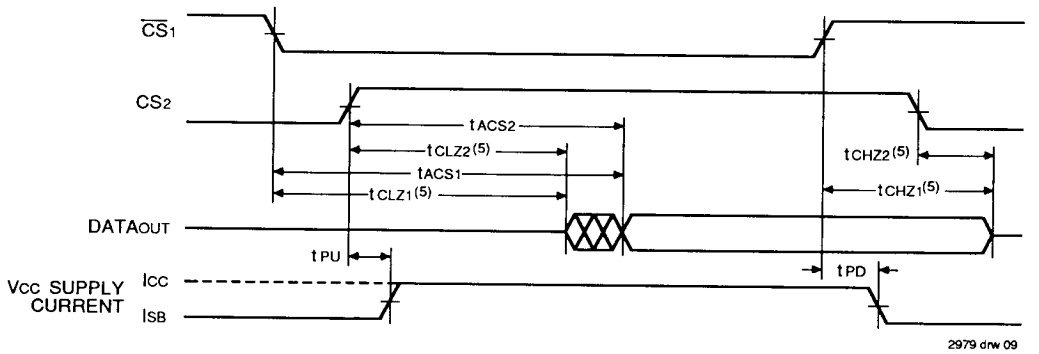
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)

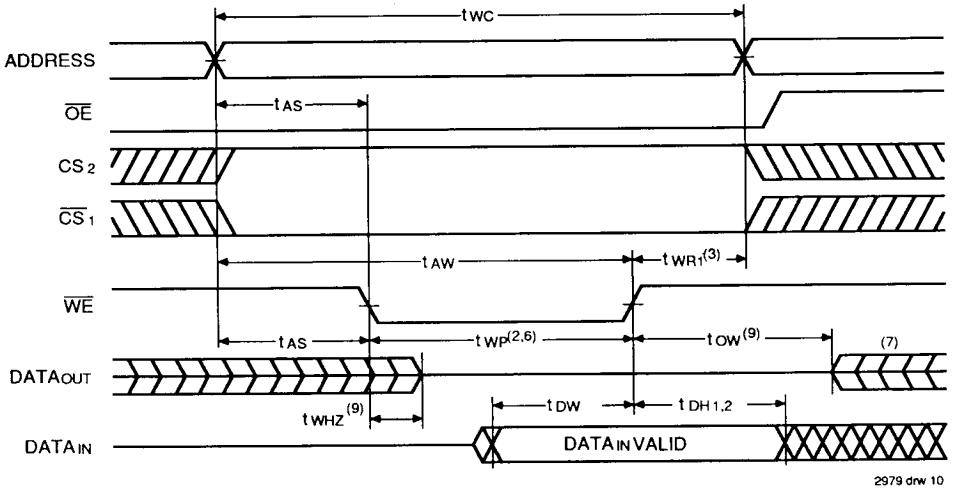


TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)

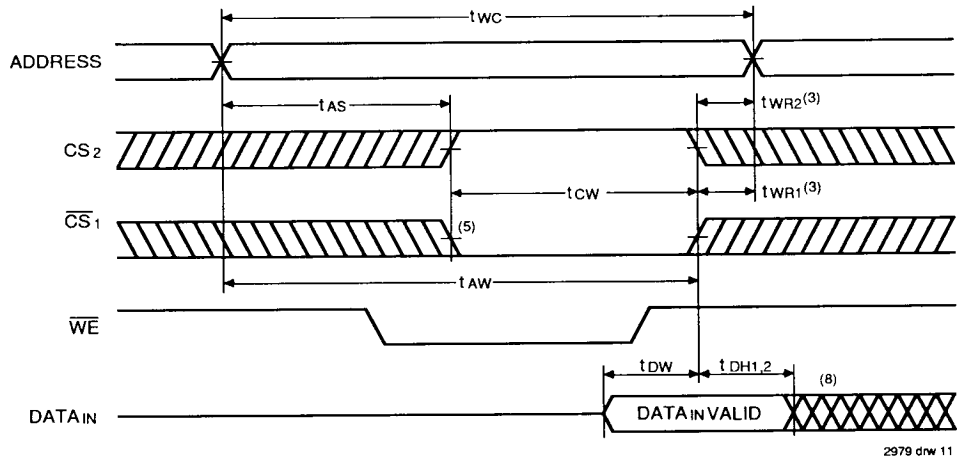


NOTES:
1. WE is high for read cycle.
2. Device is continuously selected, CS1 = VIL, CS2 = VIH.
3. Address valid prior to or coincident with CS1 transition low and CS2 transition high.
4. OE = VIL.
5. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1)



NOTES:
1. $\overline{WE}$, $\overline{CS_1}$ or CS_2 must be inactive during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{WE}$, a low $\overline{CS_1}$ and a high CS_2.
3. tWR1, 2 is measured from the earlier of $\overline{CS_1}$ or $\overline{WE}$ going high or CS_2 going low to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS_1}$ low transition or CS_2 high transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ +tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the spectified tWP.
7. DATAOUT is the same phase of write data of this write cycle.
8. If $\overline{CS_1}$ is low and CS_2 is high during this period, I/O pins are in the output state. Data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured ±200mV from steady state.

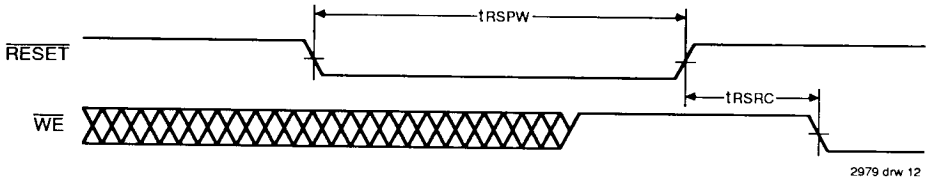
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	7165S30[1]		7165S35 7165L35[1]		7165S45 7165L45		7165S55[3] 7165L55[3]		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
tRSPW	Reset Pulse Width[2]	55	—	65	—	80	—	100	—	ns
tRSRC	Reset High to $\overline{WE}$ Low	5	—	5	—	10	—	10	—	ns

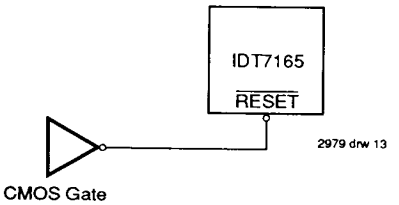
NOTES:
1. 0° to +70°C temperature range only.
2. Recommended duty cycle = 10% maximum.
3. -55°C to +125°C temperature range only.

2976 tbl 09

RESET TIMING

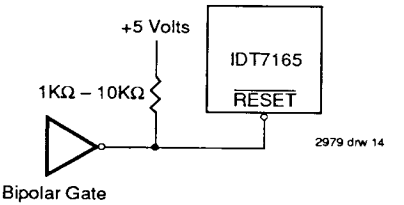


2979 drw 12



2979 drw 13

Driving the $\overline{RESET}$ pin with CMOS logic.

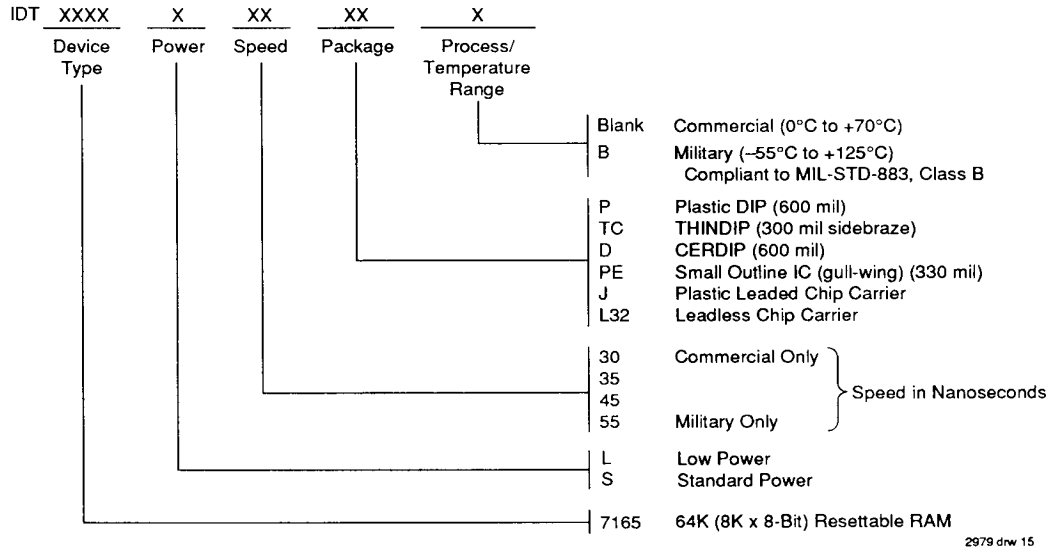


2979 drw 14

Driving the $\overline{RESET}$ pin with bipolar logic.

Figure 3.

ORDERING INFORMATION



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