Integrated Device Technology, Inc.

# 256 x 16, 512 x 16, 1024 x 16 PARALLEL-TO-SERIAL CMOS FIFO

**PRELIMINARY**
**IDT 72105**
**IDT 72115**
**IDT 72125**

T-46-35

## FEATURES:

- 25ns parallel port access time
- 50MHz serial output port shift rate
- Easily expandable in depth and width
- Asynchronous and simultaneous read write
- Dual-ported zero fall-through time architecture
- Five flags to signal FIFO status: Empty, Full, Half-full, Almost-empty and Almost-full
- Least Significant or Most Significant bit first read selectable
- Low power consumption
- Available in 28-pin 300mil Plastic and Sidebraze THINDIP and surface mount 28-pin SOIC
- Produced with advanced submicron CEMOS™ high-performance technology

## DESCRIPTION:

The IDT72105, IDT72115 and IDT72125 are high-speed, low power parallel-to-serial FIFOs. These FIFOs fit well in output peripherals as a data buffer. Some typical applications are in laser printers, FAX machines, local area networks (LANs), video storage, and disk or tape controllers.

The IDT72105/15/25 have a 16-bit parallel input port and a serial output port. Wider and Deeper parallel-to-serial data buffers can be built using multiple chips. IDT's unique serial expansion logic (RSIX, RSOX, $\overline{FL}$/DIR) makes both depth and width expansion possible using a minimum number of pins.

Serial output is driven by one data pin (SO) and one clock pin (SOCP). The Least Significant or Most Significant bit can be read first by programming the DIR pin after Reset.

Five flags, empty, full, half-full, almost-empty and almost-full are provided to monitor the FIFOs. The full and empty flags prevent any FIFO data overflow or underflow conditions. The half-full flag is available in both single and expansion configurations. The almost-empty and almost-full are only available in the single device configuration.

The IDT72105/15/25 are fabricated using IDT's high-speed submicron CEMOS™ technology.

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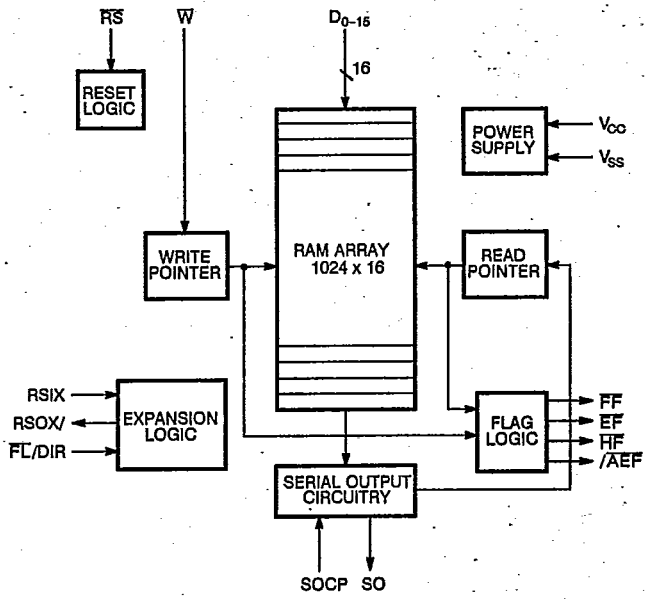
## FUNCTIONAL BLOCK DIAGRAM

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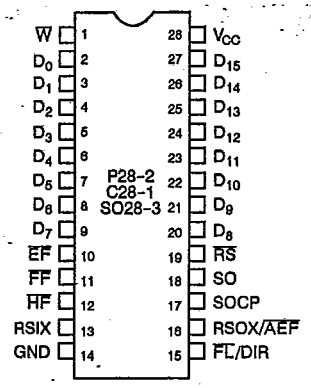
## PIN CONFIGURATIONS




DIP/SOIC
TOP VIEW

## PIN DESCRIPTIONS

| SYMBOL | NAME | I/O | DESCRIPTION |
|---|---|---|---|
| $D_0 - D_{15}$ | Inputs | I | Data inputs for 16-bit wide data. |
| $\overline{RS}$ | Reset | I | When $\overline{RS}$ is set low, internal READ and WRITE pointers are set to the first location of the RAM array. $\overline{FF}$ and $\overline{HF}$ go HIGH. $\overline{EF}$ and $\overline{AEF}$ go LOW. A reset is required before an initial WRITE after power-up. $\overline{W}$ must be high during the $\overline{RS}$ cycle. Also the First Load pin ($\overline{FL}$) is programmed only during Reset. |
| $\overline{W}$ | Write | I | A write cycle is initiated on the falling edge of WRITE if the Full Flag ($\overline{FF}$) is not set. Data set-up and hold times must be adhered to with respect to the rising edge of WRITE. Data is stored in the RAM array sequentially and independently of any ongoing read operation. |
| SOCP | Serial Output Clock | I | A serial bit read cycle is initiated on the rising edge of SOCP if the Empty Flag ($\overline{EF}$) is not set. In both Depth and Serial Word Width Expansion modes, all of the SOCP pins are tied together. |
| $\overline{FL}$/DIR | First Load/ Direction | I | This is a dual purpose input used in the width and depth expansion configurations. The First Load ($\overline{FL}$) function is programmed only during Reset ($\overline{RS}$) and a LOW on $\overline{FL}$ indicates the first device to be loaded with a byte of data. All other devices should be programmed HIGH. The Direction (DIR) function is programmed during operation after Reset and tells the device whether to read out the Least Significant or Most Significant bit first. |
| RSIX | Read Serial In Expansion | I | In the single device configuration, RSIX is set HIGH. In depth expansion or daisy chain expansion, RSIX is connected to RSOX (expansion out) of the previous device. |
| SO | Serial Output | O | Serial data is output on the Serial Output (SO) pin. Data is clocked out LSB or MSB depending on the Direction pin programming. During Expansion the SO pins are tied together. |
| $\overline{FF}$ | Full Flag | O | When $\overline{FF}$ goes low, the device is full and further WRITE operations are inhibited. When $\overline{FF}$ is high, the device is not full. |
| $\overline{EF}$ | Empty Flag | O | When $\overline{EF}$ goes low, the device is empty and further READ operations are inhibited. When $\overline{EF}$ is high, the device is not empty. |
| $\overline{HF}$ | Half Full Flag | O | When $\overline{HF}$ is LOW, the device is more than half full. When $\overline{HF}$ is HIGH, the device is empty to half full. |
| RSOX/$\overline{AEF}$ | Read Serial Out Expansion, Almost Empty, Almost Full Flag | O | This is a dual purpose output. In the single device configuration (RSIX HIGH), this is an $\overline{AEF}$ output pin. When $\overline{AEF}$ is LOW, the device is empty to 1/8 full - 1 or 7/8 full + 1 to full. When $\overline{AEF}$ is HIGH, the device is1/8 full up to 7/8 full. In the Expansion configuration (RSOX connected to RSIX of the next device) a pulse is sent from RSOX to RSIX to coordinate the width, depth or daisy chain expansion. |
| $V_{CC}$ | Power Supply | | Single power supply of 5V. |
| GND | Ground | | Single ground of 0V. |

## STATUS FLAGS

| NUMBER OF WORDS IN FIFO | | | FF | AEF | HF | EF |
|---|---|---|---|---|---|---|
| IDT72105 | IDT72115 | IDT72125 | | | | |
| 0 | 0 | 0 | H | L | H | L |
| 1-31 | 1-63 | 1-127 | H | L | H | H |
| 32-128 | 64-256 | 128-512 | H | H | H | H |
| 129-224 | 257-448 | 513-896 | H | H | L | H |
| 225-255 | 449-511 | 897-1023 | H | L | L | H |
| 256 | 512 | 1024 | L | L | L | H |

## ABSOLUTE MAXIMUM RATINGS (1)

| SYMBOL | RATING | COMMERCIAL | UNIT |
|---|---|---|---|
| $V_{TERM}$ | Terminal Voltage with Respect to GND | -0.5 to +7.0 | V |
| $T_A$ | Operating Temperature | 0 to +70 | °C |
| $T_{BIAS}$ | Temperature Under Bias | -55 to +125 | °C |
| $T_{STG}$ | Storage Temperature | -55 to +125 | °C |
| $I_{OUT}$ | DC Output Current | 50 | mA |

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## RECOMMENDED DC OPERATING CONDITIONS

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Commercial Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| GND | Supply Voltage | 0 | 0 | 0 | V |
| $V_{IH}$ | Input High Voltage | 2.0 | – | – | V |
| $V_{IL}$ (1) | Input Low Voltage | – | – | 0.8 | V |

NOTE:
1. 1.5V undershoots are allowed for 10ns once per cycle.

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## DC ELECTRICAL CHARACTERISTICS

(Commercial: $V_{CC}$ = 5V ±10%, $T_A$ = 0°C to +70°C)

| SYMBOL | PARAMETER | IDT72105 IDT72115 IDT72125 COMMERCIAL MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| $I_{IL}$ (1) | Input Leakage Current (Any Input) | -1 | – | 1 | µA |
| $I_{OL}$ (2) | Output Leakage Current | -10 | – | 10 | µA |
| $V_{OH}$ | Output Logic "1" Voltage $I_{OUT}$ = -2mA (5) | 2.4 | – | – | V |
| $V_{OL}$ | Output Logic "0" Voltage $I_{OUT}$ = 8mA (6) | – | – | 0.4 | V |
| $I_{CC1}$ (3) | Power Supply Current | – | 90 | 140 | mA |
| $I_{CC2}$ (3) | Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}$/DIR = $V_{IH}$) | – | 8 | 12 | mA |
| $I_{CC3}$ (L) (3, 4) | Power Down Current | – | – | 8 | mA |

NOTES:
1. Measurements with $0.4 \le V_{IN} \le V_{OUT}$.
2. $\overline{RS} \le V_{IL}$, $0.4 \le V_{OUT} \le V_{CC}$
3. $I_{CC}$ measurements are made with outputs open.
4. $\overline{RS}$ = $\overline{FL}$/DIR = $\overline{W}$ = $\overline{R}$ = $V_{CC}$ -0.2V; all other inputs ≥ $V_{CC}$ -0.2V or ≤ 0.2V
5. For SO, $I_{OUT}$ = -4mA
6. For SO, $I_{OUT}$ = 16mA

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## AC ELECTRICAL CHARACTERISTICS

(Commercial: $V_{CC}$ = 5V ±10%, $T_A$ = 0°C to +70°C)

| SYMBOL | PARAMETER | FIGURE | 72105x25 72115x25 72125x25 | | 72105x50 72115x50 72125x50 | | 72105x80 72115x80 72125x80 | | 72105x120 72115x120 72125x120 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| $t_S$ | Parallel Shift Frequency | – | – | 22.2 | – | 15 | – | 10 | – | 7 | MHz |
| $t_{SOCP}$ | Serial Shift Frequency | – | – | 50 | – | 40 | – | 28 | – | 25 | MHz |
| | | | | | | | | | | | |
| $t_{WC}$ | Write Cycle Time | 1 | 35 | – | 65 | – | 100 | – | 140 | – | ns |
| $t_{WPW}$ | Write Pulse Width | 1 | 25 | – | 50 | – | 80 | – | 120 | – | ns |
| $t_{WR}$ | Write Recovery Time | 1 | 10 | – | 15 | – | 20 | – | 20 | – | ns |
| $t_{DS}$ | Data Set-up Time | 1 | 10 | – | 15 | – | 15 | – | 20 | – | ns |
| $t_{DH}$ | Data Hold Time | 1 | 0 | – | 5 | – | 5 | – | 10 | – | ns |
| | | | | | | | | | | | |
| $t_{SOCP}$ | Serial Clock Cycle Time | 2 | 20 | – | 25 | – | 35 | – | 40 | – | ns |
| $t_{SOCW}$ | Serial Clock Width High/Low | 2 | 8 | – | 10 | – | 15 | – | 18 | – | ns |
| $t_{SOPD}$ | SOCP Rising Edge to SO Valid Data | 2 | – | 10 | – | 12 | – | 17 | – | 20 | ns |
| $t_{SOHZ}$ | SOCP Rising Edge to SO at High Z[1] | 2 | 3 | 10 | 3 | 12 | 3 | 17 | 3 | 20 | ns |
| $t_{SOLZ}$ | SOCP Rising Edge to SO at Low Z[1] | 2 | 3 | 10 | 3 | 12 | 3 | 17 | 3 | 20 | ns |
| | | | | | | | | | | | |
| $t_{WEF}$ | Write High to $\overline{EF}$ High | 4,5 | – | 20 | – | 25 | – | 35 | – | 40 | ns |
| $t_{WFF}$ | Write Low to $\overline{FF}$ Low | 3,6 | – | 30 | – | 40 | – | 50 | – | 60 | ns |
| $t_{WF}$ | Write Low to Transitioning $\overline{HF}$, $\overline{AEF}$ | 7 | – | 30 | – | 40 | – | 50 | – | 60 | ns |
| $t_{WPF}$ | Write Pulse Width After $\overline{FF}$ High | 6 | 25 | – | 50 | – | 80 | – | 120 | – | ns |
| $t_{SOCEF}$ | SOCP Rising Edge to $\overline{EF}$ Low | 4,5 | – | 20 | – | 25 | – | 35 | – | 40 | ns |
| $t_{SOCFF}$ | SOCP Rising Edge to $\overline{FF}$ High | 3,6 | – | 30 | – | 40 | – | 50 | – | 60 | ns |
| $t_{SOCF}$ | SOCP Rising Edge to Transitioning $\overline{HF}$, $\overline{AEF}$ | 7 | – | 30 | – | 40 | – | 50 | – | 60 | ns |
| $t_{REFSO}$ | SOCP Delay After $\overline{EF}$ High | 5 | 35 | – | 65 | – | 100 | – | 140 | – | ns |
| | | | | | | | | | | | |
| $t_{RSC}$ | Reset Cycle Time | 8 | 35 | – | 65 | – | 100 | – | 140 | – | ns |
| $t_{RS}$ | Reset Pulse Width | 8 | 25 | – | 50 | – | 80 | – | 120 | – | ns |
| $t_{RSS}$ | Reset Set-up Time | 8 | 25 | – | 50 | – | 80 | – | 120 | – | ns |
| $t_{RSR}$ | Reset Recovery Time | 8 | 10 | – | 15 | – | 20 | – | 20 | – | ns |
| | | | | | | | | | | | |
| $t_{FLS}$ | $\overline{FL}$ Set-up Time to $\overline{RS}$ Rising Edge | 9 | 5 | – | 7 | – | 10 | – | 10 | – | ns |
| $t_{FLH}$ | $\overline{FL}$ Hold Time to $\overline{RS}$ Rising Edge | 9 | 0 | – | 0 | – | 5 | – | 5 | – | ns |
| $t_{DIRS}$ | DIR Set-up Time to SOCP Rising Edge | 9 | 5 | – | 7 | – | 10 | – | 10 | – | ns |
| $t_{DIRH}$ | DIR Hold Time from SOCP Rising Edge | 9 | 0 | – | 0 | – | 5 | – | 5 | – | ns |
| $t_{SOXD1}$ | SOCP Rising Edge to RSOX Rising Edge | 9 | 3 | 11 | 3 | 15 | 3 | 20 | 3 | 20 | ns |
| $t_{SOXD2}$ | SOCP Rising Edge to RSOX Falling Edge | 9 | 3 | 11 | 3 | 15 | 3 | 20 | 3 | 20 | ns |
| $t_{SIXS}$ | RSIX Set-up Time to SOCP Rising Edge | 9 | 5 | – | 7 | – | 10 | – | 10 | – | ns |
| $t_{SIXH}$ | RSIX Hold Time from SOCP Rising Edge | 9 | 0 | – | 0 | – | 5 | – | 5 | – | ns |

NOTE:
1. Guaranteed by design minimum times, not tested.

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## AC TEST CONDITIONS

| | |
|---|---|
| Input Pulse Levels | GND to 3.0V |
| Input Rise/Fall Times | 5ns |
| Input Timing Reference Levels | 1.5V |
| Output Reference Levels | 1.5V |
| Output Load | See Figure 1 |

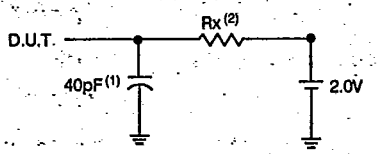


Figure A. Output Load.

1. Includes jig and scope capacitances.
2. For SO, Rx = 100Ω. For all other outputs, Rx = 200Ω.

## CAPACITANCE ($T_A$ = +25°C, f = 1.0MHz)

| SYMBOL | PARAMETER(1) | CONDITIONS | MAX. | UNIT |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | 10 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0V | 12 | pF |

NOTE:
1. This parameter is sampled and not 100% tested.

## FUNCTIONAL DESCRIPTION

### Parallel Data Input

The device must be reset before beginning operation so that all flags are set to location zero. In width or depth expansion the First Load pin ($\overline{FL}$) must be programmed to indicate the first device.

The data is written into the FIFO in parallel through the $D_{0-15}$ input data lines. A write cycle is initiated on the falling edge of the Write ($\overline{W}$) signal provided the Full Flag ($\overline{FF}$) is not asserted. If the $\overline{W}$ signal changes from HIGH-to-LOW and the Full Flag ($\overline{FF}$) is already set, the write line is inhibited internally from incrementing the write pointer and no write operation occurs.

Data set-up and hold times must be met with respect to the rising edge of Write. The data is written to the RAM at the write pointer. On the rising edge of $\overline{W}$, the write pointer is incremented. Write operations can occur simultaneously or asynchronously with read operations.

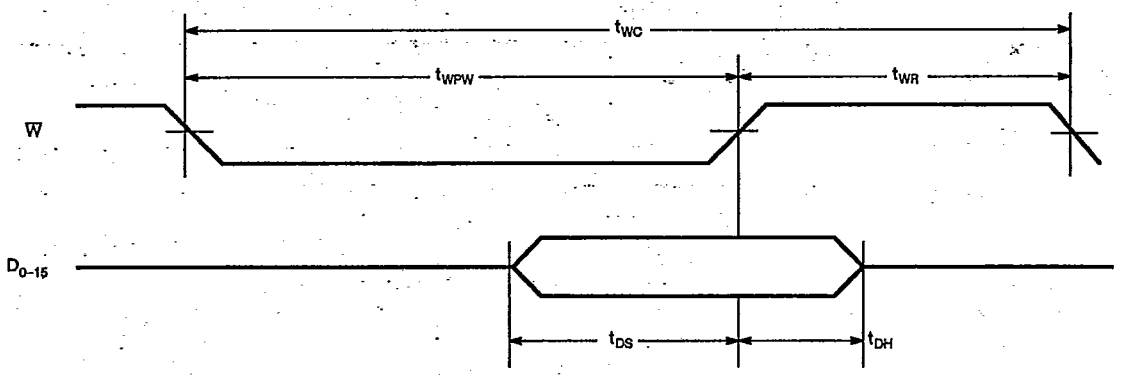


Figure 1. Write Operation

### Serial Data Output

The serial data is output on the SO pin. The data is clocked out on the rising edge of SOCP providing the Empty Flag ($\overline{EF}$) is not asserted. If the Empty Flag is asserted then the next data word is inhibited from moving to the output register and being clocked out by SOCP.

The serial word is shifted out Least Significant Bit or Most Significant Bit first depending on the $\overline{FL}$/DIR level during operation. A LOW on DIR will cause the Least Significant Bit to be read out first. A HIGH on DIR will cause the Most Significant Bit to be read out first.

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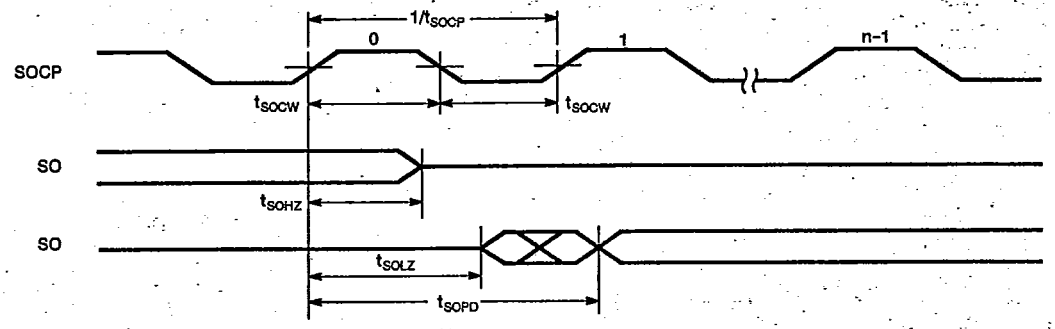


Figure 2. Read Operation

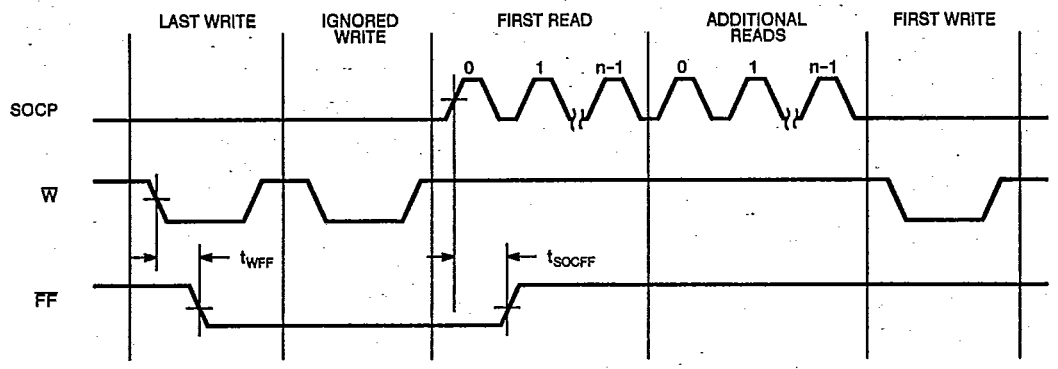


Figure 3. Full Flag from Last Write to First Read

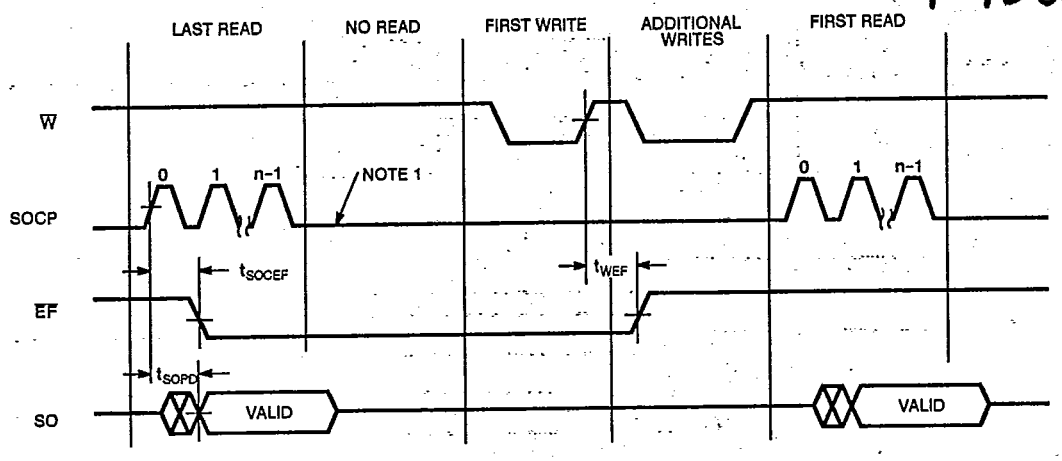


Figure 4. Empty Flag from Last Read to First Write

NOTE:
1. SOCP should not be clocked until $\overline{EF}$ goes high.

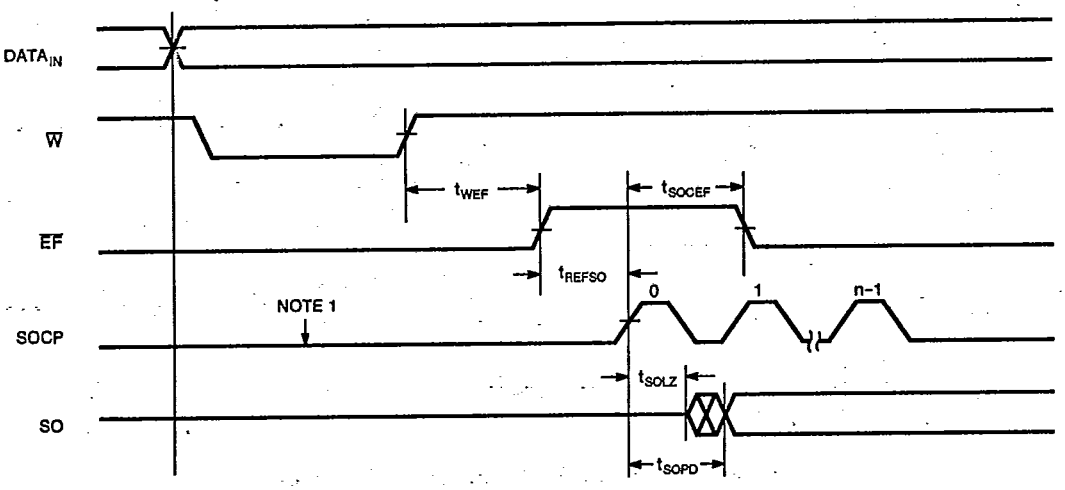


Figure 5. Empty Boundry Condition Timing

NOTE:
1. SOCP should not be clocked until $\overline{EF}$ goes high.

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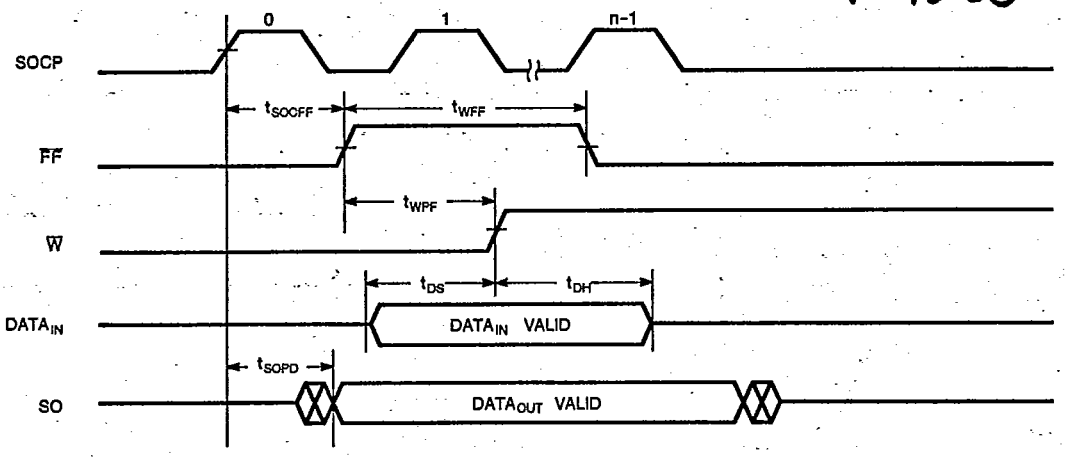


Figure 6. Full Boundary Condition Timing

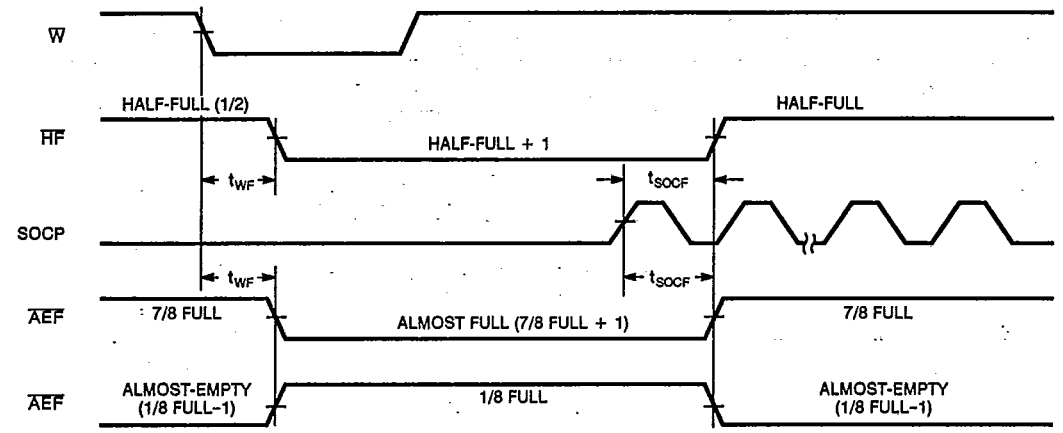


Figure 7. Half Full, Almost Full and Almost Empty Timings

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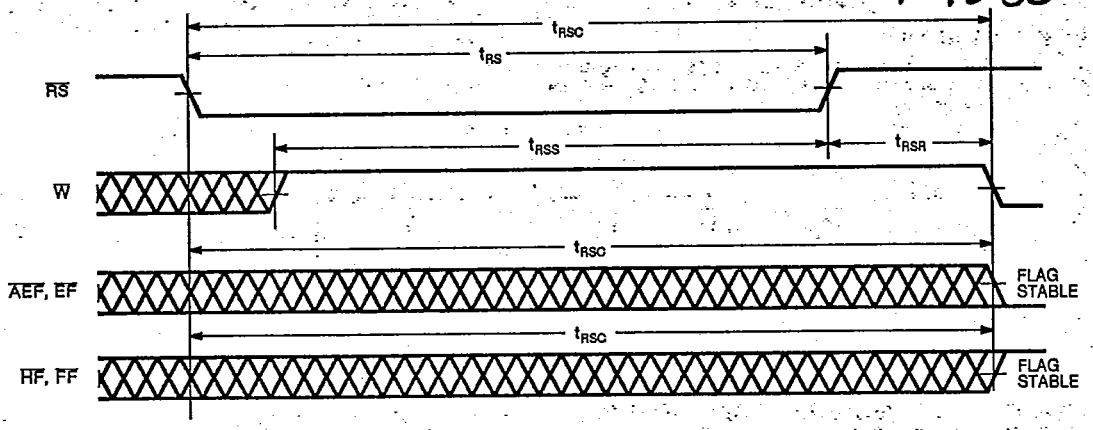


Figure 8. Reset

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NOTE:
1. $\overline{EF}$, $\overline{FF}$, $\overline{HF}$ and $\overline{AEF}$ may change status during Reset, but flags will be valid at $t_{RSC}$.

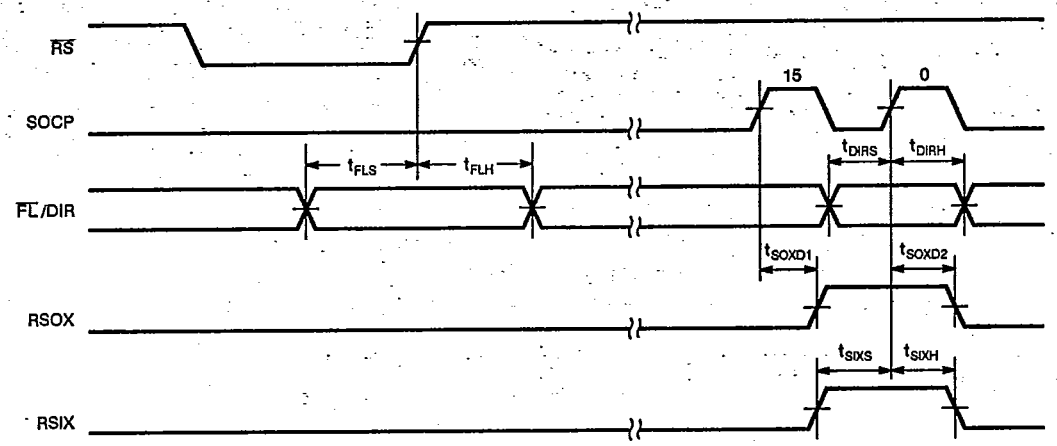


Figure 9. Serial Read Expansion

## OPERATING CONFIGURATIONS

### Single Device Mode

The device must be reset before beginning operation so that all flags are set to location zero. In the standalone case, the RSIX line is tied HIGH and indicates single device operation to the device. The RSOX/$\overline{AEF}$ pin defaults to $\overline{AEF}$, and outputs the Almost Empty and Almost Full Flag.

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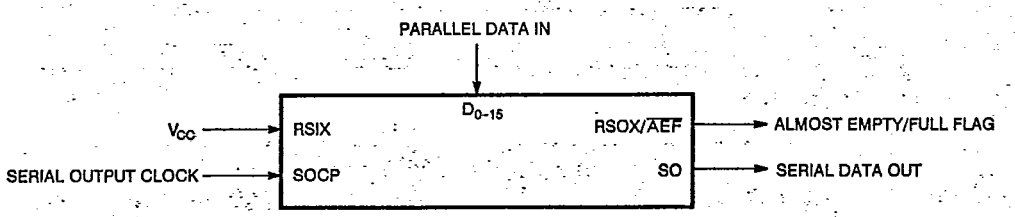


**Figure 10. Single Device Configuration**

### TABLE 1: RESET AND FIRST LOAD TRUE TABLE—SINGLE DEVICE CONFIGURATION

| MODE | INPUTS | | | INTERNAL STATUS | | OUTPUTS | | |
|---|---|---|---|---|---|---|---|---|
| | $\overline{RS}$ | $\overline{FL}$ | DIR | READ POINTER | WRITE POINTER | $\overline{AEF}$, $\overline{EF}$ | $\overline{FF}$ | $\overline{HF}$ |
| Reset | 0 | X | X | Location Zero | Location Zero | 0 | 1 | 1 |
| Read/Write | 1 | X | 0, 1 | Increment(1) | Increment(1) | X | X | X |

**NOTE:**
1. Pointer will increment if appropriate flag is HIGH.

### Width Expansion Mode

In the cascaded case, word widths of more than 16 bits can be achieved by using more than one device. By tying the RSOX and RSIX pins together as shown in Figure 11 and programming which is the Least Significant Device, a cascaded serial word is achieved. The Least Significant Device is programmed by a LOW on the $\overline{FL}$/DIR pin during reset. All other devices should be programmed HIGH on the $\overline{FL}$/DIR pin at reset.

The Serial Data Output (SO) of each device in the serial word must be tied together. Since the SO pin is three stated, only the device which is currently shifting out is enabled and driving the 1-bit bus. NOTE: After reset, the level on the $\overline{FL}$/DIR pin decides if the Least Significant or Most Significant Bit is read first out of each device.

The three flag outputs, Empty ($\overline{EF}$), Half Full ($\overline{HF}$) and Full ($\overline{FF}$), should be taken from the Most Significant Device (in the example, FIFO #2). The Almost Empty and Almost Full Flag is not available due to using the RSOX pin for expansion.

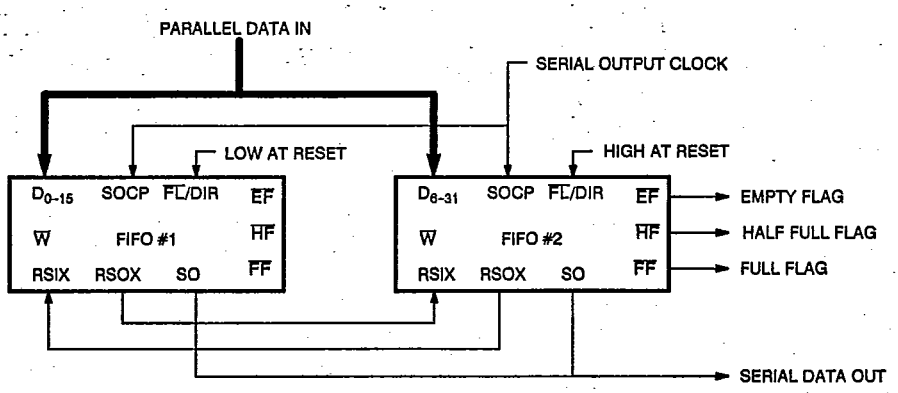


**Figure 11. Width Expansion for 32-bit Parallel Data In**

### Depth Expansion (Daisy Chain) Mode

The IDT 72105/15/25 can easily be adapted to applications where the requirements are for greater than 1024 words. Figure 12 demonstrates Depth Expansion using three IDT72105/15/25 and an IDT74FCT138 Address Decoder. Any depth can be attained by adding additional devices. The Address Decoder is necessary to determine which FIFO to write data into. A byte of data should be written sequentially into each FIFO so that the RSOX/RSIX handshake can control reading out the data in the correct sequence. The IDT72105/15/25 operate in the Depth Expansion Mode when the following conditions are met:

1. The first device must be designated by programming $\overline{FL}$ LOW at Reset, All other devices to be programmed HIGH.
2. The Read Serial Out Expansion (RSOX) of each device must be tied to the Read Serial In Expansion (RSIX of the next device in the manner shown).
3. External logic is needed to generate composite Empty, Half Full and Full Flags. This requires the OR-ing of all $\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ Flags.
4. The Almost Empty and Almost Full Flag is not available due to using the RSOX pin for expansion.

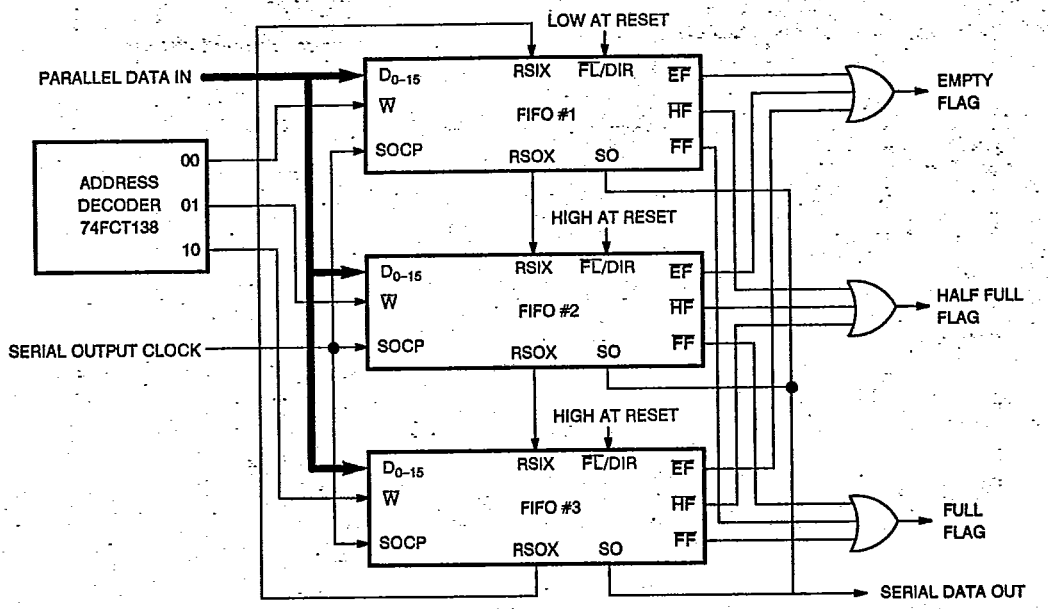


**Figure 12. A 3K x 16 Parallel-to-Serial FIFO using the IDT72125**

### TABLE 2: RESET AND FIRST LOAD TRUTH TABLE — WIDTH/DEPTH COMPOUND EXPANSION MODE

| MODE | INPUTS | | | INTERNAL STATUS | | OUTPUTS | |
|---|---|---|---|---|---|---|---|
| | $\overline{RS}$ | $\overline{FL}$ | DIR | READ POINTER | WRITE POINTER | $\overline{EF}$ | $\overline{HF}$, $\overline{FF}$ |
| Reset-First Device | 0 | 0 | X | Location Zero | Location Zero | 0 | 1 |
| Reset all Other Devices | 0 | 1 | X | Location Zero | Location Zero | 0 | 1 |
| Read/Write | 1 | X | 0, 1 | X | X | X | X |

NOTE:
1. $\overline{RS}$ = Reset Input, $\overline{FL}$/DIR = First Load/Direction, $\overline{EF}$ = Empty Flag Output, $\overline{HF}$ = Half Full Flag Output, $\overline{FF}$ = Full Flag Output

### Compound Expansion (Daisy Chain) Mode

The IDT72105/15/25 can be expanded in both depth and width as Figure 13 indicates:

1. The RSOX-to-RSIX expansion signals are wrapped around sequentially.
2. The write ($\overline{W}$) signal is expanded in width.
3. Flag signals are only taken from the Most Significant Devices.
4. The Least Significant device in the array must be programmed with a LOW on $\overline{FL}$/DIR during reset.

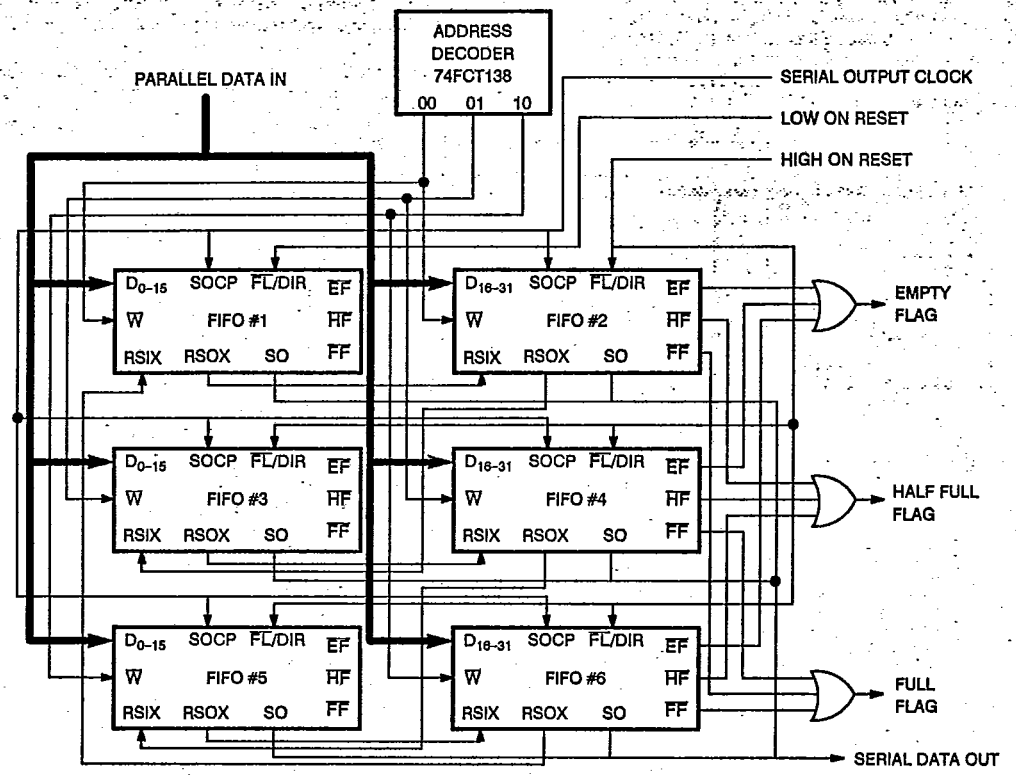


**Figure 13. A 3K x 32 Parallel-to-Serial FIFO using the IDT72125**

## ORDERING INFORMATION