Integrated Device Technology, Inc.

CMOS SINGLE BIT SyncFIFO™ 64 X 1, 256 x 1, 512 x 1

PRELIMINARY
IDT72423
IDT72203
IDT72213

FEATURES:

- 64 x 1-bit organization (IDT72423)
- 256 x 1-bit organization (IDT72203)
- 512 x 1-bit organization (IDT72213)
- 10 ns read/write cycle time (IDT72423/72203/72213)
- Independent read and write clock lines
- Empty and Full flags signal FIFO status
- Programmable Almost-Empty and Almost-Full flags can be programmed to any depth via a dedicated port (Pn). These flags default to Empty+7 and Full-7, respectively.
- Output enable puts output data bus in high impedance state
- Available in 24-pin SOIC, 24-pin plastic DIP (300 mil.), and 24-pin ceramic DIP (300 mil.)
- Military product compliant to MIL-STD-883, Class B Advanced submicron CMOS technology

DESCRIPTION:

The IDT72423/72203/72213 SyncFIFO™ are very high-speed, low-power First-In, First-Out (FIFO) memories with a word width of 1 and clocked read and write controls. The IDT72423/72203/72213 have a 64, 256, and 512 x 1-bit memory arrays, respectively. These FIFOs are appropriate for a wide variety of serial data buffering needs, especially telecommunications applications such as networks, modems, signal processing, and serial interfaces.

These single-bit FIFOs have 1-bit input (D) and output ports (Q). The input port is controlled by a free-running clock (WCLK), and two write enable pins ($\overline{WEN1}$, WEN2). Data is written into the Synchronous FIFO on every rising clock edge when the write enable pins are asserted. The output port is controlled by another clock pin (RCLK) and a read enable pin ($\overline{REN}$). The read clock can be tied to the write clock for single clock operation or the two clocks can run asynchronous of one another for dual clock operation. An output enable pin ($\overline{OE}$) is provided on the read port for three-state control of the output.

The Synchronous FIFOs have two fixed flags, Empty ($\overline{EF}$) and Full ($\overline{FF}$). Two programmable flags, Almost-Empty ($\overline{PAE}$) and Almost-Full ($\overline{PAF}$), are provided for improved system control. The programmable flags default to Empty+7 and Full-7 for $\overline{PAE}$ and $\overline{PAF}$, respectively. The programmable flag offset is loaded via the Program Inputs (P0 - P7), on the rising WCLK when the load pin ($\overline{LD}$) is asserted.

The IDT72423/72203/72213/ are fabricated using IDT's high-speed submicron CMOS technology. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

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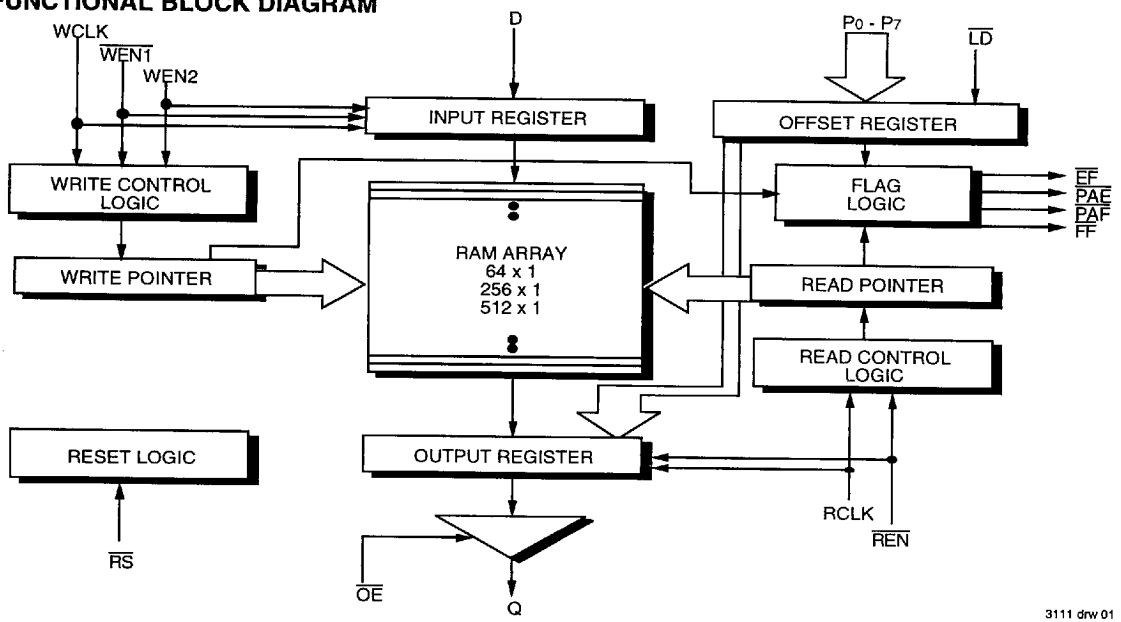
FUNCTIONAL BLOCK DIAGRAM



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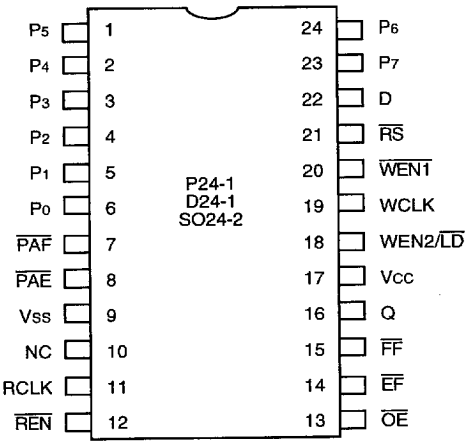
PIN CONFIGURATION



DIP/SOIC
TOP VIEW

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PIN DESCRIPTIONS

Symbol	Name	I/O	Description
D	Data Input	I	Input for serial data.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is set LOW, internal read and write pointers are set to the first location of the RAM array, $\overline{FF}$ and $\overline{PAF}$ go HIGH, and $\overline{PAE}$ and $\overline{EF}$ go LOW. A reset is required before an initial WRITE after power-up.
WCLK	Write Clock	I	Data is written into the FIFO on a LOW-to-HIGH transition of WCLK when the Write Enable(s) are asserted.
$\overline{WEN1}$	Write Enable 1	I	If the FIFO is configured to have programmable flags, $\overline{WEN1}$ is the only write enable pin. When $\overline{WEN1}$ is LOW, data is written into the FIFO on every LOW-to-HIGH transition WCLK. If the FIFO is configured to have two write enables, $\overline{WEN1}$ must be LOW and WEN2 must be HIGH to write data into the FIFO. Data will not be written into the FIFO if the $\overline{FF}$ is LOW.
WEN2/$\overline{LD}$	Write Enable 2/ Load	I	The FIFO is configured at reset to have either two write enables or programmable flags. If WEN2/$\overline{LD}$ is HIGH at reset, this pin operates as a second write enable. If WEN2/$\overline{LD}$ is LOW at reset, this pin operates as a control to load and read the programmable flag offsets. If the FIFO is configured to have two write enables, $\overline{WEN1}$ must be LOW and WEN2 must be HIGH to write data into the FIFO. Data will not be written into the FIFO if the $\overline{FF}$ is LOW. If the FIFO is configured to have programmable flags, WEN2/$\overline{LD}$ is held LOW to write or read the programmable flag offsets.
P0-P7	Program Inputs	I	Offsets for the programmable flag registers are entered at these inputs on the rising edge of WCLK when $\overline{LD}$ and $\overline{WEN}$ are LOW
Q	Data Output	O	Output for serial data.
RCLK	Read Clock	I	Data is read from the FIFO on a LOW-to-HIGH transition of RCLK when $\overline{REN}$ is asserted.
$\overline{REN}$	Read Enable 1	I	When $\overline{REN}$ is LOW, data is read from the FIFO on every LOW-to-HIGH transition of RCLK. Data will not be read from the FIFO if the $\overline{EF}$ is LOW.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is LOW, the data output bus is active. If $\overline{OE}$ is HIGH, the output data bus will be in a high impedance state.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ is LOW, the FIFO is empty and further data reads from the output are inhibited. When $\overline{EF}$ is HIGH, the FIFO is not empty. $\overline{EF}$ is synchronized to RCLK.
$\overline{PAE}$	Programmable Almost-Empty Flag	O	When $\overline{PAE}$ is LOW, the FIFO is almost empty based on the offset programmed into the FIFO. The default offset at reset is Empty+7. $\overline{PAE}$ is synchronized to RCLK.
$\overline{PAF}$	Programmable Almost-Full Flag	O	When $\overline{PAF}$ is LOW, the FIFO is almost full based on the offset programmed into the FIFO. The default offset at reset is Full-7. $\overline{PAF}$ is synchronized to WCLK.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ is LOW, the FIFO is full and further data writes into the input are inhibited. When $\overline{FF}$ is HIGH, the FIFO is not full. $\overline{FF}$ is synchronized to WCLK.
VCC	Power		One +5Volt power supply pin.
GND	Ground		One 0Volt ground pin.

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ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +135	°C
I_{OUT}	DC Output Current	50	50	mA

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NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CCC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage Commercial	2.0	—	—	V
V_{IH}	Input High Voltage Military	2.2	—	—	V
V_{IL}	Input Low Voltage Commercial & Military	—	—	0.8	V

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CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}(2)	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}(1,2)	Output Capacitance	V_{OUT} = 0V	10	pF

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NOTES:
1. With output deselected ($\overline{OE}$ = HIGH).
2. Characterized values, not currently tested.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

Symbol	Parameter	IDT72423 IDT72203 IDT72213 Commercial t_{CLK} = 10, 12, 15ns Min.	Typ.	Max.	IDT72423 IDT72203 IDT72213 Military t_{CLK} = 15, 25ns Min.	Typ.	Max.	Unit
I_{LI}(1)	Input Leakage Current (Any Input)	–1	—	1	–10	—	10	µA
I_{LO}(2)	Output Leakage Current	–10	—	10	–10	—	10	µA
V_{OH}	Output Logic "1" Voltage, I_{OH} = -2 mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage, I_{OL} = 8 mA	—	—	0.4	—	—	0.4	V
I_{CC}(3)	Active Power Supply Current	—	—	80	—	—	100	mA

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NOTES:
1. Measurements with 0.4 ≤ V_{IN} ≤ V_{CC}.
2. $\overline{OE}$ ≥ V_{IH}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
3. Measurements are made with outputs unloaded. Tested at f_{CLK} = 20MHz.

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AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to + 70°C; Military: V_{CC} = 5V ± 10%, T_A = –55°C to +125°C)

		Commmercial				Com'l & Mil.		Military		
		72423L10 72203L10 72213L10		72423L12 72203L12 72213L12		72423L15 72203L15 72213L15		72423L25 72203L25 72213L25		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
fS	Clock Cycle Frequency	100	—	—	83.3	—	66.7	—	40	Mhz
tA	Data Access Time	2	7.5	2	8	2	10	3	15	ns
tCLK	Clock Cycle Time	10	—	12	—	15	—	25	—	ns
tCLKH	Clock High Time	4.5	—	5	—	6	—	10	—	ns
tCLKL	Clock Low Time	4.5	—	5	—	6	—	10	—	ns
tDS	Data Set-up Time	3	—	3	—	4	—	6	—	ns
tDH	Data Hold Time	0	—	0	—	1	—	1	—	ns
tENS	Enable Set-up Time	3	—	3	—	4	—	6	—	ns
tENH	Enable Hold Time	0	—	0.2	—	1	—	1	—	ns
tRS	Reset Pulse Width[1]	10	—	12	—	15	—	25	—	ns
tRSS	Reset Set-up Time	10	—	12	—	15	—	25	—	ns
tRSR	Reset Recovery Time	10	—	12	—	15	—	25	—	ns
tRSF	Reset to Flag and Output Time	10	—	—	12	—	15	—	25	ns
tOLZ	Output Enable to Output in Low-Z[2]	0	—	0	—	0	—	0	—	ns
tOE	Output Enable to Output Valid	3	6.5	3	7	3	8	3	13	ns
tOHZ	Output Enable to Output in High-Z[2]	3	6.5	3	7	3	8	3	13	ns
tWFF	Write Clock to Full Flag	7.5	—	—	8	—	10	—	15	ns
tREF	Read Clock to Empty Flag	7.5	—	—	8	—	10	—	15	ns
tAF	Write Clock to Almost-Full Flag	7.5	—	—	8	—	10	—	15	ns
tAE	Read Clock to Almost-Empty Flag	7.5	—	—	8	—	10	—	15	ns
tSKEW1	Skew time between Read Clock & Write Clock for Empty Flag &Full Flag	5	—	5	—	6	—	10	—	ns
tSKEW2	Skew time between Read Clock & Write Clock for Almost-Empty Flag & Almost-Full Flag	22	—	22	—	28	—	40	—	ns

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NOTES:
1. Pulse widths less than minimum values are not allowed.
2. Values guaranteed by design, not currently tested.

AC TEST CONDITIONS

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

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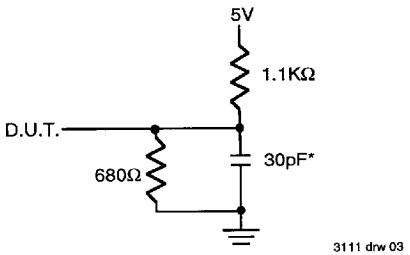

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or equivalent circuit

Figure 1. Output Load

*Includes jig and scope capacitances.

SIGNAL DESCRIPTIONS

INPUTS:

Data In (D) — Input for serial data.

CONTROLS:

Reset ($\overline{RS}$)—Reset is accomplished whenever the Reset ($\overline{RS}$) input is taken to a LOW state. During reset, both internal read and write pointers are set to the first location. A reset is required after power-up before a write operation can take place. The Full Flag ($\overline{FF}$) and Programmable Almost-Full Flag ($\overline{PAF}$) will be reset to HIGH after tRSF. The Empty Flag ($\overline{EF}$) and Programmable Almost-Empty Flag ($\overline{PAE}$) will be reset to low after tRSF. During reset, the output register is initialized to all zeros and the offset registers are initialized to their default values.

Write Clock (WCLK)—A write cycle is initiated on the LOW-to-HIGH transition of the write clock (WCLK). Data set-up and hold times must be met in respect to the LOW-to-HIGH transition of the write clock (WCLK). The Full Flag ($\overline{FF}$) and Programmable Almost-Full Flag ($\overline{PAF}$) are synchronized with respect to the LOW-to-HIGH transition of the write clock (WCLK).

The write and read clocks can be asynchronous or coincident.

Write Enable 1 ($\overline{WEN1}$)—If the FIFO is configured for programmable flags, Write Enable 1 ($\overline{WEN1}$) is the only enable control pin. In this configuration, when Write Enable 1 ($\overline{WEN1}$) is LOW, data can be loaded into the input register and RAM array on the LOW-to-HIGH transition of every write clock (WCLK). Data is stored in the RAM array sequentially and independently of any on-going read operation.

In this configuration, when Write Enable 1 ($\overline{WEN1}$) is HIGH, the input register holds the previous data and no new data is allowed to be loaded into the register.

If the FIFO is configured to have two write enables, which allows for depth expansion, there are two enable control pins. See Write Enable 2 paragraph below for operation in this configuration.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go LOW, inhibiting further write operations. Upon the completion of a valid read cycle, the Full Flag ($\overline{FF}$) will go high after tWFF, allowing a valid write to begin. Write Enable 1 ($\overline{WEN1}$) is ignored when the FIFO is full.

Read Clock (RCLK) — Data can be read on the outputs on the LOW-to-HIGH transition of the read clock (RCLK). The Empty Flag ($\overline{EF}$) and Programmable Almost-Empty Flag ($\overline{PAE}$) are synchronized with respect to the LOW-to-HIGH transition of the read clock (RCLK).

The write and read clocks can be asynchronous or coincident.

Read Enables ($\overline{REN}$)—When the Read Enable ($\overline{REN}$) is LOW, data is read from the RAM array to the output register on the LOW-to-HIGH transition of the read clock (RCLK).

When the Read Enable ($\overline{REN}$) is HIGH, the output register holds the previous data and no new data is allowed to be loaded into the register.

When all the data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go LOW, inhibiting further read operations. Once a valid write operation has been accomplished, the Empty Flag ($\overline{EF}$) will go HIGH after tREF and a valid read can begin. The Read Enable ($\overline{REN}$) is ignored when the FIFO is empty.

Output Enable ($\overline{OE}$)—When Output Enable ($\overline{OE}$) is enabled (LOW), the output buffer receives data from the output register. When Output Enable ($\overline{OE}$) is disabled (HIGH), the Q data output is in a high-impedance state.

Write Enable 2/Load (WEN2/$\overline{LD}$)—This is a dual-purpose pin. The FIFO is configured at Reset to have programmable flags or to have two write enables, which allows depth expansion. If Write Enable 2/Load (WEN2/$\overline{LD}$) is set HIGH at Reset ($\overline{RS}$ = LOW), this pin operates as a second write enable pin.

If the FIFO is configured to have two write enables, when Write Enable ($\overline{WEN1}$) is LOW and Write Enable 2/Load (WEN2/$\overline{LD}$) is HIGH, data can be loaded into the input register and RAM array on the LOW-to-HIGH transition of every write clock (WCLK). Data is stored in the RAM array sequentially and independently of any on-going read operation.

In this configuration, when Write Enable ($\overline{WEN1}$) is HIGH and/or Write Enable 2/Load (WEN2/$\overline{LD}$) is LOW, the input register holds the previous data and no new data is allowed to be loaded into the register.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go LOW, inhibiting further write operations. Upon the completion of a valid read cycle, the Full Flag ($\overline{FF}$) will go HIGH after tWFF, allowing a valid write to begin. Write Enable 1 ($\overline{WEN1}$) and Write Enable 2/Load (WEN2/$\overline{LD}$) are ignored when the FIFO is full.

The FIFO is configured to have programmable flags when the Write Enable 2/Load (WEN2/$\overline{LD}$) is set LOW at Reset ($\overline{RS}$ = LOW). The IDT72423/72203/72213 devices contain four 8-bit offset registers which can be loaded with data on the Program Inputs (P_0 - P_7). See Figure 3 for details of the size of the registers and the default values.

If the FIFO is configured to have programmable flags when the Write Enable 1 ($\overline{WEN1}$) and Write Enable 2/Load (WEN2/$\overline{LD}$) are set LOW, data on the Program Inputs (P_0 - P_7) are written into the Empty (Least Significant Bit) offset register on the first LOW-to-HIGH transition of the write clock (WCLK). Data is written into the Empty (Most Significant Bit) offset register on the second LOW-to-HIGH transition of the write clock (WCLK), into the Full (Least Significant Bit) offset register on the third transition, and into the Full (Most Significant Bit) offset register on the fourth transition. The fifth transition of the write clock (WCLK) again writes to the Empty (Least Significant Bit) offset register.

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However, writing all offset registers does not have to occur at one time. One or two offset registers can be written and then by bringing the Write Enable 2/Load (WEN2/$\overline{LD}$) pin HIGH, the FIFO is returned to normal read/write operation. When the Write Enable 2/Load (WEN2/$\overline{LD}$) pin is set LOW, and Write Enable 1 ($\overline{WEN1}$) is LOW, the next offset register in sequence is written.

Program Inputs (P0 - P7)—Flag offsets on these inputs are entered into the programmable offset registers on the rising edge of WCLK when $\overline{LD}$ and $\overline{WEN}$ are LOW.

LD	WEN1	WCLK[1]	Selection
0	0	↑	Empty Offset (LSB) Empty Offset (MSB) Full Offset (LSB) Full Offset (MSB)
0	1	↑	No Operation
1	0	↑	Write into FIFO
1	1	↑	No Operation

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Figure 2. Write Offset Register

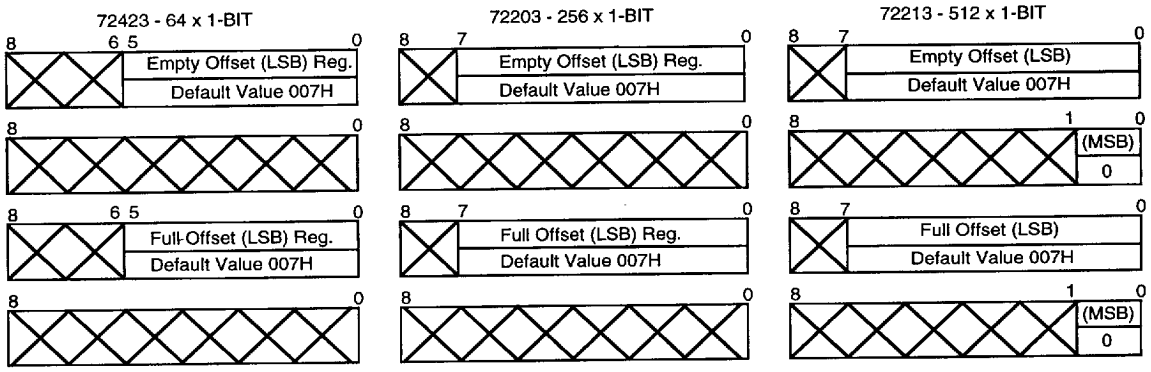

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Figure 3. Offset Register Location and Default Values

OUTPUTS:

Full Flag ($\overline{FF}$)—The Full Flag ($\overline{FF}$) will go LOW, inhibiting further write operation, when the device is full. If no reads are performed after Reset ($\overline{RS}$), the Full Flag ($\overline{FF}$) will go LOW after 64 writes for the IDT72423, 256 writes for the IDT72203, 512 writes for the IDT72213.

The Full Flag ($\overline{FF}$) is synchronized with respect to the LOW-to-HIGH transition of the write clock (WCLK).

Empty Flag ($\overline{EF}$)—The Empty Flag ($\overline{EF}$) will go LOW, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating the device is empty.

The Empty Flag ($\overline{EF}$) is synchronized with respect to the LOW-to-HIGH transition of the read clock (RCLK).

Programmable Almost-Full Flag ($\overline{PAF}$)—The Programmable Almost-Full Flag ($\overline{PAF}$) will go LOW when the FIFO reaches the Almost-Full condition. If no reads are performed after Reset ($\overline{RS}$), the Programmable Almost-Full Flag ($\overline{PAF}$) will go LOW after (64-m) writes for the IDT72423, (256-m) writes for the IDT72203, (512-m) writes for the IDT72213. The offset "m" is defined in the Full offset registers.

If there is no Full offset specified, the Programmable Almost-Full Flag ($\overline{PAF}$) will go LOW at Full-7 words.

The Programmable Almost-Full Flag ($\overline{PAF}$) is synchronized with respect to the LOW-to-HIGH transition of the write clock (WCLK).

Programmable Almost-Empty Flag ($\overline{PAE}$)—The Programmable Almost-Empty Flag ($\overline{PAE}$) will go LOW when the read pointer is "n+1" locations less than the write pointer. The offset "n" is defined in the Empty offset registers. If no reads are performed after Reset the Programmable Almost-Empty Flag ($\overline{PAE}$) will go HIGH after "n+1" for the IDT72423/72203/72213. If there is no Empty offset specified, the Programmable Almost-Empty Flag ($\overline{PAE}$) will go LOW at Empty+7 words.

The Programmable Almost-Empty Flag ($\overline{PAE}$) is synchronized with respect to the LOW-to-HIGH transition of the read clock (RCLK).

Data Outputs (Q) — Output for serial data.

TABLE 1: STATUS FLAGS

NUMBER OF WORDS IN FIFO						
72423	72203	72213	$\overline{FF}$	$\overline{PAF}$	$\overline{PAE}$	$\overline{EF}$
0	0	0	H	H	L	L
1 to n[1]	1 to n[1]	1 to n[1]	H	H	L	H
(n+1) to (64-(m+1))	(n+1) to (256-(m+1))	(n+1) to (512-(m+1))	H	H	H	H
(64-m)[2] to 63	(256-m)[2] to 255	(512-m)[2] to 511	H	L	H	H
64	256	512	L	L	H	H

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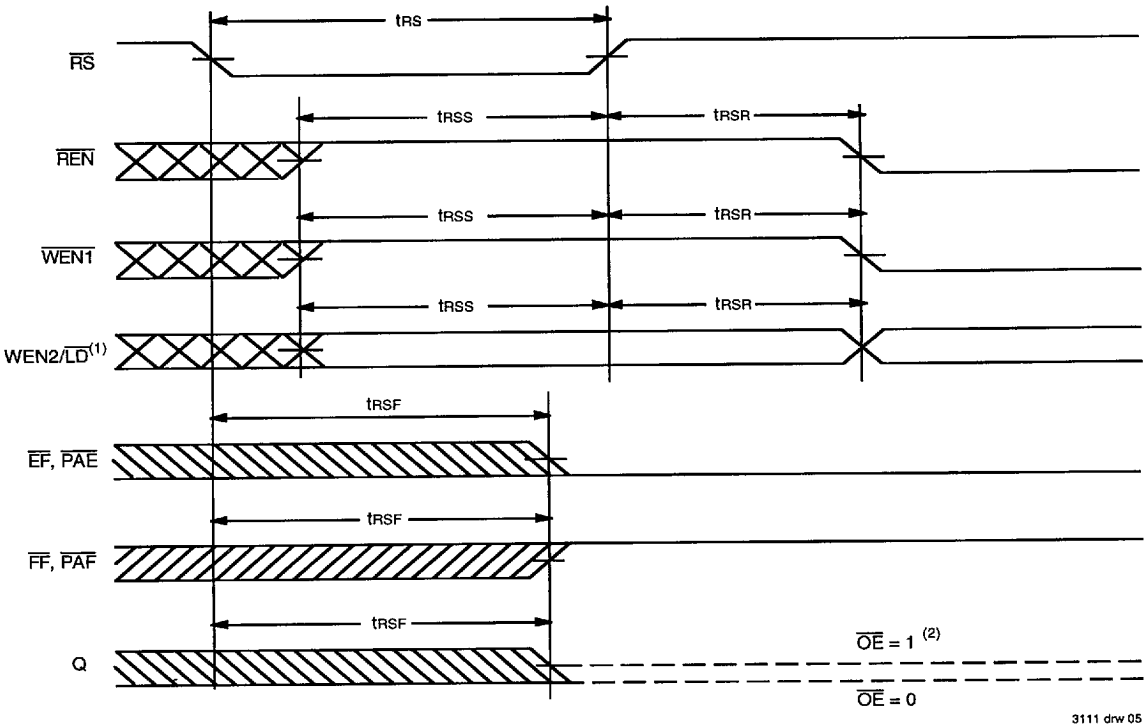
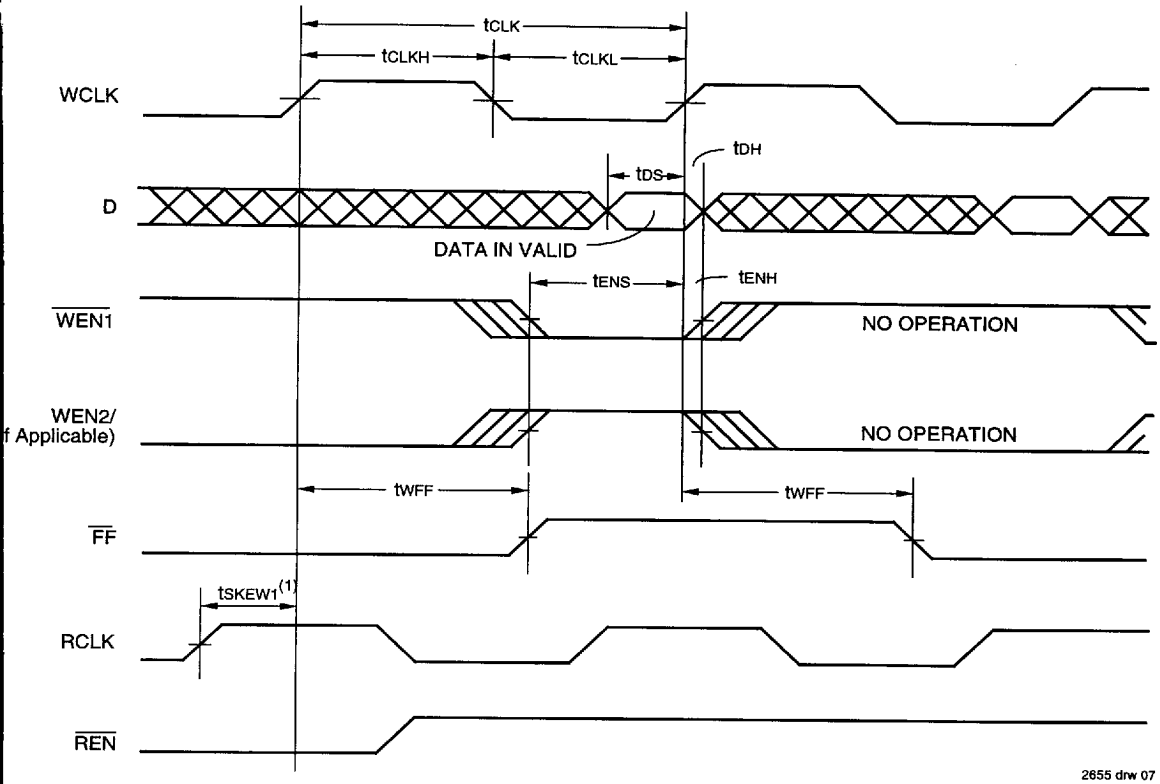
NOTES:
1. n = Empty Offset (n = 7 default value)
2. m = Full Offset (m = 7 default value)



NOTES:
1. Holding WEN2/$\overline{LD}$ HIGH during reset will make the pin act as a second write enable pin. Holding WEN2/$\overline{LD}$ LOW during reset will make the pin act as a load enable for the programmable flag offset registers.
2. After reset, the outputs will be LOW if $\overline{OE}$ = 0 and tri-state if $\overline{OE}$ = 1.
3. The clocks (RCLK, WCLK) can be free-running during reset.

Figure 4. Reset Timing



NOTE:
1. tSKEW1 is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{FF}$ to change during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than tSKEW1, then $\overline{EF}$ may not change state until the next RCLK edge.

Figure 5. Write Cycle Timing

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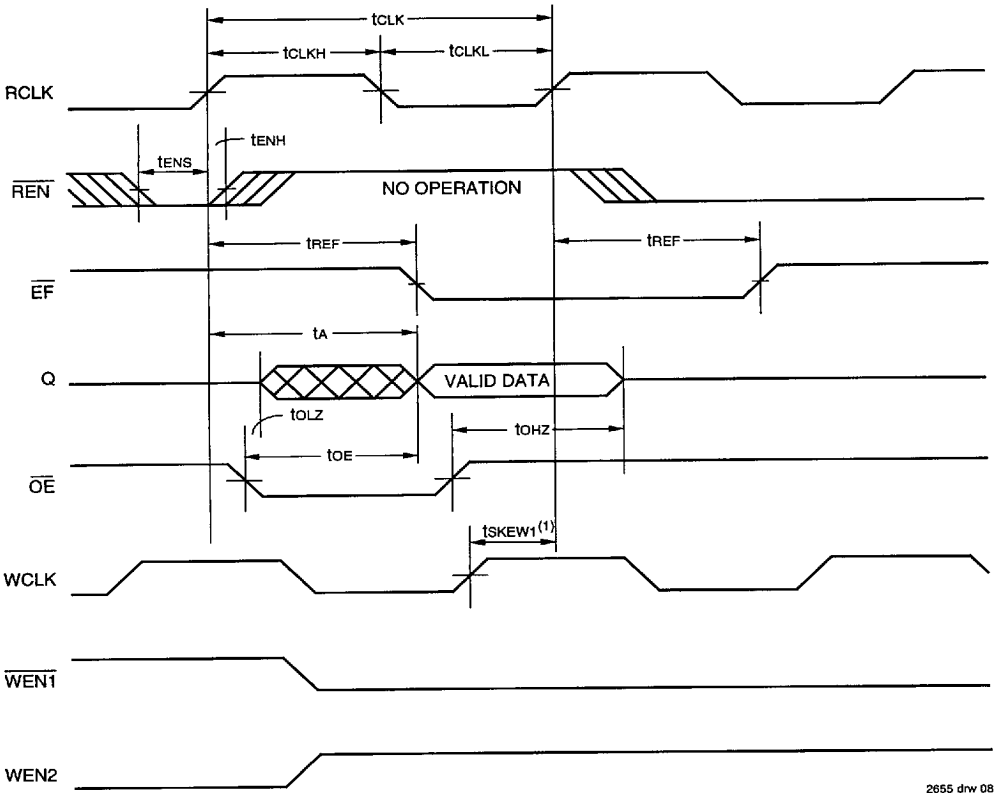
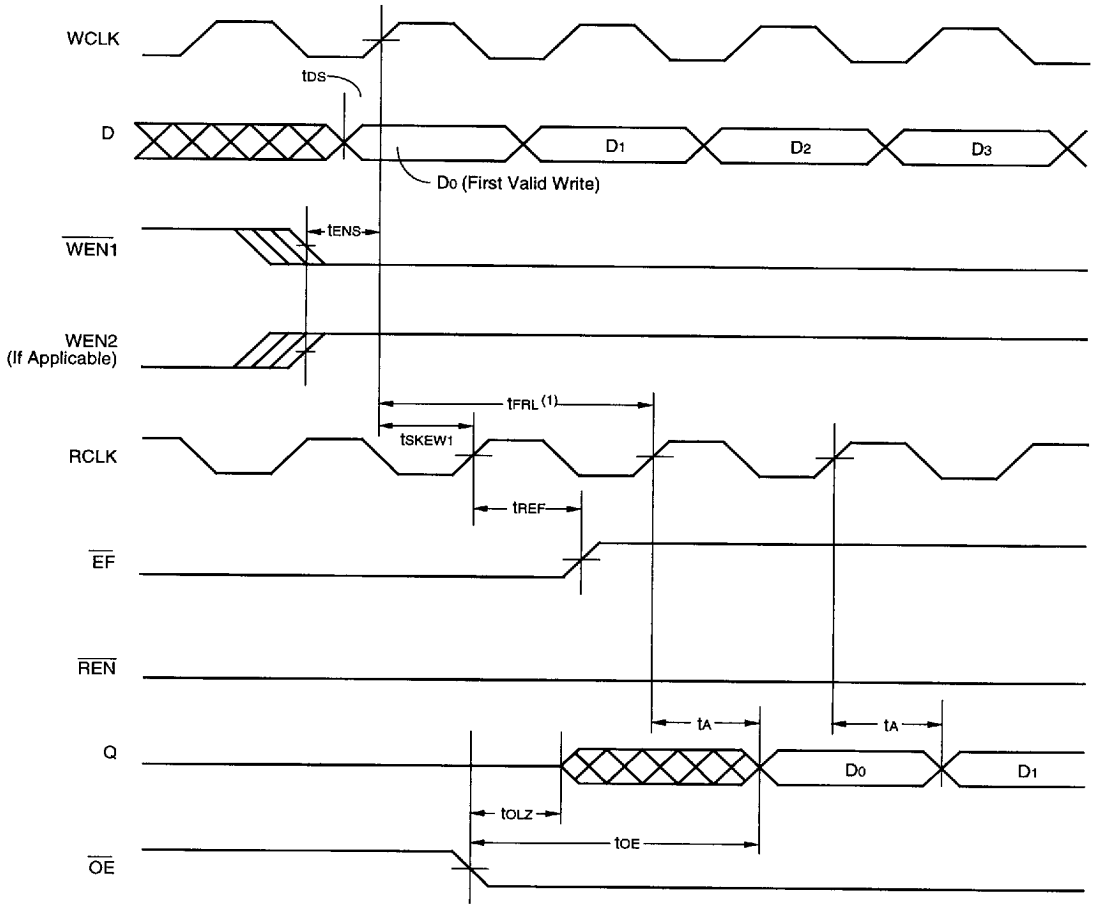


Note:
1. tSKEW1 is the minimum time between a rising WCLK edge and a rising RCLK edge for $\overline{EF}$ to change during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than tSKEW1, then $\overline{EF}$ may not change state until the next RCLK edge. Figure 6. Read Cycle - Timing

Figure 6. Read Cycle Timing



Note:
1. When $t_{SKEW1} \geq$ minimum specification, $t_{FRL} = t_{CLK} + t_{SKEW1}$
   When $t_{SKEW1} <$ minimum specification, $t_{FRL} = 2t_{CLK} + t_{SKEW1}$ or $t_{CLK} + t_{SKEW1}$
   The Latency Timings apply only at the Empty Boundary ($\overline{EF}$ = LOW).

Figure 7. First Data Word Latency Timing

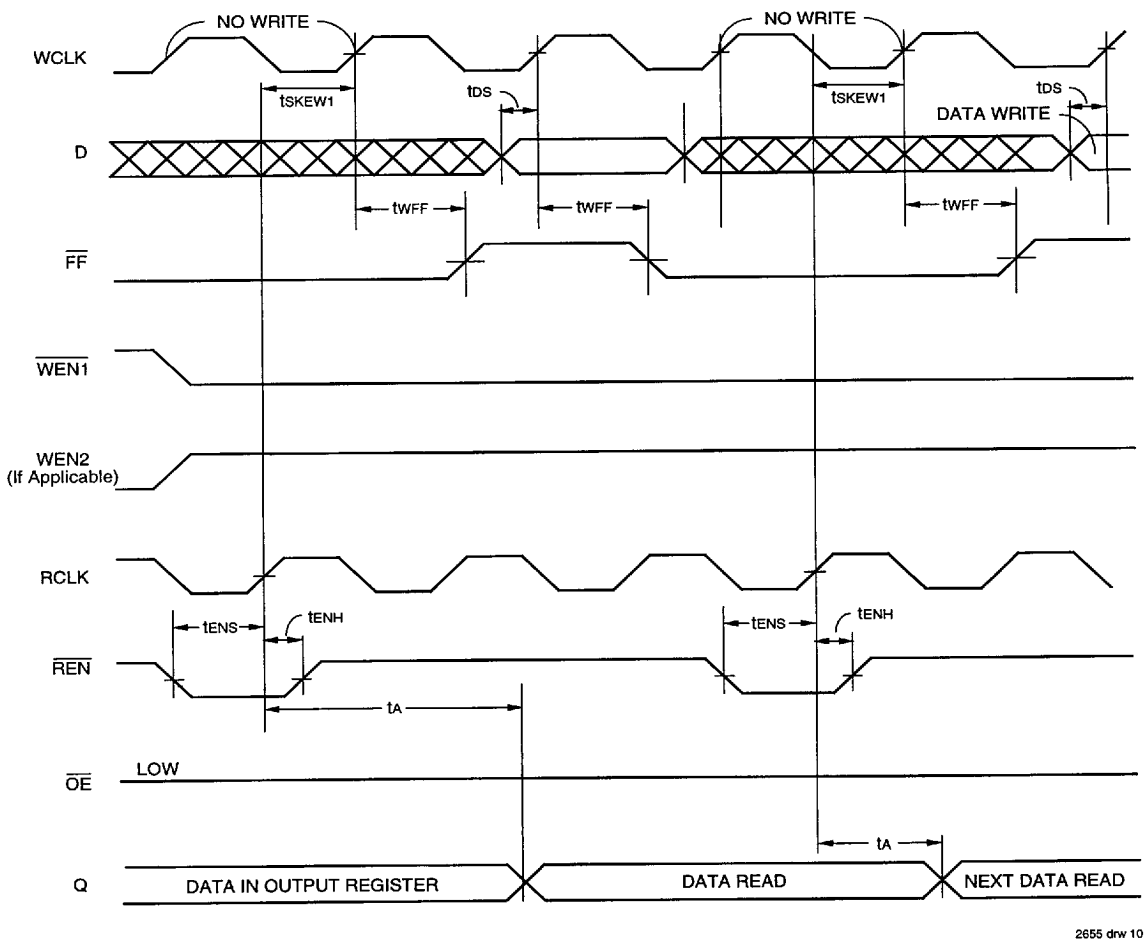
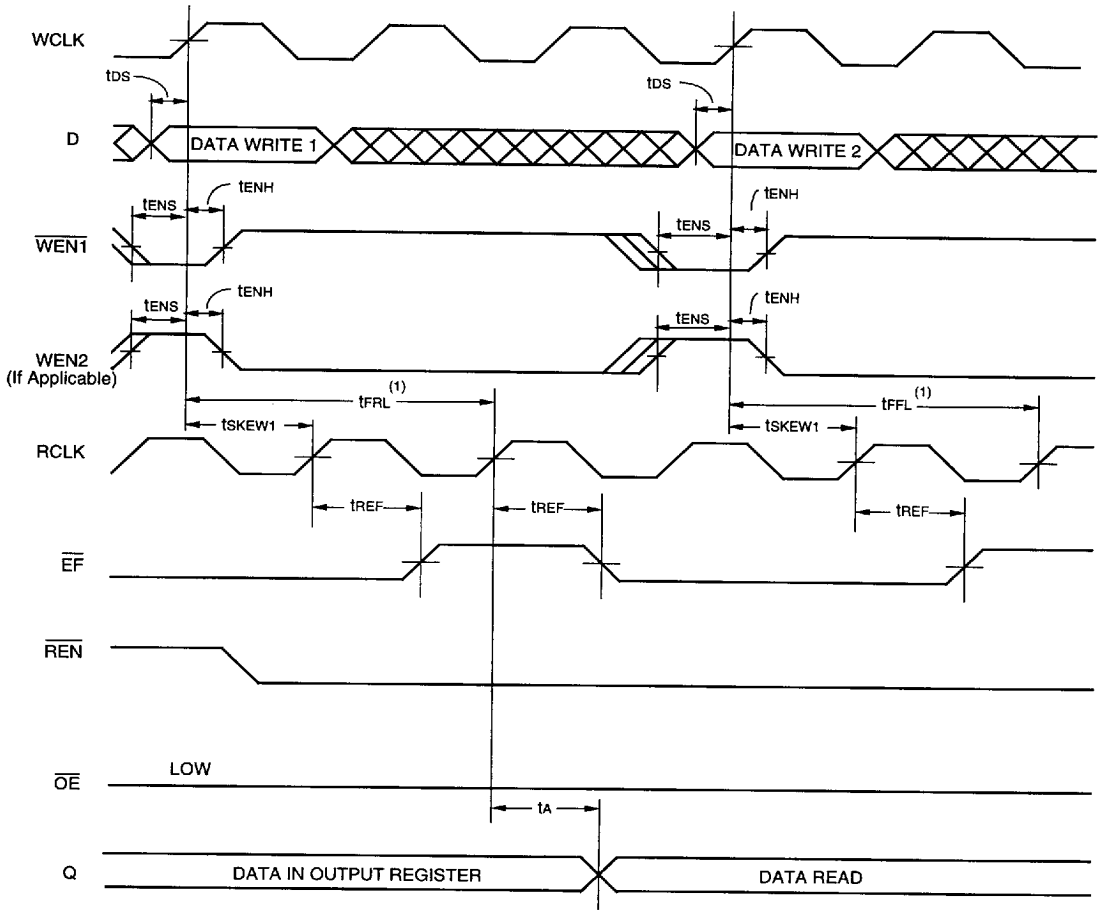


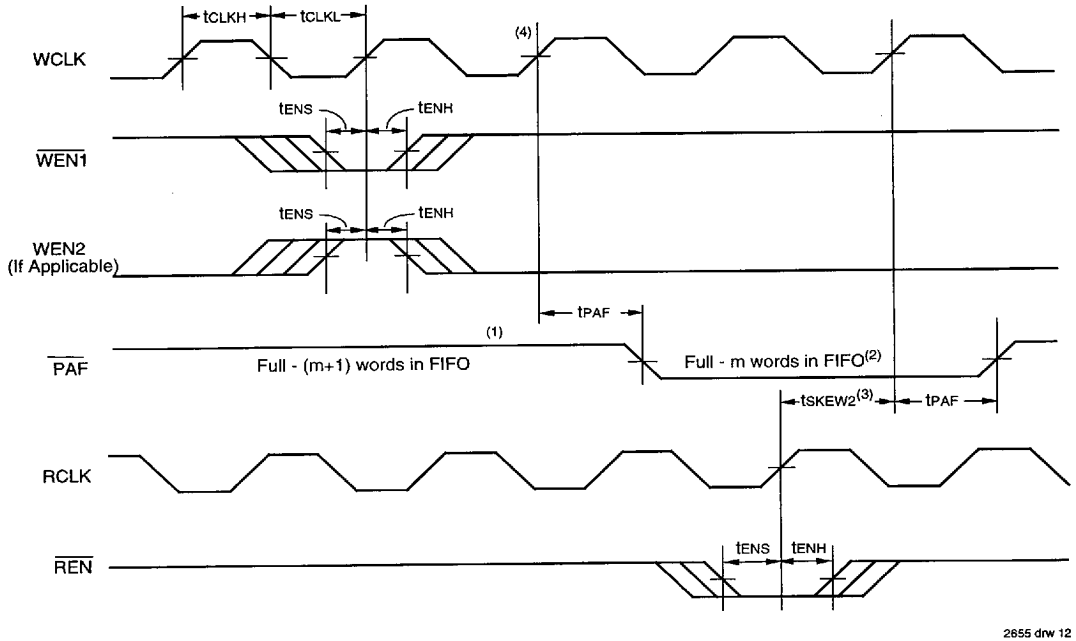
Figure 8. Full Flag Timing



Note:
1. When $t_{SKEW1} \geq$ minimum specification, t_{FRL} maximum = $t_{CLK} + t_{SKEW1}$
   When $t_{SKEW1} <$ minimum specification, t_{FRL} maximum = $2t_{CLK} + t_{SKEW1}$ or $t_{CLK} + t_{SKEW1}$
   The Latency Timings apply only at at the Empty Boundary ($\overline{EF}$ = LOW).

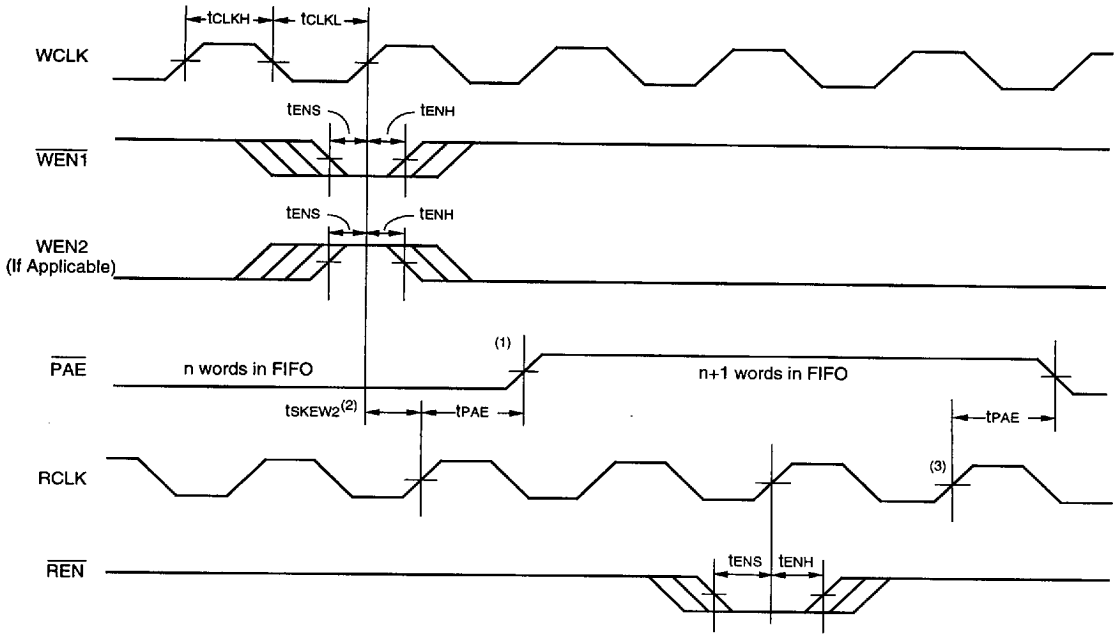
Figure 9. Empty Flag Timing

5



NOTES:
1. PAF offset = m.
2. 64 - m words in for IDT72423, 256 - m words in FIFO for IDT72203, 512 - m words for IDT72213.
3. t_{SKEW2} is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{PAF}$ to change during that clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW2}, then $\overline{PAF}$ may not change state until the next WCLK rising edge.
4. If a write is performed on this rising edge of the write clock, there will be Full - (m-1) words in the FIFO when $\overline{PAF}$ goes LOW.

Figure 10. Programmable Full Flag Timing



NOTES:
1. PAE offset = n.
2. t_{SKEW2} is the minimum time between a rising WCLK edge and a rising RCLK edge for $\overline{PAE}$ to change during that clock cycle. If the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then $\overline{PAE}$ may not change state until the next RCLK rising edge.
3. If a read is performed on this rising edge of the read clock, there will be Empty + (n-1) words in the FIFO when $\overline{PAE}$ goes LOW.

Figure 11. Programmable Empty Flag Timing

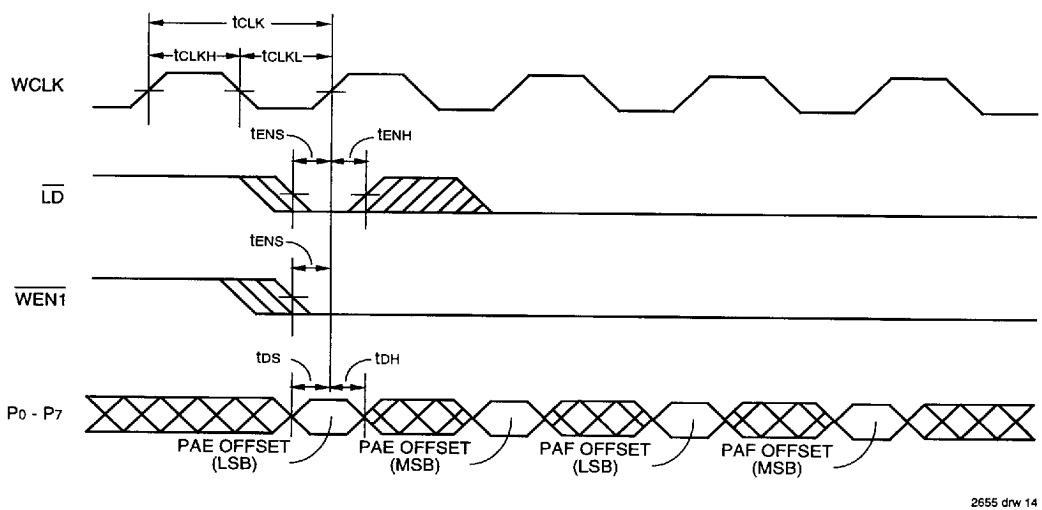


Figure 12. Write Offset Registers Timing

OPERATING CONFIGURATIONS

SINGLE DEVICE CONFIGURATION—A single IDT72423/72203/72213 may be used when the application requirements are for 64/256/512 bits or less. In this configuration, the Write Enable 2/Load (WEN2/$\overline{LD}$) pin is set LOW at Reset so that the pin operates as a control to load and read the programmable flag offsets.

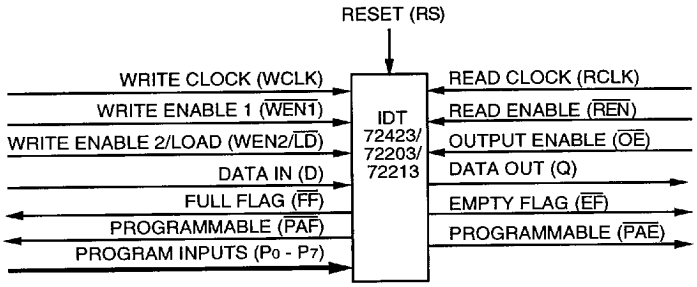


Figure 14. Block Diagram of Single 64 x 1/256 x 1/512 x 1 Synchronous FIFO

DEPTH EXPANSION—The IDT72423/72203/72213 can be adapted to applications when the requirements are for greater than 64/256/512 words. The existence of two enable pins on the write port facilitates depth expansion. The Write Enable 2/Load pin is used as a second write enable in a depth expansion configuration thus the Programmable flags are set to the default values. Two read enables can be created by adding a two-input AND gate to the $\overline{REN}$ line of the FIFO. Depth expansion is possible by using one enable input for system control while the other enable input is controlled by expansion logic to direct the flow of data. A typical application would have the expansion logic alternate data access from one device to the next in a sequential manner. The IDT72423/72203/72213 operates in the Depth Expansion configuration when the following conditions are met:

1. The WEN2/$\overline{LD}$ pin is held HIGH during Reset so that this pin operates a second Write Enable.
2. An external two-input AND gate is used to create two read enables, $\overline{REN1}$ and $\overline{REN2}$. The output of the AND gate is tied to the $\overline{REN}$ pin of the FIFO device, one input of the AND gate is designated $\overline{REN1}$, the other $\overline{REN2}$.
3. External logic is used to control the flow of data.

Please see the Application Note "Depth Expansion of IDT's Synchronous FIFOs Using the Ring Counter Approach" for details of this configuration.

ORDERING INFORMATION