Integrated Device Technology, Inc.

CMOS PARALLEL SyncFIFO™ (CLOCKED FIFO) 512 x 18-BIT & 1024 x 18-BIT

PRELIMINARY
IDT72215A
IDT72225A

FEATURES:

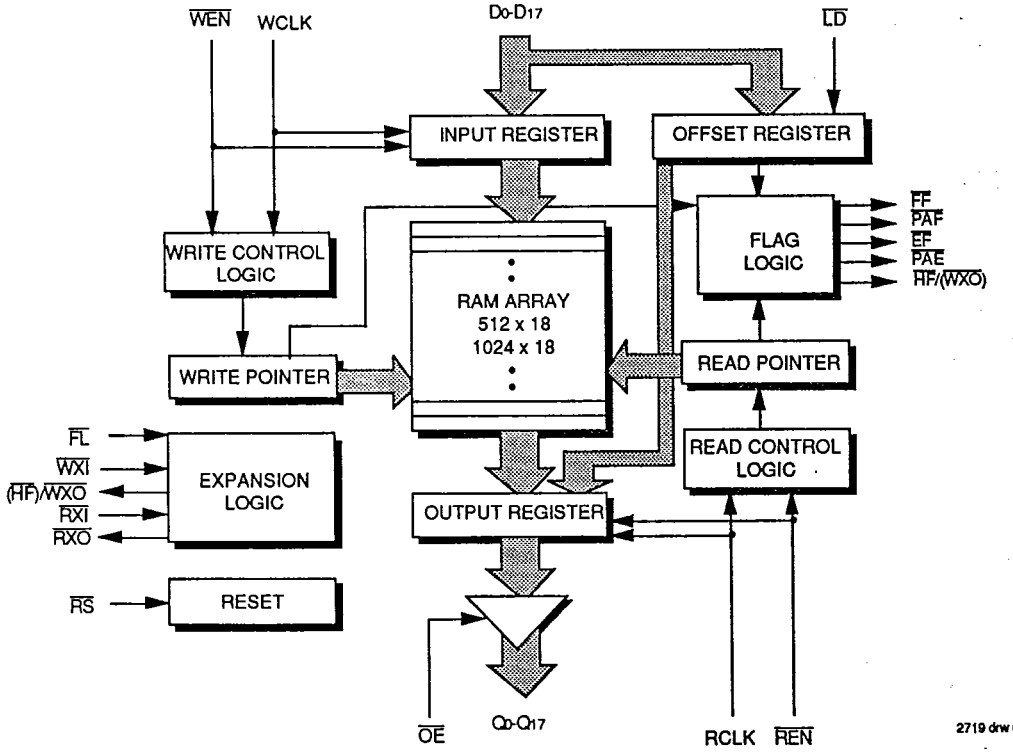
- 512 x 18-bit and 1024 x 18-bit memory array structures
- 20ns read / write cycle time
- Easily expandable in depth and width
- Read and write clocks can be asynchronous or coincident
- Dual-port zero fall-through time architecture
- Programmable almost-empty and almost-full flags
- Empty and Full flags signal FIFO status
- Half-Full flag capability in a single device configuration
- Output enable puts output data bus in high impedance
- First device controls all flag logic in depth expansion
- Produced with advanced submicron CEMOS™ technology
- Available in a 68-lead pin grid array (PGA), and plastic leaded chip carrier (PLCC)
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

The IDT72215A and IDT72225A are very high speed, low-power first-in, first-out (FIFO) memories with clocked read and write controls. The IDT72215A has a 512 x 18-bit memory array, while the IDT72225A has a 1024 x 18-bit memory array. These FIFOs are applicable for a wide variety of data buffering needs, such as optical disk controllers, local area networks (LANs), and interprocessor communication.

Both FIFOs have 18-bit input and output ports. The input port is controlled by a free-running clock (WCLK), and a data input enable pin ($\overline{WEN}$). Data is read into the synchonous FIFO on every clock when $\overline{WEN}$ is asserted. The output port is controlled by another clock pin (RCLK) and another enable pin ($\overline{REN}$). The read clock can be tied to the write clock for single clock operation or the two clocks can run asynchronous of one another for dual clock operation. An output enable pin ($\overline{OE}$) is provided on the read port for three-state control of the output.

FUNCTIONAL BLOCK DIAGRAM



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DESCRIPTION (Continued):

The synchronous FIFOs have two fixed flags, Empty ($\overline{EF}$) and Full ($\overline{FF}$), and two programmable flags, Almost-Empty ($\overline{PAE}$) and Almost-Full ($\overline{PAF}$). The offset loading of the programmable flags is controlled by a simple state machine, and is initiated by asserting the load pin ($\overline{LD}$). A Half-Full flag ($\overline{HF}$) is available when the FIFO is used in a single device configuration.

The IDT72215A and IDT72225A are depth expandable using a daisy-chain technique. The $\overline{XI}$ and $\overline{XO}$ pins are used to expand the FIFOs. To permit programmable flags in depth expansion, the first device indicated by setting $\overline{FL}$ to low, controls the flags.

The IDT72215A/72225A is fabricated using IDT's high speed submicron CEMOS technology. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

PIN CONFIGURATIONS

	A	B	C	D	E	F	G	H	J	K	L
11		Vcc	Q3	GND	Q0	$\overline{WXO/HF}$	$\overline{RXI}$	Vcc	$\overline{WEN}$	$\overline{FL}$	
10	GND	Q4	Q2	Q1	$\overline{RXO}$	$\overline{FF}$	$\overline{PAF}$	$\overline{WXI}$	WCLK	$\overline{PAE}$	D0
09	Q6	Q5								D2	D1
08	Q7	Vcc								D4	D3
07	GND	Q8								D6	D5
06	Q10	Q9								GND	D7
05	Q11	Vcc								Vcc	D8
04	GND	Q12								D10	D9
03	Q14	Q13								D12	D11
02	Vcc	Q15	Q16	Vcc	GND	$\overline{RS}$	$\overline{LD}$	RCLK	D17	D14	D13
01		GND	Q17	$\overline{EF}$	Vcc	$\overline{OE}$	$\overline{REN}$	GND	D16	D15	

Pin 1 Designator

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PGA
TOP VIEW

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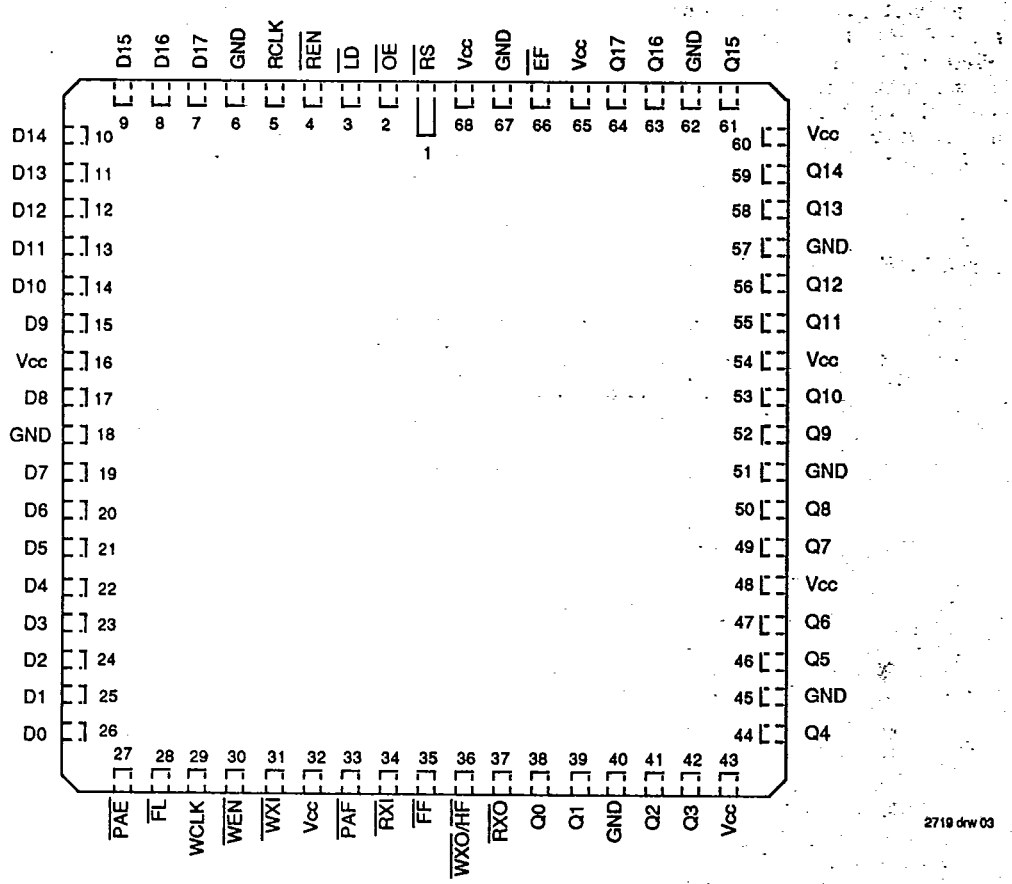
PIN CONFIGURATIONS (Continued)



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PLCC
TOP VIEW

PIN DESCRIPTIONS

Symbol	Name	I/O	Description
D_0 - D_{17}	Data Inputs	I	Data inputs for a 18-bit bus.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is set low, internal read and write pointers are set to the first location of the RAM array, $\overline{FF}$ and $\overline{PAF}$ go high, and $\overline{PAE}$ and $\overline{EF}$ go low. A reset is required before an initial WRITE after power-up.
WCLK	Write Clock	I	Data is written into the FIFO on a LOW-to-HIGH transition of WCLK when Write Enable $\overline{WEN}$ is asserted (LOW).
$\overline{WEN}$	Write Enable	I	When $\overline{WEN}$ is LOW, data is written into the FIFO on every LOW-to-HIGH transition of WCLK. When $\overline{WEN}$ is high, the FIFO holds the previous data. Data will not be written into the FIFO if the $\overline{FF}$ is LOW.
RCLK	Read Clock	I	Data is read from the FIFO on a LOW-to-HIGH transition of RCLK when Read Enable $\overline{REN}$ is asserted (LOW).
$\overline{REN}$	Read Enable	I	When $\overline{REN}$ is LOW, data is read from the FIFO on every LOW-to-HIGH transition of RCLK. When $\overline{REN}$ is high, the output register holds the previous data. Data will not be read from the FIFO if the $\overline{EF}$ is LOW.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is LOW, the data output bus is active. If $\overline{OE}$ is HIGH, the output data bus will be in a high impedance state.
$\overline{LD}$	Load	I	When $\overline{LD}$ is LOW, data on the inputs D_0-D_{15} is written to the offset and depth registers on the LOW-to-HIGH transition of the WCLK, when $\overline{WEN}$ is LOW. When $\overline{LD}$ is LOW, data on the outputs Q_0-Q_{15} is read from the offset and depth registers on the LOW-to-HIGH transition of the RCLK, when $\overline{REN}$ is LOW.
$\overline{FL}$	First Load	I	In the single device or width expansion configuration, $\overline{FL}$ is grounded. In the depth expansion configuration, $\overline{FL}$ is grounded on the first device (first load device) and set to high for all other devices in the daisy chain.
$\overline{WXI}$	Write Expansion Input	I	In the single device or width expansion configuration, $\overline{WXI}$ is grounded. In the depth expansion configuration, $\overline{WXI}$ is connected to $\overline{WXO}$ (Write Expansion Out) of the previous device.
$\overline{RXI}$	Read Expansion Input	I	In the single device or width expansion configuration, $\overline{RXI}$ is grounded. In the depth expansion configuration, $\overline{RXI}$ is connected to $\overline{RXO}$ (Read Expansion Out) of the previous device.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ is LOW, the FIFO is empty and further data reads from the output are inhibited. When $\overline{EF}$ is HIGH, the FIFO is not empty. $\overline{EF}$ is synchronized to RCLK.
$\overline{PAE}$	Programmable Almost-Empty Flag	O	When $\overline{PAE}$ is LOW, the FIFO is almost empty based on the offset programmed into the FIFO. The default offset at reset is 1/8 full.
$\overline{PAF}$	Programmable Almost-Full Flag	O	When $\overline{PAF}$ is LOW, the FIFO is almost full based on the offset programmed into the FIFO. The default offset at reset is 7/8 full.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ is LOW, the FIFO is full and further data writes into the input are inhibited. When $\overline{FF}$ is HIGH, the FIFO is not full. $\overline{FF}$ is synchronized to WCLK.
$\overline{WXO}/\overline{HF}$	Write Expansion Out/Half-Full Flag	O	In the single device or width expansion configuration, the device is more than half full when $\overline{HF}$ is LOW. In the depth expansion configuration, a pulse is sent from $\overline{WXO}$ to $\overline{WXI}$ of the next device when the last location in the FIFO is written.
$\overline{RXO}$	Read Expansion Out	O	In the depth expansion configuration, a pulse is sent from $\overline{RXO}$ to $\overline{RXI}$ of the next device when the last location in the FIFO is read.
Q_0 - Q_{17}	Data Outputs	O	Data outputs for a 18-bit bus.
V_{CC}	Power		Eight +5 volt power supply pins.
GND	Ground		Eight 0 volt ground pins.

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ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +155	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2719 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.

CAPACITANCE (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter(1)	Condition	Max.	Unit
C_{IN}(2)	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}(1,2)	Output Capacitance	V_{OUT} = 0V	10	pF

NOTES: 2719 tbl 03

1. With output deselected. ($\overline{OE}$ = high)
2. Characterized values, not currently tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CCC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Votage Commercial	2.0	—	—	V
V_{IH}	Input High Votage Military	2.2	—	—	V
V_{IL}(1)	Input Low Voltage Com'l. and Mil.	—	—	0.8	V

NOTE: 2719 tbl 04

1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5.0V ± 10%, T_A = -55°C + 125°C)

Symbol	Parameter	IDT72215A IDT72225A Commercial t_{CLK} = 20, 25, 50 ns			IDT72215A IDT72225A Military t_{CLK} = 25, 30, 50 ns			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{LI}(1)	Input Leakage Current (any input)	–1	—	1	–10	—	10	µA
I_{LO}(2)	Output Leakage Current	–10	—	10	–10	—	10	µA
V_{OH}	Output Logic "1" Voltage, I_{OH} = –2 mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage, I_{OL} = 8 mA	—	—	0.4	—	—	0.4	V
I_{CC1}(3)	Active Power Supply Current	—	—	250	—	—	300	mA
I_{CC2}(3)	Average Standby Current (All Input = V_{CC} – 0.2V, except RCLK and WCLK which are free-running)	—	—	60	—	—	75	mA

NOTES: 2917 tbl 05

1. Measurements with 0.4 ≤ V_{IN} ≤ V_{OUT}.
2. $\overline{OE}$ ≥ V_{IH}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
3. Tested at f = 20 MHz.

AC ELECTRICAL CHARACTERISTICS

(Commercial: Vcc = 5.0V ± 10%, TA = 0°C to +70°C; Military: Vcc = 5.0V ± 10%, TA = -55°C + 125°C)

Symbol	Parameter	Com'l. IDT72215L20 IDT72225L20		Com'l. & Mil. IDT72215L25 IDT72225L25		Mil. IDT72215L30 IDT72225L30		Com'l. & Mil. IDT72215L50 IDT72225L50		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
fS	Clock Cycle Frequency	—	50	—	40	—	33	—	20	MHz
tA	Data Access Time	2	14	3	15	3	18	3	25	ns
tCLK	Clock Cycle Time	20	—	25	—	30	—	50	—	ns
tCLKH	Clock High Time	8	—	10	—	12	—	20	—	ns
tCLKL	Clock Low Time	9	—	10	—	12	—	20	—	ns
tDS	Data Set-up Time	5	—	6	—	7	—	10	—	ns
tDH	Data Hold Time	1	—	1	—	1	—	2	—	ns
tENS	Enable Set-up Time	5	—	6	—	7	—	10	—	ns
tENH	Enable Hold Time	1	—	1	—	1	—	2	—	ns
tRS	Reset Pulse Width (1)	20	—	25	—	30	—	50	—	ns
tRSS	Reset Set-up Time (2)	12	—	15	—	18	—	30	—	ns
tRSF	Reset to Flag and Output Time	—	20	—	25	—	30	—	50	ns
tOLZ	Output Enable to Output in Low Z (2)	0	—	0	—	0	—	0	—	ns
tOE	Output Enable to Output Valid	—	9	—	12	—	15	—	20	ns
tOHZ	Output Enable to Output in High Z (2)	1	9	1	12	1	15	1	20	ns
tWFF	Write Clock to Full Flag	—	14	—	16	—	18	—	30	ns
tREF	Read Clock to Empty Flag	—	12	—	15	—	18	—	30	ns
tPAF	Clock to Programmable Almost-Full Flag	—	20	—	22	—	24	—	35	ns
tPAE	Clock to Programmable Almost-Empty Flag	—	20	—	22	—	24	—	35	ns
tHF	Clock to Half-Full Flag	—	20	—	22	—	24	—	35	ns
tXO	Clock to Expansion Out	—	12	—	15	—	18	—	30	ns
tXI	Expansion In Pulse Width	8	—	10	—	12	—	20	—	ns
tXIS	Expansion In Set-Up Time	8	—	10	—	12	—	20	—	ns
tSKEW1	Skew time between Read Clock & Write Clock for Full Flag	14	—	16	—	18	—	20	—	ns
tSKEW2	Skew time between Read Clock & Write Clock for Empty Flag	14	—	16	—	18	—	20	—	ns

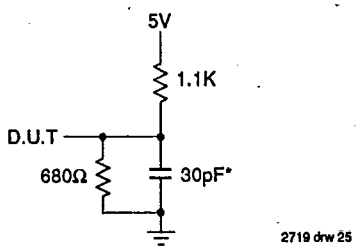
NOTES:
1. Pulse widths less than minimum values are not allowed.
2. Values guaranteed by design, not currently tested.

2719 tbl 08

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2719 tbl 07



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or equivalent circuit

Figure 1. Output Load

*Includes jig and scope capacitances.

SIGNAL DESCRIPTIONS:

INPUTS:

DATA IN (D_0 - D_{17})
Data inputs for 18-bit wide data.

CONTROLS:

RESET ($\overline{RS}$)
Reset is accomplished whenever the Reset ($\overline{RS}$) input is taken to a low state. During reset, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. The Full Flag ($\overline{FF}$), Half-Full Flag ($\overline{HF}$), and Programmable Almost-Full Flag ($\overline{PAF}$) will be reset to high after t_{RSF}. The Empty Flag ($\overline{EF}$) and Programmable Almost-Empty Flag ($\overline{PAE}$) will be reset to low after t_{RSF}.

WRITE CLOCK (WCLK)
A write cycle is initiated on the low-to-high transition of the write clock (WCLK). Data set-up and hold times must be met with respect to the low-to-high transition of the write clock (WCLK).

The write and read clocks can be asynchronous or coincident.

WRITE ENABLE ($\overline{WEN}$)
When Write Enable ($\overline{WEN}$) is low, data can be loaded into the input register and RAM array on the low-to-high transition of every write clock (WCLK). Data is stored in the RAM array sequentially and independently of any on-going read operation.

When Write Enable ($\overline{WEN}$) is high, the input register holds the previous data and no new data is loaded into the FIFO.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go low, inhibiting further write operations. Upon the completion of a valid read cycle, the Full Flag ($\overline{FF}$) will go high after t_{WFF} allowing a write to begin. Write Enable ($\overline{WEN}$) is ignored when the FIFO is full.

READ CLOCK (RCLK)
Data can be read on the outputs on the low-to-high transition of the read clock (RCLK), when Output Enable ($\overline{OE}$) is set low.

The write and read clocks can be asynchronous or coincident.

READ ENABLE ($\overline{REN}$)
When Read Enable ($\overline{REN}$) is low, data is loaded into the RAM array to the output register on the low-to-high transition of the read clock (RCLK).

When Read Enable ($\overline{REN}$) is high, the output register holds the previous data and no new data is loaded into the register.

When all the data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go low, inhibiting further read operations. Once a write is performed, the Empty Flag ($\overline{EF}$) will go high after t_{REF} and a read can begin. Read Enable ($\overline{REN}$) is ignored when the FIFO is empty.

OUTPUT ENABLE ($\overline{OE}$)
When Output Enable ($\overline{OE}$) is enabled (low), the parallel output buffers receive data from the output register. When Output Enable ($\overline{OE}$) is disabled (high), the Q output data bus is in a high impedance state.

LOAD ($\overline{LD}$)
The IDT72215A and IDT72225A devices contain two 16-bit offset registers and a 6-bit depth register which can be loaded with data on the inputs, or read on the outputs. When the Load ($\overline{LD}$) pin is set low and $\overline{WEN}$ is set low, data on the inputs D0-D15 is written into the Empty offset register on the first low-to-high transition of the write clock (WCLK). When the Load ($\overline{LD}$) pin and Write Enable ($\overline{WEN}$) are held low then data is written into the Full offset register on the second low-to-high transition of the write clock (WCLK) and into the Depth register on the third transition. The fourth transition of the write clock (WCLK) again writes to the Empty offset register.

However, writing all offset registers does not have to occur at one time. One or two offset registers can be written and then by bringing the Load ($\overline{LD}$) pin high, the FIFO is returned to normal read/write operation. When the Load ($\overline{LD}$) pin is set low, and Write Enable ($\overline{WEN}$) is low, the next offset register in sequence is written.

When the Load pin is low and Write Enable is high, the offset register counter increments without writing into the offset registers.

The contents of the offset registers can be read on the output lines when the Load ($\overline{LD}$) pin is set low and $\overline{REN}$ is set low. Data can be read on the low-to-high transition of the read clock (RCLK) when $\overline{REN}$ is enabled (low).

A read and a write should not be performed simultaneously to the offset registers.

$\overline{LD}$	$\overline{WEN}$	WCLK[1]	SELECTION
0	0	↑	WRITING TO OFFSET REGISTERS: EMPTY OFFSET FULL OFFSET DEPTH REGISTER
0	1	↑	INCREMENTING OFFSET REGISTER COUNTER BUT NOT WRITING: EMPTY OFFSET FULL OFFSET DEPTH REGISTER
1	0	↑	WRITE INTO FIFO
1	1	↑	NO OPERATION

NOTE: 2719 drw 04
1. The same selection sequence applies to reading from the registers. $\overline{REN}$ is enabled and read is performed on the low-to-high transition of RCLK.

Figure 2. Write Offset Register

FIRST LOAD ($\overline{FL}$)

First Load ($\overline{FL}$) is grounded to indicate operation in the Single Device or Width Expansion mode. In the Depth Expansion configuration, First Load ($\overline{FL}$) is grounded to indicate it is the first device loaded and is set to high for all other devices in the daisy chain. (See Operating Configurations for further details.)

WRITE EXPANSION INPUT ($\overline{WXI}$)

This is a dual purpose pin. Write Expansion In ($\overline{WXI}$) is grounded to indicate operation in the Single Device or Width Expansion mode. Write Expansion In ($\overline{WXI}$) is connected to Write Expansion Out ($\overline{WXO}$) of the previous device in the Depth Expansion or Daisy Chain mode.

READ EXPANSION INPUT ($\overline{RXI}$)

This is a dual purpose pin. Read Expansion In ($\overline{RXI}$) is grounded to indicate operation in the Single Device or Width Expansion mode. Read Expansion In ($\overline{RXI}$) is connected to Read Expansion Out ($\overline{RXO}$) of the previous device in the Depth Expansion or Daisy Chain mode.

OUTPUTS:

FULL FLAG ($\overline{FF}$)

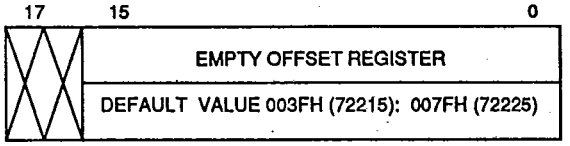
The Full Flag ($\overline{FF}$) will go low, inhibiting further write operation, indicating that the device is full. If no reads are performed after Reset ($\overline{RS}$), the Full Flag ($\overline{FF}$) will go low after 512 writes for the IDT72215SA and 1024 writes for the IDT72225A.

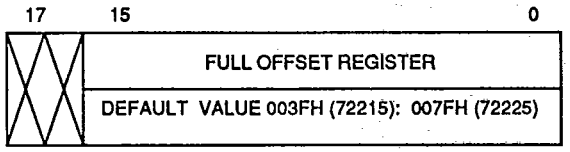
The Full Flag ($\overline{FF}$) is updated on the low-to-high transition of the write clock (WCLK).

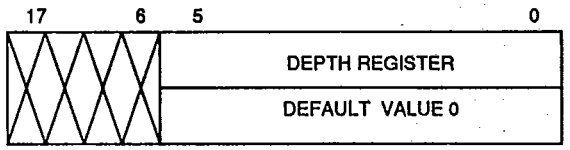
EMPTY FLAG ($\overline{EF}$)

The Empty Flag ($\overline{EF}$) will go low, inhibiting further read operations, when the read pointer is equal to the write pointer, indicating the device is empty.

The Empty Flag ($\overline{EF}$) is updated on the low-to-high transition the read clock (RCLK).







NOTE: 2719 drw 24
1. Any bits of the offset register not being programmed should be set to zero.

Figure 3. Offset Register Location and Default Values

IDT72215A		IDT72225A	
Data Loaded In Depth Register	Total Depth In Expansion Configuration	Data Loaded In Depth Register	Total Depth In Expansion Configuration
0 or 1	512	0 or 1	1024
2	1024	2	2048
3	1536	3	3072
4	2048	4	4096
5	2560	5	5120
6	3072	6	6144
•	•	•	•
•	•	•	•
•	•	•	•
32	16384	32	32768

Figure 4. Depth Register Programming

TABLE I — STATUS FLAGS

Number of Words In FIFO						
72215A	72225A	$\overline{FF}$	$\overline{PAF}$	$\overline{HF}$	$\overline{PAE}$	$\overline{EF}$
0	0	H	H	H	L	L
1 to n[1]	1 to n[1]	H	H	H	L	H
(n+1) to 257	(n+1) to 513	H	H	H	H	H
258 to (512-(m+1))	514 to (1024-(m+1))	H	H	L	H	H
(512-m) [2] to 511	(1024-m) [2] to 1023	H	L	L	H	H
512	1024	L	L	L	H	H

NOTES:
1. n = Empty Offset (Default Values : 72215A n = 63 : 72225A n = 127)
2. m = Full Offset (Default Values : 72215A m = 63 : 72225A m = 127)

2917 tbl 08

PROGRAMMABLE ALMOST-FULL FLAG ($\overline{PAF}$)

The Programmable Almost-Full Flag ($\overline{PAF}$) will go low when FIFO reaches the Almost-Full condition. If no reads are performed after Reset ($\overline{RS}$), the Programmable Almost Full Flag ($\overline{PA}$) will go low after (512–m) writes for the IDT72215A and (1024–m) writes for the IDT72225A. The offset "m" is defined in the FULL offset register.

If there is no Full offset specified, the Programmable Almost-Full Flag ($\overline{PAF}$) will be low when the device is 7/8 full to completely full.

The Programmable Almost-Full Flag ($\overline{PAF}$) is asserted low on the low-to-high transition of the write clock (WCLK). $\overline{PAF}$ is reset to high on the low-to-high transition of the read clock (RCLK). Thus the $\overline{PAF}$ is asychronous.

PROGRAMMABLE ALMOST-EMPTY FLAG ($\overline{PAE}$)

The Programmable Almost-Empty Flag ($\overline{PAE}$) will go low when the read pointer is "n+1" locations less than the write pointer. The offset "n" is defined in the EMPTY offset register.

If there is no Empty offset specified, the Programmable Almost Empty Flag ($\overline{PAE}$) will be low when the device is completely empty to 1/8 full.

The Programmable Almost-Empty Flag ($\overline{PAE}$) is asserted low on the low-to-high transition of the read clock (RCLK). $\overline{PAE}$ is reset to high on the low-to-high transition of the write clock (WCLK). Thus the $\overline{PAF}$ is asychronous.

WRITE EXPANSION OUT/HALF-FULL FLAG ($\overline{WXO}/\overline{HF}$)

This is a dual-purpose output. In the Single Device and Width Expansion mode, when Write Expansion In ($\overline{WXI}$) is grounded, this output acts as an indication of a half-full memory.

After half of the memory is filled, and at the low-to-high transition of the next write cycle, the Half-Full Flag goes low and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset to high by the low-to-high transition of the read clock (RCLK). The $\overline{HF}$ is asychronous.

In the Depth Expansion or Daisy Chain mode, Write Expansion In ($\overline{WXI}$) is connected to Write Expansion Out ($\overline{WXO}$) of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse when the previous device write to the last location of memory.

READ EXPANSION OUT ($\overline{RXO}$)

In the Depth Expansion or Daisy Chain configuration, Read Expansion In ($\overline{RXI}$) is connected to Read Expansion Out ($\overline{RXO}$) of the previous device. This output acts as a signal to the next device in the Daisy Chain by providing a pulse when the previous device reads from the last location of memory.

DATA OUTPUTS (Q_0-Q_{17})

Q_0-Q_{17} are data outputs for 18-bit wide data.

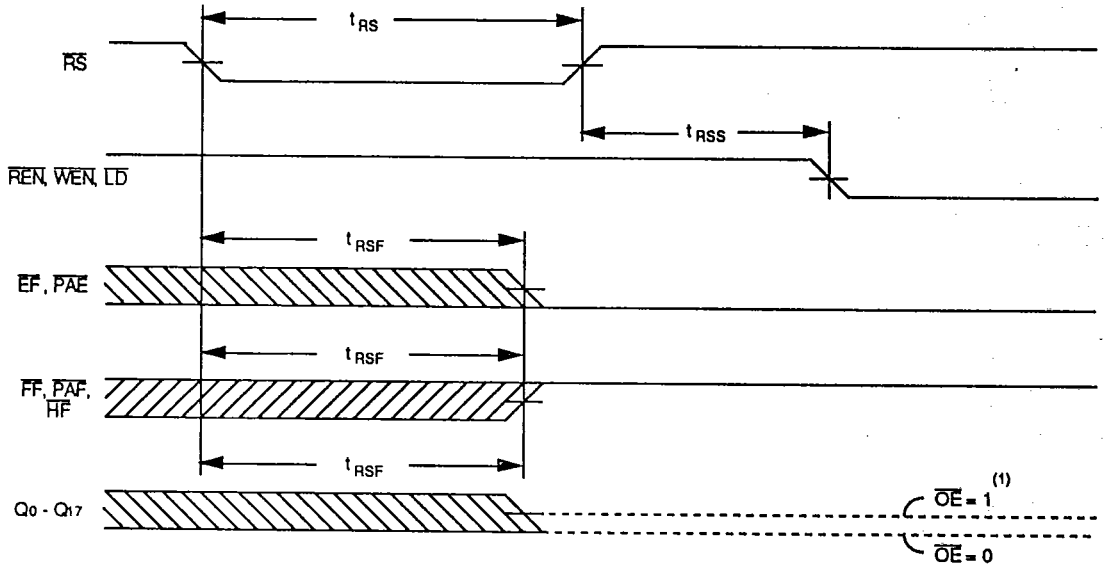


Figure 5. Reset Timing[2]

NOTE:
1. After reset, the outputs will be low if $\overline{OE}$ = 0 and tri-state if $\overline{OE}$ = 1.
2. The clocks (RCLK, WCLK) can be free-running during reset.

6

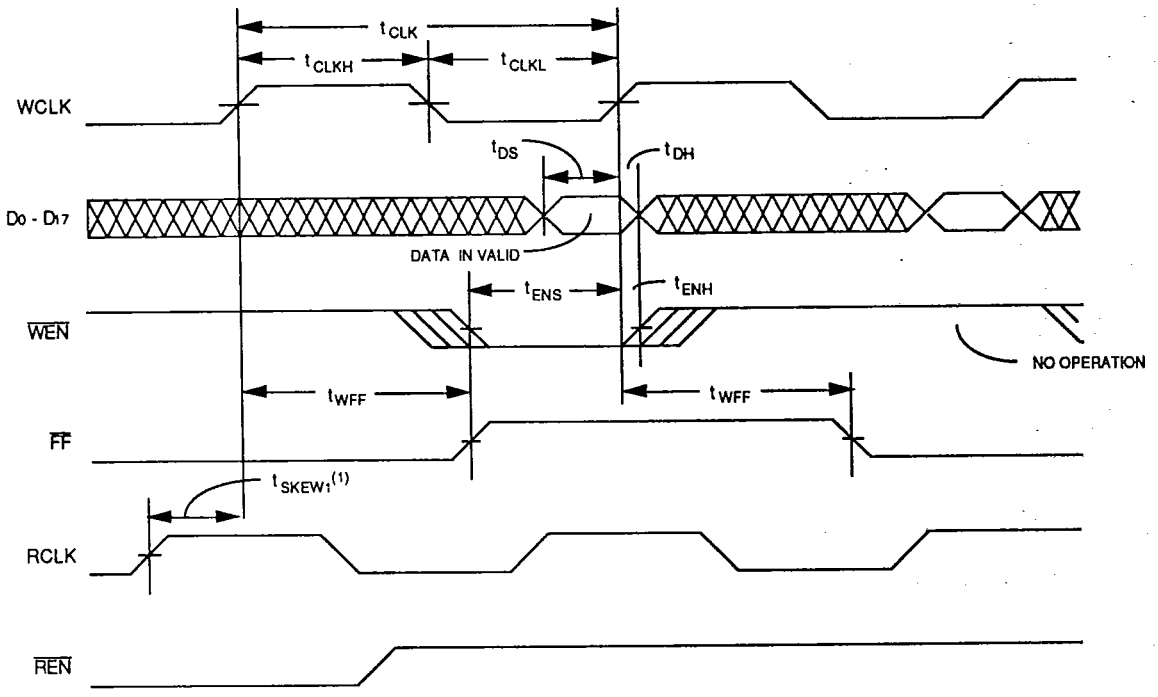


Figure 6. Write Cycle Timing

NOTE:
1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{FF}$ to change during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then $\overline{FF}$ may not change state until the next WCLK edge.

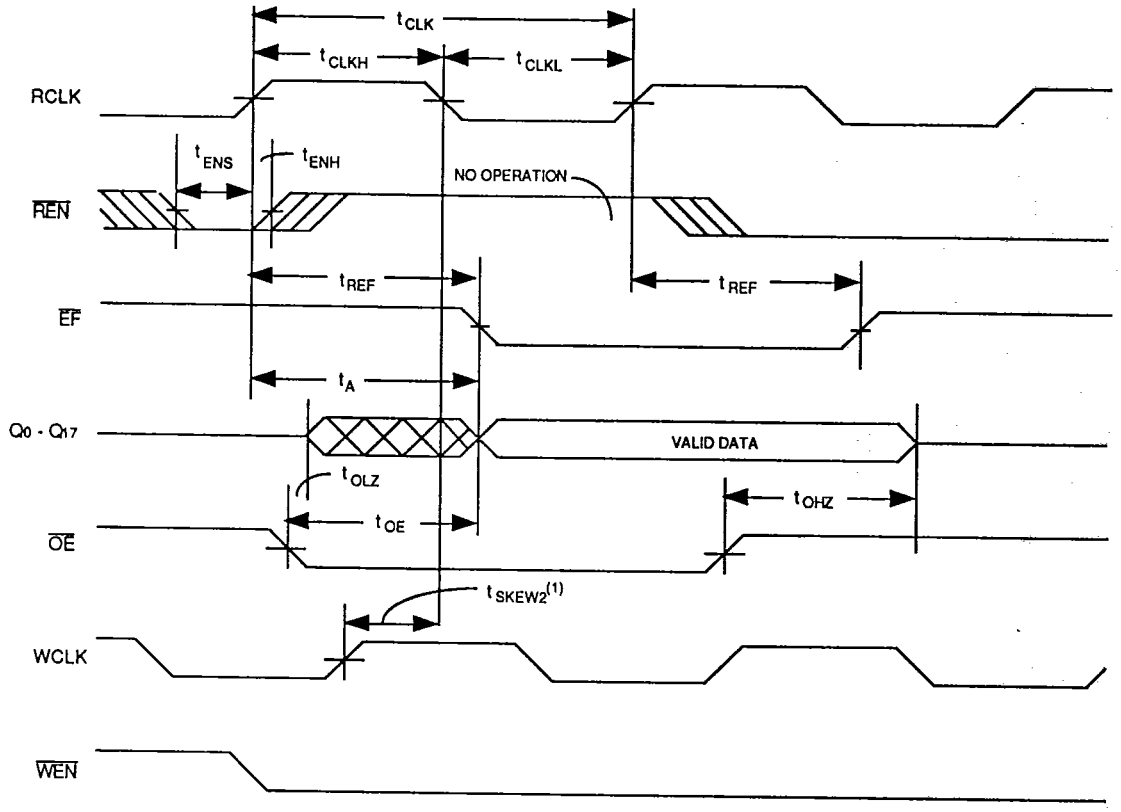


Figure 7. Read Cycle Timing

6

NOTE:

1. t_{SKEW2} is the minimum time between a rising WCLK edge and a falling RCLK edge for $\overline{EF}$ to change during the current clock cycle. If the time between the rising edge of WCLK and the falling edge of RCLK is less than t_{SKEW2}, then $\overline{EF}$ may not change state until the next RCLK edge.

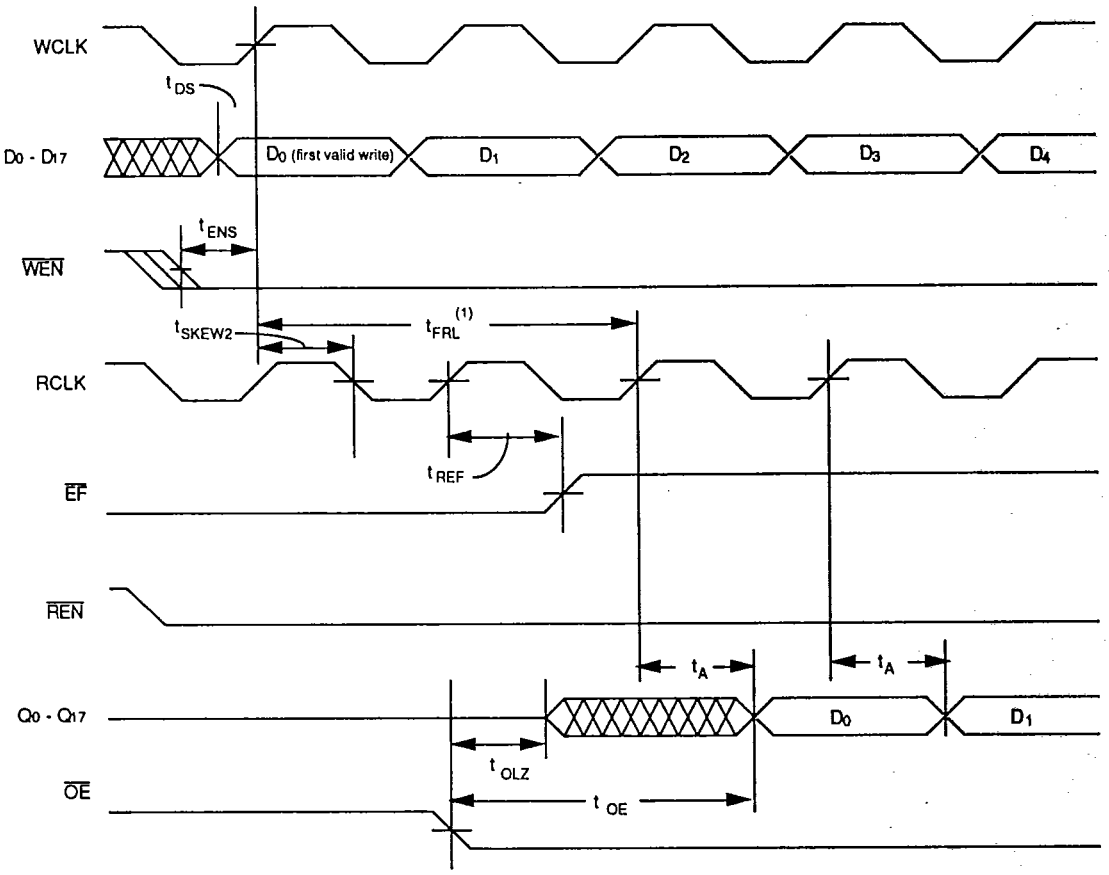


Figure 8. First Data Word Latency after Reset with Simultaneous Read and Write

NOTE:
1. When $t_{SKEW2} \geq$ minimum specification, t_{FRL} (maximum) = 1.5 * t_{CLK} + t_{SKEW2}. t_{SKEW2} < minimum specification, t_{FRL} (maximum) = 2.5 * t_{CLK} + t_{SKEW2}. The Latency Timing apply only at the Empty Boundary ($\overline{EF}$ = LOW).

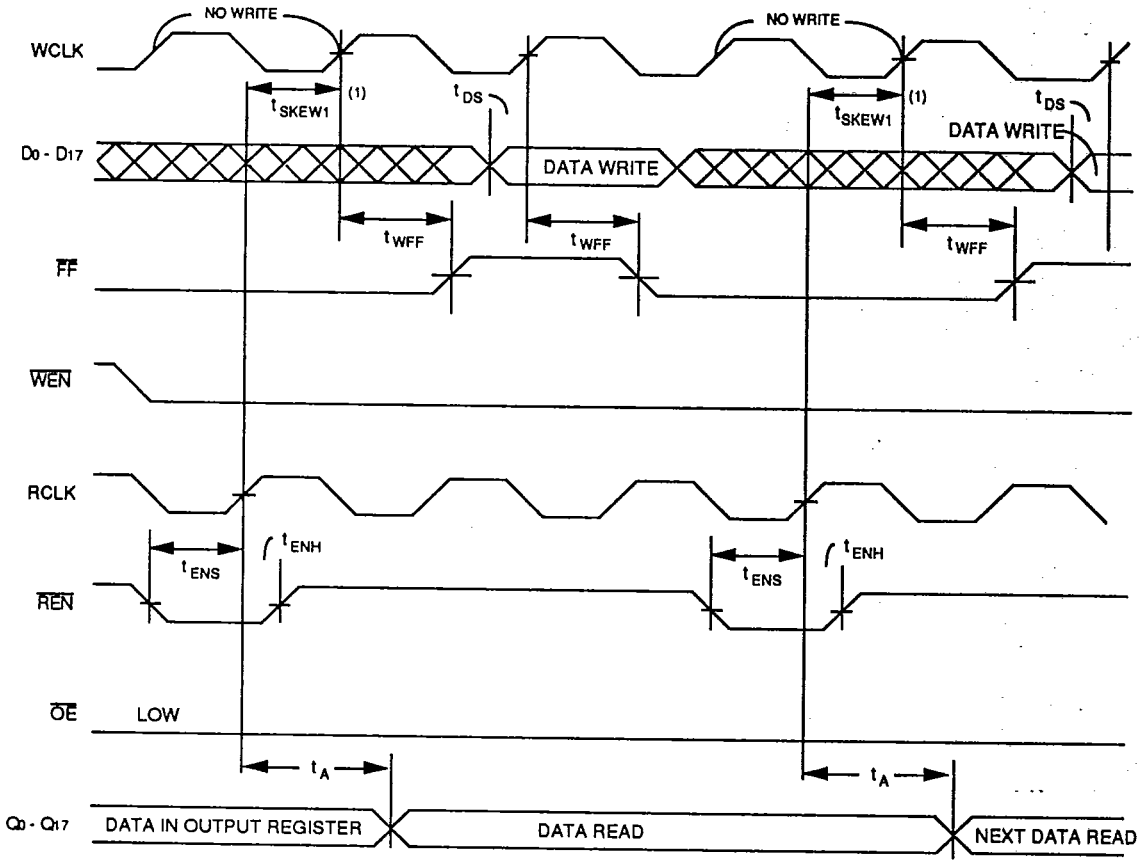


Figure 9. Full Flag Timing

NOTE:

1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{FF}$ to change during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then $\overline{FF}$ may not change state until the next WCLK edge.

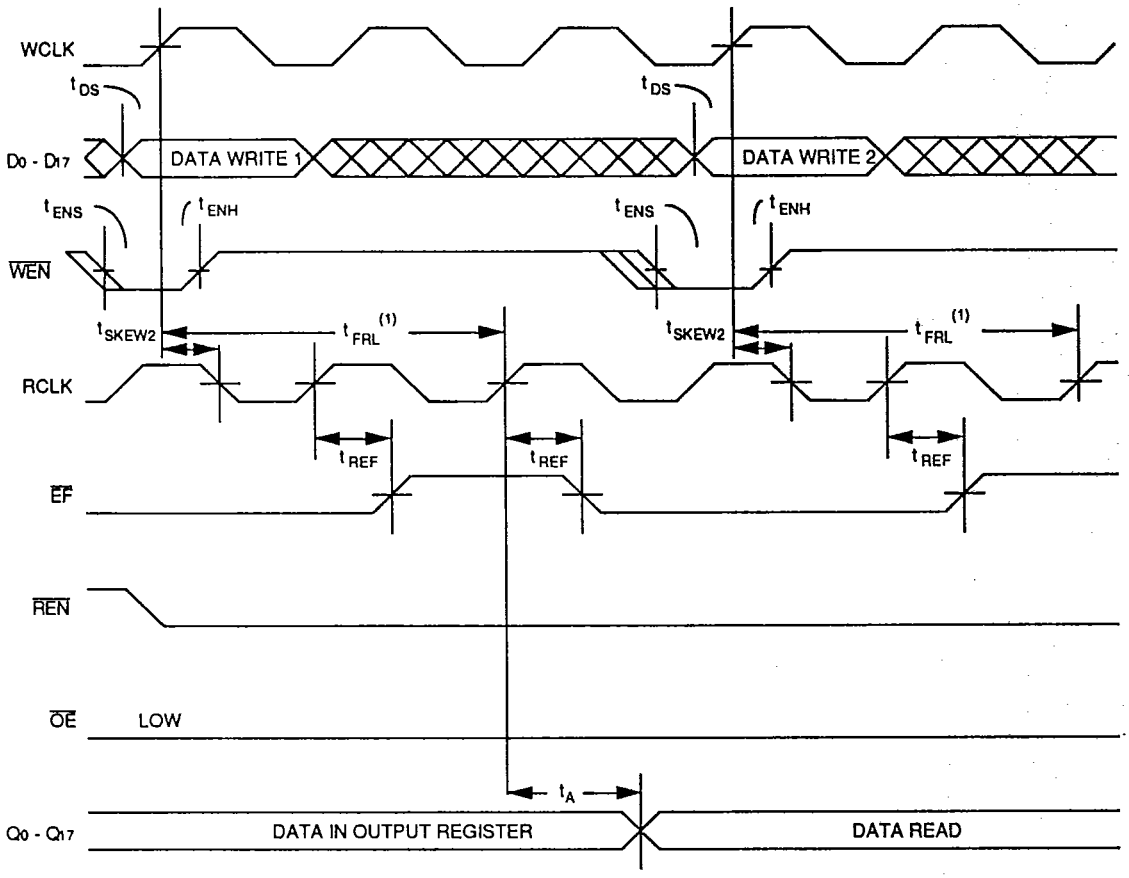


Figure 10. Empty Flag Timing

NOTE:
1. When $t_{SKEW2} \geq$ minimum specification, t_{FRL} (maximum) = 1.5 * t_{CLK} + t_{SKEW2}. t_{SKEW2} < minimum specification, t_{FRL} (maximum) = 2.5 * t_{CLK} + t_{SKEW2}. The Latency Timing apply only at the Empty Boundary ($\overline{EF}$ = LOW).

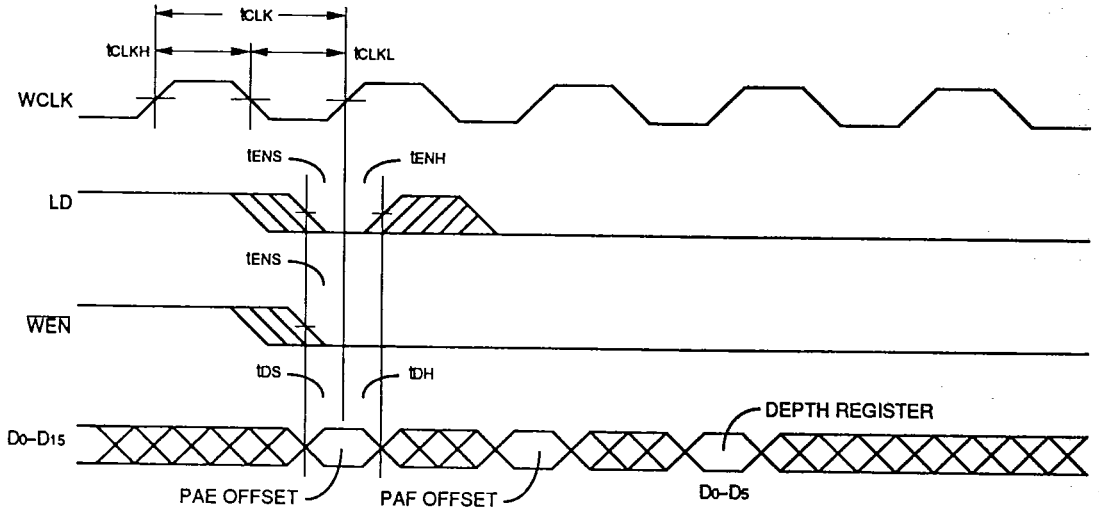


Figure 11. Write Programmable Registers

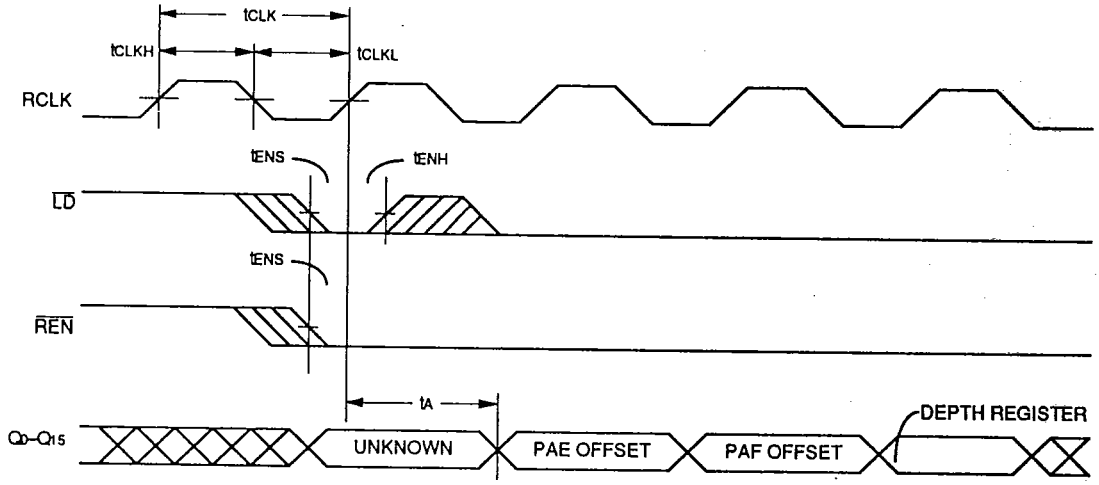


Figure 12. Read Programmable Registers

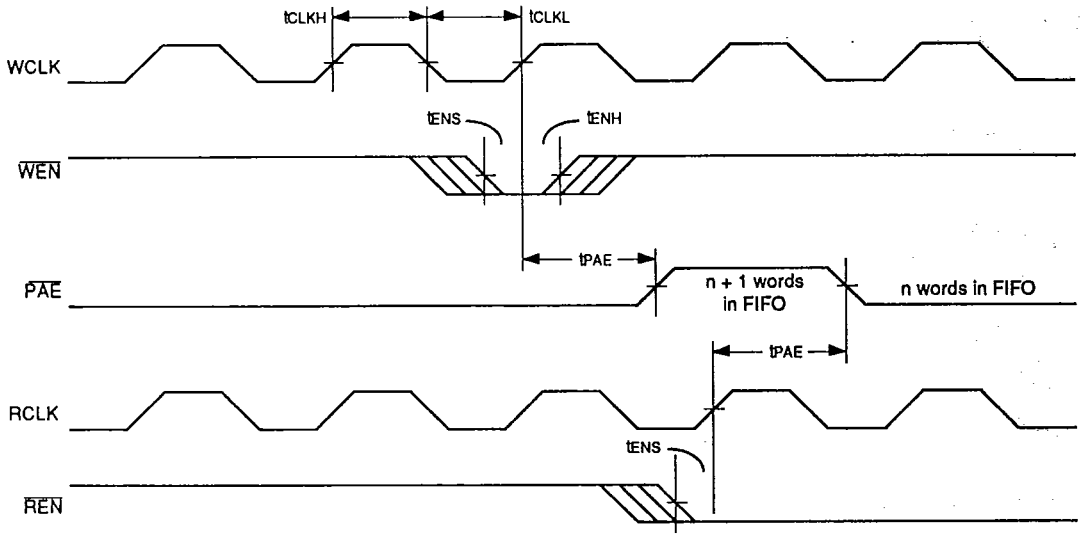


Figure 13. Programmable Almost Empty Flag Timing

NOTE:
1. PAE is offset = n. Number of data words written into FIFO already = n.

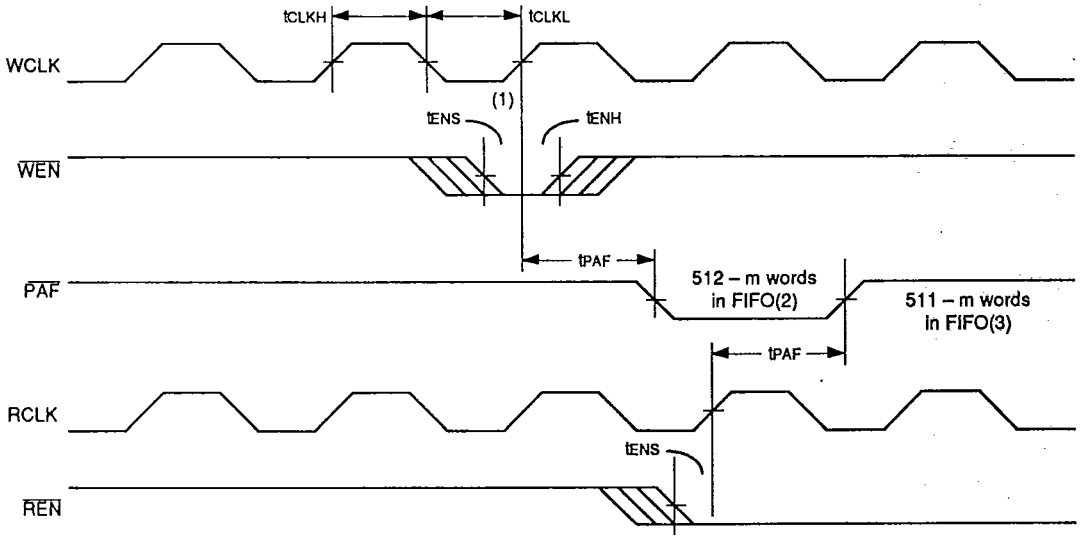


Figure 14. Programmable Almost-Full Flag Timing

NOTES:
1. PAF offset = m. Number of data words written into FIFO already = 511 – m for the IDT72215A and 1023 – m for the IDT72225A.
2. 512 – m words in FIFO for IDT72215A. 1024 – m word in FIFO for IDT72225A.
3. 511 – m words in FIFO for IDT72215A. 1023 – m word in FIFO for IDT72225A.

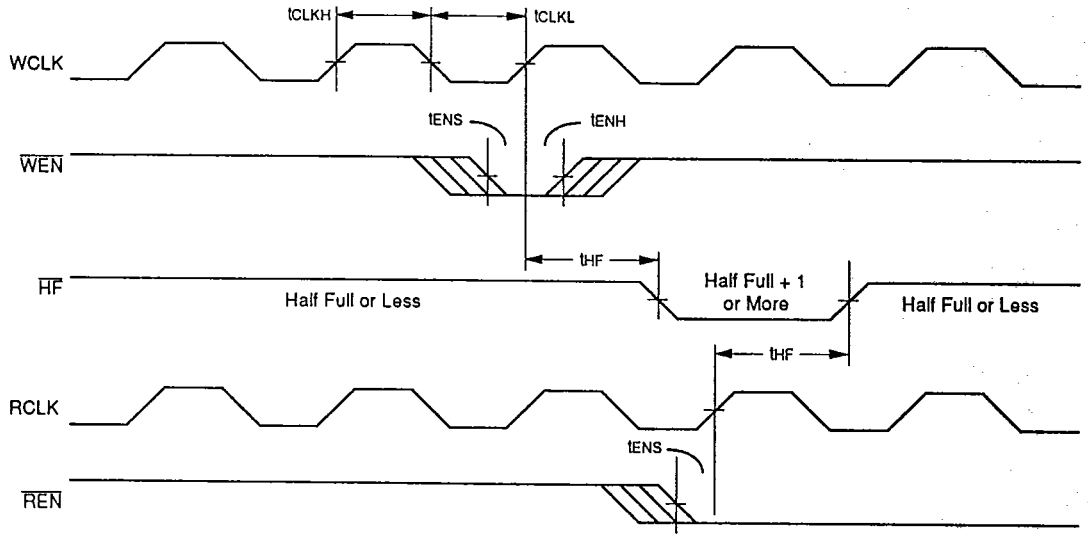


Figure 15. Half-Full Flag Timing

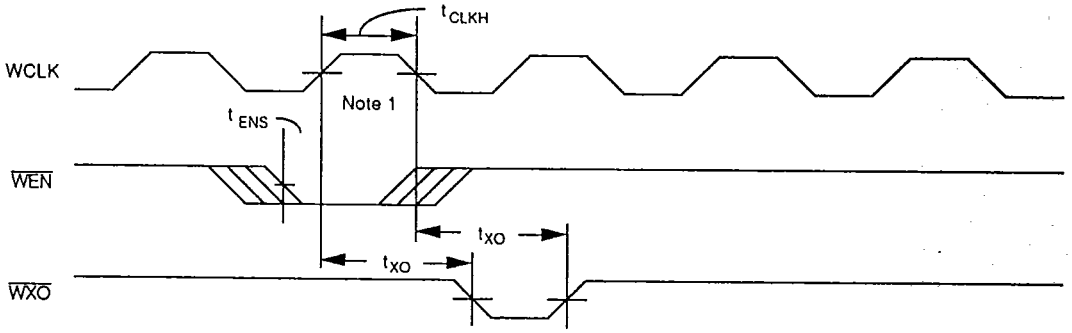


Figure 16. Write Expansion Out Timing

NOTE:
1. Write to Last Physical Location.

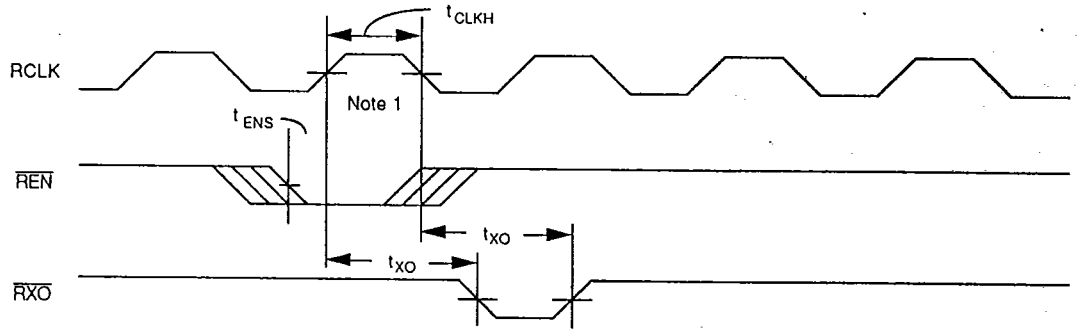


Figure 17. Read Expansion Out Timing

NOTE:
1. Read from Last Physical Location.

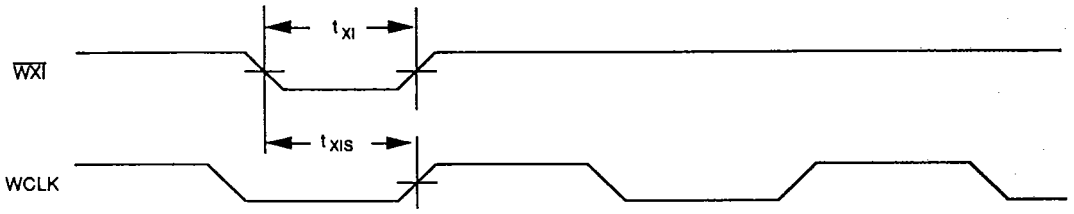


Figure 18. Write Expansion In Timing

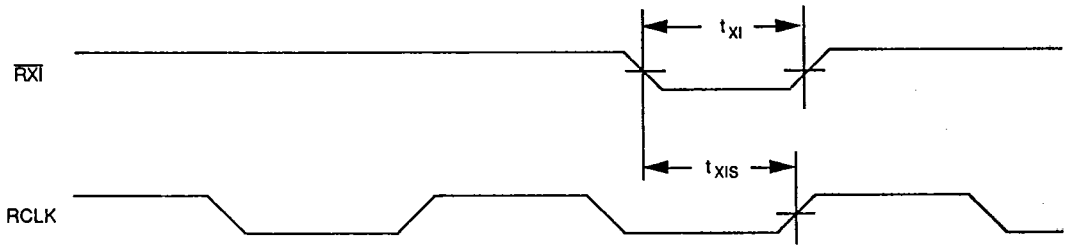


Figure 19. Read Expansion In Timing

OPERATING CONFIGURATIONS

SINGLE DEVICE CONFIGURATION

A single IDT72215A/72225A may be used when the application requirements are for 512/1024 words or less. The IDT72215A/72225A are in a single Device Configuration when the Write Exansion In ($\overline{WXI}$), Read Expansion In ($\overline{RXI}$), and First Load ($\overline{FL}$) control inputs are grounded . (See Figure 20.)

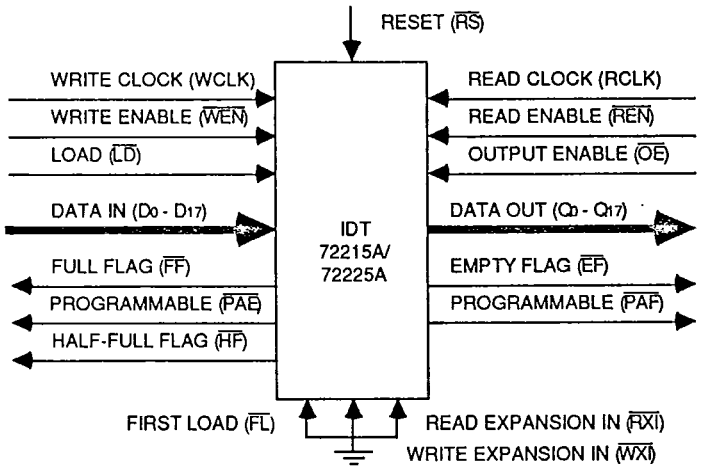
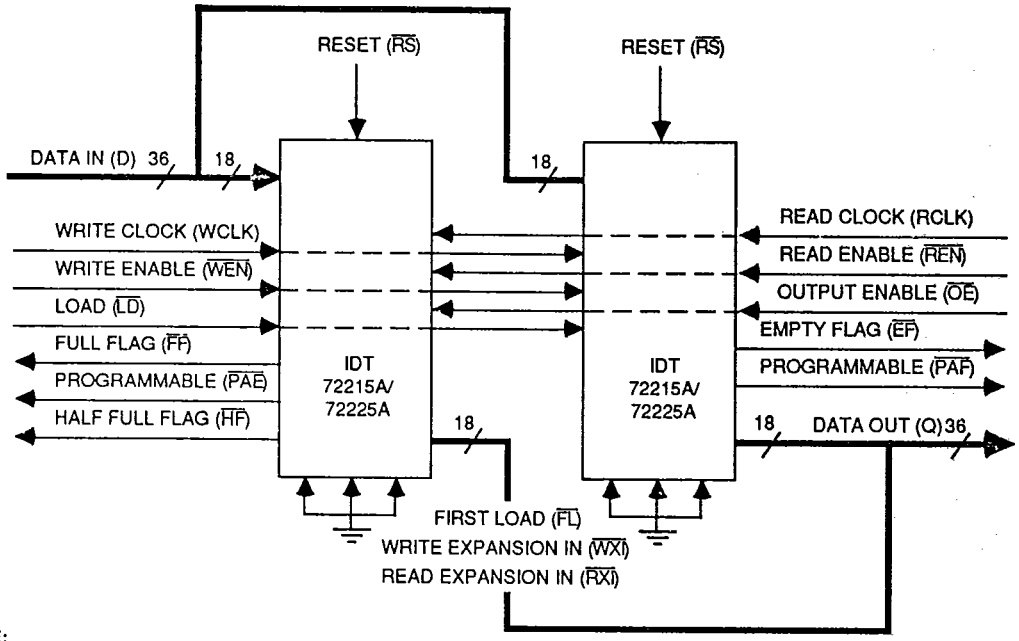


Figure 20. Block Diagram of Single 512 x 18/1024 x 18 Synchronous FIFO

WIDTH EXPANSION CONFIGURATION

Word width may be increased simply by connecting the corresponding control signals of multiple devices. Status flags ($\overline{EF}$, $\overline{PAE}$, $\overline{HF}$, $\overline{PAF}$, and $\overline{FF}$) can be detected from any one device. Figure 21 demonstrates a 36-word width by using two IDT72215A.72225As. Any word width can be attained by adding additional IDT72215A/72225As.



NOTE:
1. Flag detection is accomplished by monitoring the flag signals on either (any) device used in width expansion configuration. Do not connect any output control signals together.

Figure 21. Block Diagram of 512 x 36/1024 x 36 Synchronous FIFO Memory Used in a a Width Expansion Configuration

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DEPTH EXPANSION CONFIGURATION (WITH PROGRAMMABLE FLAGS)

The IDT72215A/72225A can easily be adapted to applications when the requirements are for greater than 512/1024 words. Figure 22 demonstrates Depth Expansion using three IDT72215A/72225As. Any depth up to 32768 can be attained by adding IDT72225As. The IDT72215A/72225A operates in the Depth Expansion configuration with programmable flags when the following conditions are met:

1. The first device must be designated by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the high state.
3. The Write Expansion Out ($\overline{WXO}$) pin of each device must be tied to the Write Expansion In ($\overline{WXI}$) pin of the next device. See Figure 20.
4. The Read Expansion Out ($\overline{RXO}$) pin of each device must be tied to the Read Expansion In ($\overline{RXI}$) pin of the next device. See Figure 20.
5. To permit programmable flags, the first component controls the flags, and the flags are ignored on all other components. The total depth of the configuration is programmed in the master device by loading the total number of FIFOs into the depth register.
6. All Load ($\overline{LD}$) pins are tied together.
7. The Half-Full Flag ($\overline{HF}$) is not available in the Depth Expansion Configuration.

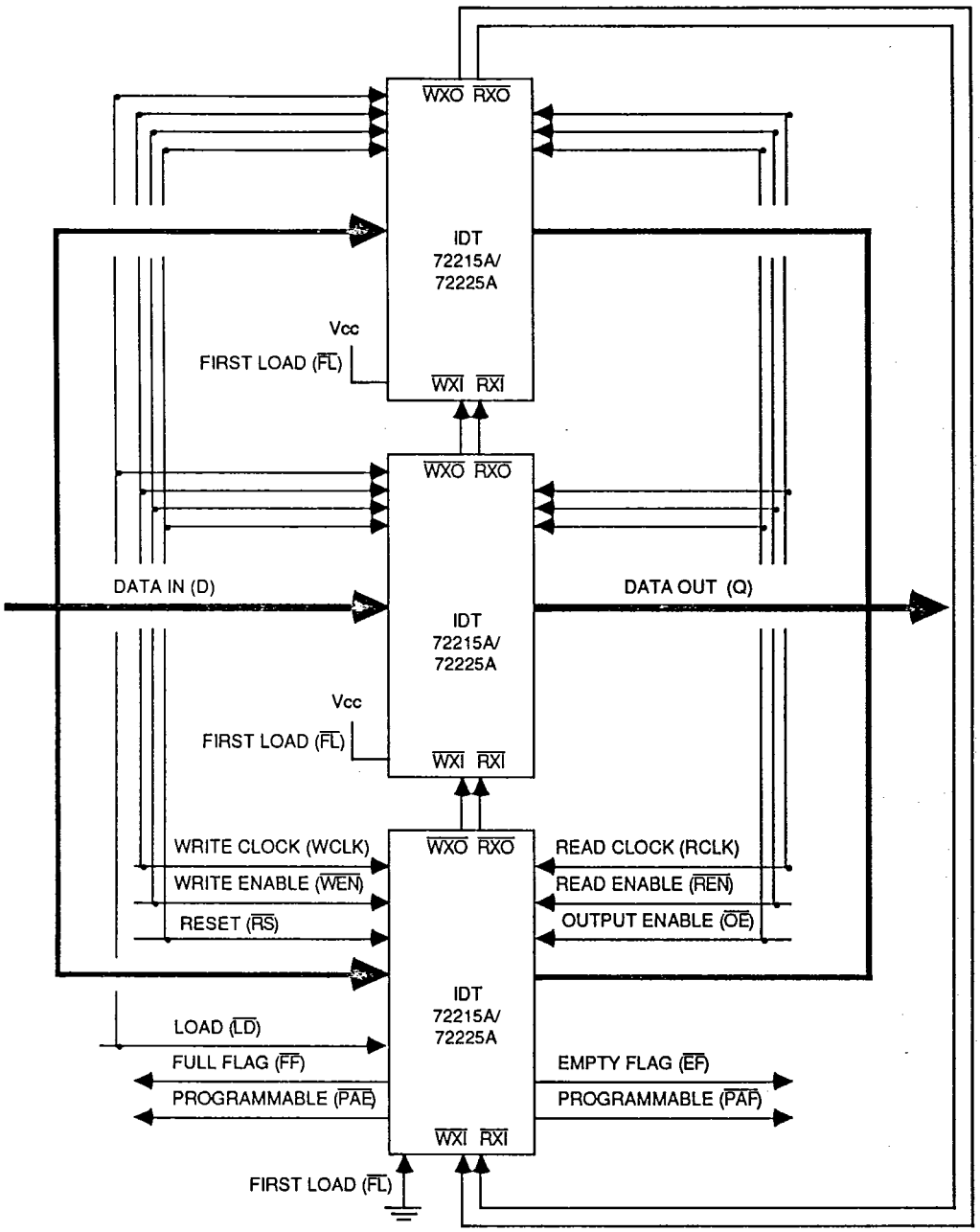
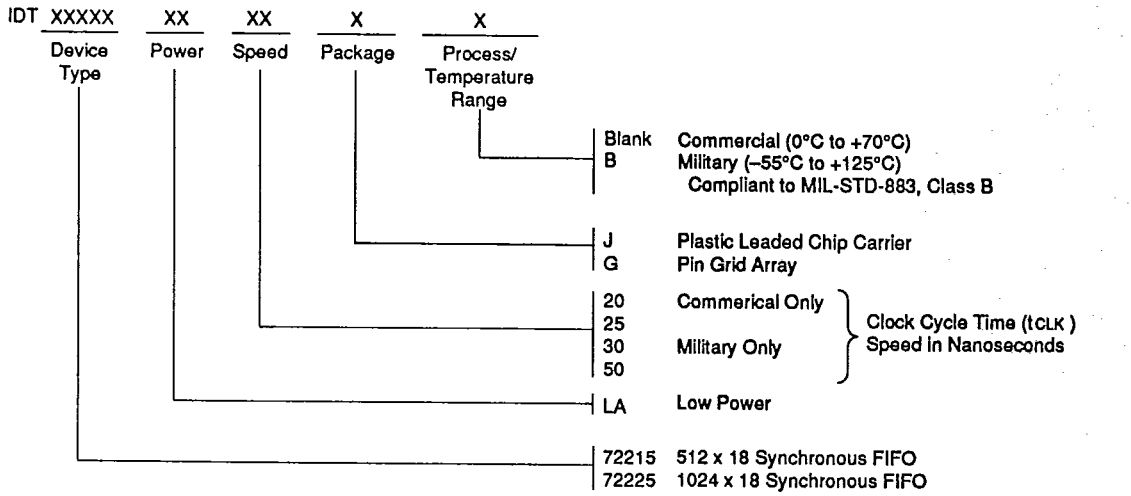


Figure 22. Block Diagram of 1536 x 18/3072 x 18 Synchronous FIFO Memory With Programmable Flags used in Depth Expansion Configuration

ORDERING INFORMATION



2719 drw 23

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