Integrated Device Technology, Inc.

CMOS PARALLEL SyncFIFO™ (CLOCKED FIFO) 512 x 18-BIT & 1024 x 18-BIT

IDT72215L
IDT72225L

T-46-35

FEATURES

- 512 x 18-bit and 1024 x 18-bit memory array structures
- 20ns read / write cycle time
- Easily expandable in width
- Read and write clocks can be independent or coincident
- Dual-port zero fall-through time architecture
- Programmable almost-empty and almost-full flags
- Empty and Full flags signal FIFO status
- Half-Full flag capability in a single device configuration
- Output enable puts output data bus in high impedance state
- Produced with advanced submicron CEMOS™ technology
- Available in a 68-lead flatpack (FP), pin grid array (PGA), and plastic leaded chip carrier (PLCC)
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION

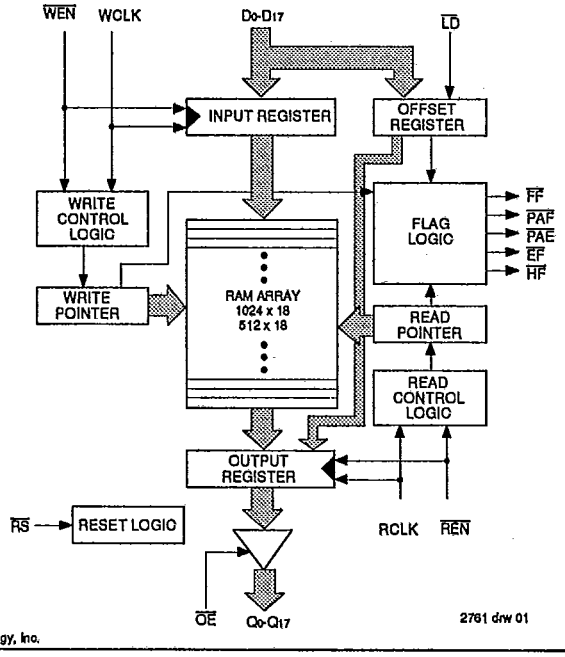
The IDT72215L and IDT72225L are very high speed, low-power first-in, first-out (FIFO) memories with read and write controls. The IDT72215L has a 512 x 18-bit memory array, while the IDT72225L has a 1024 x 18-bit memory array. These FIFOs are applicable for a wide variety of data buffering needs, such as optical disk controllers, local area networks (LANs), and interprocessor communication.

Both FIFOs have 18-bit input and output ports. The input port is controlled by a free-running clock (WCLK) and a data input enable pin ($\overline{WEN}$). Data is written into the Synchronous FIFO on every clock when $\overline{WEN}$ is asserted. The output port is controlled by another clock pin (RCLK) and another enable pin ($\overline{REN}$). The read clock can be tied to the write clock for single clock operation or the two clocks can run independent of one another for dual clock operation. An output enable pin ($\overline{OE}$) is provided on the read port for three-state control of the output.

The Synchronous FIFOs have two fixed flags, Empty ($\overline{EF}$) and Full ($\overline{FF}$), and two programmable flags, Almost-Empty ($\overline{PAE}$) and Almost-Full ($\overline{PAF}$). The loading of the programmable flag offsets can be controlled by a simple state machine and is initiated by asserting the load pin ($\overline{LD}$). A Half-Full flag ($\overline{HF}$) is also available.

The IDT72215L/72225L is fabricated using IDT's high speed submicron CEMOS™ technology. Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B.

FUNCTIONAL BLOCK DIAGRAM



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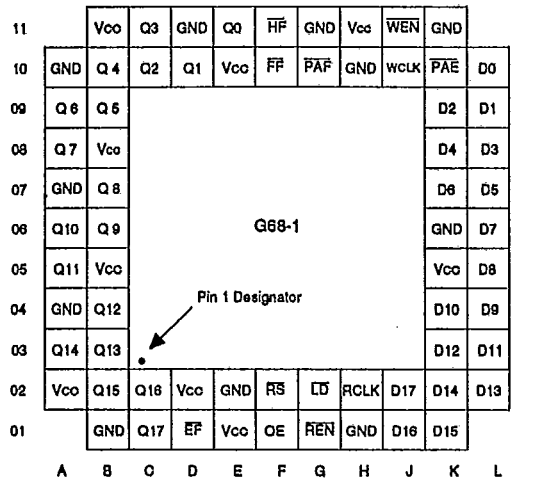
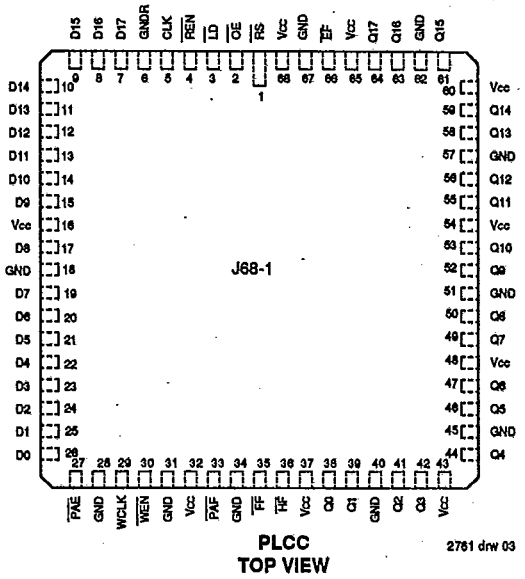
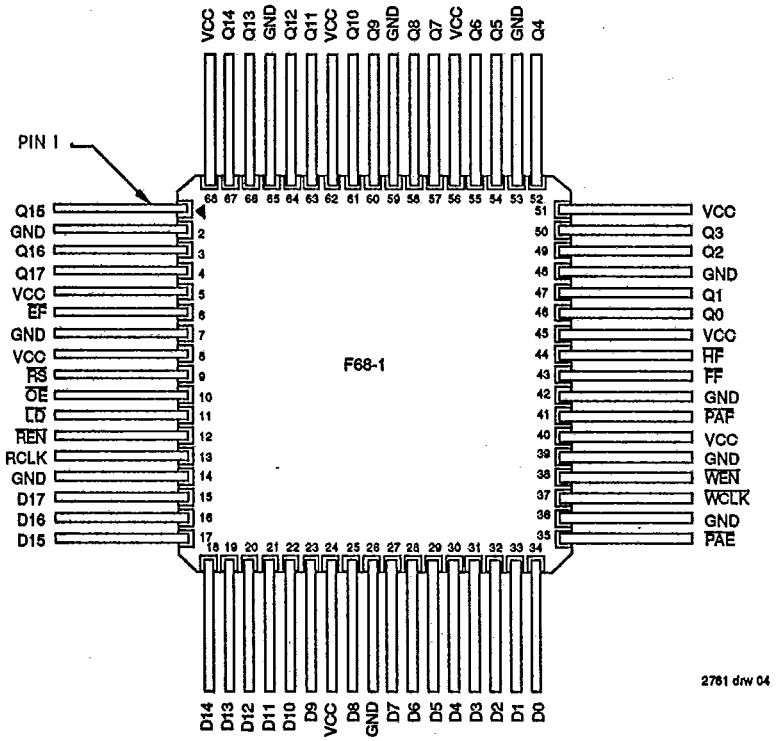
PIN CONFIGURATIONS







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PIN DESCRIPTIONS

SYMBOL	NAME	I/O	DESCRIPTION
D0 - D17	Inputs	I	Data inputs for 18-bit wide data.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is set low, internal read and write pointers are set to the first location of the RAM array. $\overline{FF}$ and $\overline{PAF}$ go high, and $\overline{PAE}$ and $\overline{EF}$ go low. A reset is required before an initial WRITE after power-up.
WCLK	Write Clock	I	When $\overline{WEN}$ is low, a write cycle is initiated on the low-to-high transition of the write clock WCLK, if the FIFO is not full.
$\overline{WEN}$	Write Enable	I	When $\overline{WEN}$ is low, data can be loaded into the FIFO on the low-to-high transition of every WCLK clock. When the FIFO is full ($\overline{FF}$ - low), the internal WRITE operation is blocked.
RCLK	Read Clock	I	When $\overline{REN}$ is enabled (low), data can be read on the outputs on the low-to-high transition of the read clock RCLK, if the FIFO is not empty.
$\overline{REN}$	Read Enable	I	When $\overline{REN}$ is low, data can be read from the FIFO on the low-to-high transition of every RCLK clock. When $\overline{REN}$ is high, the output register holds the previous data. When the FIFO is empty ($\overline{EF}$-low), the internal READ operation is blocked.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is enabled (low), the parallel output buffers receive data from the output register. When $\overline{OE}$ is disabled (high), the Q output bus is in a high impedance state.
$\overline{LD}$	Load	I	When $\overline{LD}$ is low, data on the inputs D0-D15 is written to the offset registers on the low-to-high transition of the WCLK.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ goes low, the device is full and further WRITE operations are inhibited. When $\overline{FF}$ is high, the device is not full. $\overline{FF}$ is synchronized with WCLK.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ goes low, the device is empty and further READ operations are inhibited. When $\overline{EF}$ is high, the device is not empty. $\overline{EF}$ is synchronized with RCLK.
$\overline{PAF}$	Programmable Almost Full Flag	O	When $\overline{PAF}$ is low, the device is almost full based on the programmable full offset. If there is no offset specified, the default value is 63 for 72215, and 127 for 72225.
$\overline{PAE}$	Programmable Almost Empty Flag	O	When $\overline{PAE}$ is low, the device is almost empty based on the programmable empty offset. If there is no offset specified, the default value is 63 for 72215, and 127 for 72225.
$\overline{HF}$	Half-Full Flag	O	The device is more than half full when $\overline{HF}$ is low.
Q0-Q17	Outputs	O	Data outputs for 18-bit wide data.
Vcc	Power Supply		Nine +5 V power supply pins.
GND	Ground		Eleven Ground pins.

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ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +135	°C
I_{OUT}	DC Output Current	50	50	mA

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NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CCM}	Military Supply Voltage	4.5	5.0	5.5	V
V_{CCC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage Commercial	2.0	—	—	V
V_{IH}	Input High Voltage Military	2.2	—	—	V
V_{IL}(1)	Input Low Voltage Commercial & Military	—	—	0.8	V

NOTE:
1. 1.5V undershoots are allowed for 10ns once per cycle.

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DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C; Military: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C)

Symbol	Parameter	IDT72215L/72225L Commercial t_{CLK} = 20, 25, 35, 50ns Min.	Typ.	Max.	IDT72215L/72225L Military t_{CLK} = 25, 35, 50ns Min.	Typ.	Max.	Unit
I_{LI}(1)	Input Leakage Current (Any Input)	-1	—	-1	-10	—	10	µA
I_{LO}(2)	Output Leakage Current	-10	—	10	-10	—	10	µA
V_{OH}	Output Logic "1" Voltage, I_{OH} = -2 mA	2.4	—	—	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage, I_{OL} = 8 mA	—	—	0.4	—	—	0.4	V
I_{CC1}(3)	Active Power Supply Current	—	—	250	—	—	250	mA
I_{CC2}(3)	Average Standby Current (All inputs = V_{CC} - 0.2V, except RCLK and WCLK which are free running)	—	—	70	—	—	85	mA

NOTES:
1. Measurements with 0.4 ≤ V_{IN} ≤ V_{CC}.
2. $\overline{OE}$ ≥ V_{IH}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
3. Tested at f = 20MHz with outputs open.

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CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}(1)	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}(1,2)	Output Capacitance	V_{OUT} = 0V	10	pF

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NOTES:
1. Characterized values, not currently tested.
2. With output deselected, ($\overline{OE}$ = high).

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AC ELECTRICAL CHARACTERISTICS[1]

(Commercial: Vcc = 5V ± 10%, TA = 0°C to + 70°C; Military: Vcc = 5V ± 10%, TA = -55°C to +125°C)

Symbol	Parameter	Com'l. 72215L/25L20 Min.	Com'l. 72215L/25L20 Max.	Commercial & Military 72215L/25L25 Min.	72215L/25L25 Max.	72215L/25L35 Min.	72215L/25L35 Max.	72215L/25L50 Min.	72215L/25L50 Max.	Unit
fS	Clock Cycle Frequency	—	50	—	40	—	28.6	—	20	MHz
tA	Data Access Time	—	13	—	15	—	20	—	25	ns
tCLK	Clock Cycle Time	20	—	25	—	35	—	50	—	ns
tCLKH	Clock High Time	8	—	10	—	14	—	20	—	ns
tCLKL	Clock Low Time	10	—	10	—	14	—	20	—	ns
tDS	Data Set-up Time	7	—	8	—	10	—	10	—	ns
tDH	Data Hold Time[1]	1	—	1	—	2	—	2	—	ns
tENS	Enable Set-up Time	7	—	9	—	11	—	12	—	ns
tENH	Enable Hold Time	1	—	1	—	2	—	2	—	ns
tRS	Reset Pulse Width	20	—	25	—	35	—	50	—	ns
tRSS	Reset Set-up Time	12	—	15	—	20	—	30	—	ns
tRSR	Reset Recovery Time	15	—	20	—	25	—	35	—	ns
tRSF	Reset to Flag and Output Time	—	20	—	25	—	35	—	50	ns
tOLZ	Output Enable to Output in Low Z[3]	0	—	0	—	0	—	0	—	ns
tOE	Output Enable to Output Valid	—	9	—	12	—	17	—	20	ns
tOHZ	Output Enable to Output in High Z[3]	1	9	1	12	1	17	1	20	ns
tWFF	Write Clock to Full Flag	—	14	—	16	—	20	—	30	ns
tREF	Read Clock to Empty Flag	—	12	—	15	—	20	—	30	ns
tPAE	Clock to Programmable Almost-Empty Flag	—	20	—	22	—	30	—	35	ns
tPAF	Clock to Programmable Almost-Full Flag	—	20	—	22	—	30	—	35	ns
tHF	Clock to Half-Full Flag	—	20	—	22	—	30	—	35	ns
tSKW1	Skew time between Read Clock & Write Clock for Full Flag	14	—	16	—	18	—	20	—	ns
tSKW1	Skew time between Read Clock & Write Clock for Empty Flag	14	—	16	—	18	—	20	—	ns

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NOTES:
1. Allow an additional two (2) ns hold time when programming the offset registers.
2. Pulse widths less than minimum values are not allowed.
3. Values guaranteed by design, not 100% tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

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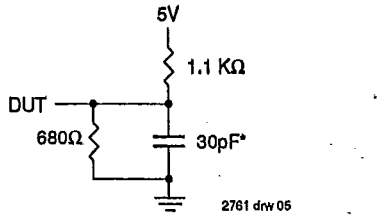

Figure 1. Output Load

* Includes jig and scope capacitances.

SIGNAL DESCRIPTIONS:

Inputs

DATA IN (D0 - D17)

Data inputs for 18-bit wide data.

Controls:

RESET ($\overline{RS}$)

Reset is accomplished whenever the Reset ($\overline{RS}$) input is taken to a low state. During reset, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. The Full Flag ($\overline{FF}$), Half-Full Flag ($\overline{HF}$), and Programmable Almost Full Flag ($\overline{PAF}$) will be reset to high after tRSF. The Empty Flag ($\overline{EF}$) and Programmable Almost Empty Flag ($\overline{PAE}$) will be reset to low after tRSF.

WRITE CLOCK (WCLK)

A write cycle is initiated on the low-to-high transition of the write clock (WCLK) if $\overline{WEN}$ is low. Data set-up and hold times must be met in respect to the low-to-high transition of the write clock (WCLK).

WRITE ENABLE ($\overline{WEN}$)

When Write Enable ($\overline{WEN}$) is low, data can be loaded into the input register and RAM array on the low-to-high transition of every write clock (WCLK). Data is stored in the RAM array sequentially and independently of any on-going read operation.

When Write Enable ($\overline{WEN}$) is high, the input register holds the previous data and no new data is allowed to be loaded into the register.

To prevent data overflow, the Full Flag ($\overline{FF}$) will go low, inhibiting further write operations. Upon the completion of a valid read cycle, the Full Flag ($\overline{FF}$) will go high after tWFF, allowing a write to begin. Write Enable ($\overline{WEN}$) is ignored when the FIFO is full.

READ CLOCK (RCLK)

Data can be read on the outputs on the low-to-high transition of the read clock (RCLK) if $\overline{REN}$ is low.

READ ENABLE ($\overline{REN}$)

When Read Enable ($\overline{REN}$) is low, data that has been stored in the output register on the previous read cycle can be read on the outputs on the low-to-high transition of every read clock (RCLK), if Output Enable ($\overline{OE}$) is enabled. At the same time, data is read from the RAM array to the output register on the low-to-high transition of the read clock (RCLK).

When Read Enable ($\overline{REN}$) is high, the output register holds the previous data and no new data is allowed to be loaded into the register.

When all the data has been read from the FIFO, the Empty Flag ($\overline{EF}$) will go low, inhibiting further read operations. Once a write is performed, the Empty Flag ($\overline{EF}$) will go high after t_{REF} and a read can begin. Read Enable ($\overline{REN}$) is ignored when the FIFO is empty.

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OUTPUT ENABLE ($\overline{OE}$)

When Output Enable ($\overline{OE}$) is enabled (low), the parallel output buffers receive data from the output register. When Output Enable ($\overline{OE}$) is disabled (high), the Q output data bus is in a high impedance state.

LOAD ($\overline{LD}$)

The IDT72215L and IDT72225L devices contain two 16-bit offset registers and a 6-bit blank register which can be loaded with data from the data inputs, or read on the data outputs. When the Load ($\overline{LD}$) pin is set low and $\overline{WEN}$ is set low, data on the inputs D0 - D15 is written into the Empty offset register on the first low-to-high transition of the write clock (WCLK). When the Load ($\overline{LD}$) pin and Write Enable ($\overline{WEN}$) are held low then data is written into the Full offset register on the second low-to-high transition of the write clock (WCLK) and into the blank register on the third transition. The blank register must be written with all zeros. The fourth transition of the write clock (WCLK) again writes to the Empty offset register.

However, writing all offset registers does not have to occur at one time. One or two offset registers can be written and then by bringing the Load ($\overline{LD}$) pin high, the FIFO is returned to normal read/write operation. When the Load ($\overline{LD}$) pin is set low, and Write Enable ($\overline{WEN}$) is low, the next offset register in sequence is written.

The contents of the offset registers can be read on the output lines when the Load ($\overline{LD}$) pin is set low and $\overline{REN}$ is set low. Data can be read on the low-to-high transition of the read clock (RCLK), when $\overline{REN}$ is enabled (low).

A read and a write should not be performed simultaneously to the offset registers.

Outputs:

FULL FLAG ($\overline{FF}$)

The Full Flag ($\overline{FF}$) will go low, inhibiting further write operation, indicating that the device is full. If no reads are performed after Reset ($\overline{RS}$), the Full Flag ($\overline{FF}$) will go low after 512 writes for the IDT72215L and 1024 writes for the IDT72225L.

The Full Flag ($\overline{FF}$) is updated on the low-to-high transition of the write clock (WCLK).

EMPTY FLAG ($\overline{EF}$)

The Empty Flag ($\overline{EF}$) will go low, inhibiting further read operations, indicating the device is empty.

The Empty Flag ($\overline{EF}$) is updated on the low-to-high transition of the read clock (RCLK).

PROGRAMMABLE ALMOST FULL FLAG ($\overline{PAF}$)

The Programmable Almost Full Flag ($\overline{PAF}$) will go low when the FIFO reaches the Almost Full condition. If no reads are performed after Reset ($\overline{RS}$), the Programmable Almost Full Flag ($\overline{PAF}$) will go low after (512 - m) writes for the IDT72215L and (1024 - m) writes for the IDT72225L. The offset 'm' is defined in the FULL offset register.

If there is no Full offset specified, the Programmable Almost Full Flag ($\overline{PAF}$) default value is 63 for 72215L, and 127 for 72225L.

The Programmable Almost Full Flag ($\overline{PAF}$) going low is updated on the low-to-high transition of the write clock (WCLK). $\overline{PAF}$ is reset to high on the low-to-high transition of the read clock (RCLK).

PROGRAMMABLE ALMOST EMPTY FLAG ($\overline{PAE}$)

The Programmable Almost Empty Flag ($\overline{PAE}$) will go low when the read pointer is 'n' locations less than the write pointer. The offset 'n' is defined in the EMPTY offset register. If no reads are performed after Reset ($\overline{RS}$), the Programmable Almost Empty Flag ($\overline{PAE}$) will go high after n writes for both the IDT72215L and the IDT72225L. The Programmable Almost Empty Flag ($\overline{PAE}$) will be low when the FIFO is empty up to n writes, if the read pointer is not moved.

If there is no Empty offset specified, the Programmable Almost Empty Flag ($\overline{PAE}$) default value is 63 for 72215L, and 127 for 72225L.

The Programmable Almost Empty Flag ($\overline{PAE}$) going low is updated on the low-to-high transition of the read clock (RCLK). $\overline{PAE}$ is reset to high on the low-to-high transition of the wirte clock (WCLK).

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HALF-FULL FLAG ($\overline{HF}$)

After half of the memory is filled, and at the low-to-high transition of the next write cycle, the Half-Full Flag ($\overline{HF}$) goes low and will remain set until the difference between the write pointer and read pointer is less than or equal to one half of the total memory of the device. The Half-Full Flag ($\overline{HF}$) is then reset to high by the low-to-high transition of the read clock (RCLK).

DATA OUTPUTS (Q0 - Q17)

Q_0 - Q_{17} are data outputs for 18-bit wide data.

$\overline{LD}$	$\overline{WEN}$	WCLK[1]	SELECTION
0	0	↑	WRITING TO OFFSET REGISTERS: EMPTY OFFSET, FULL OFFSET, BLANK REGISTER
0	1	↑	INCREMENTING OFFSET REGISTER COUNTER BUT NOT WRITING: EMPTY OFFSET, FULL OFFSET, BLANK REGISTER
1	0	↑	WRITE INTO FIFO
1	1	↑	NO OPERATION

2761 tbl 08

Figure 2. Write Offset Register

NOTE:
1. The same selection sequence applies to reading from the register. $\overline{REN}$ is enabled and read is performed on the low-to-high transition of RCLK.

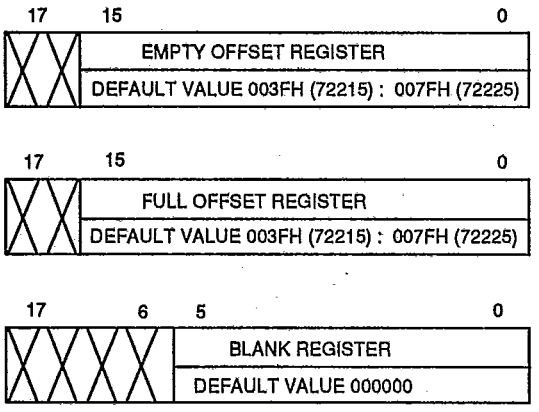

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Figure 3. Offset Register Location and Default Values

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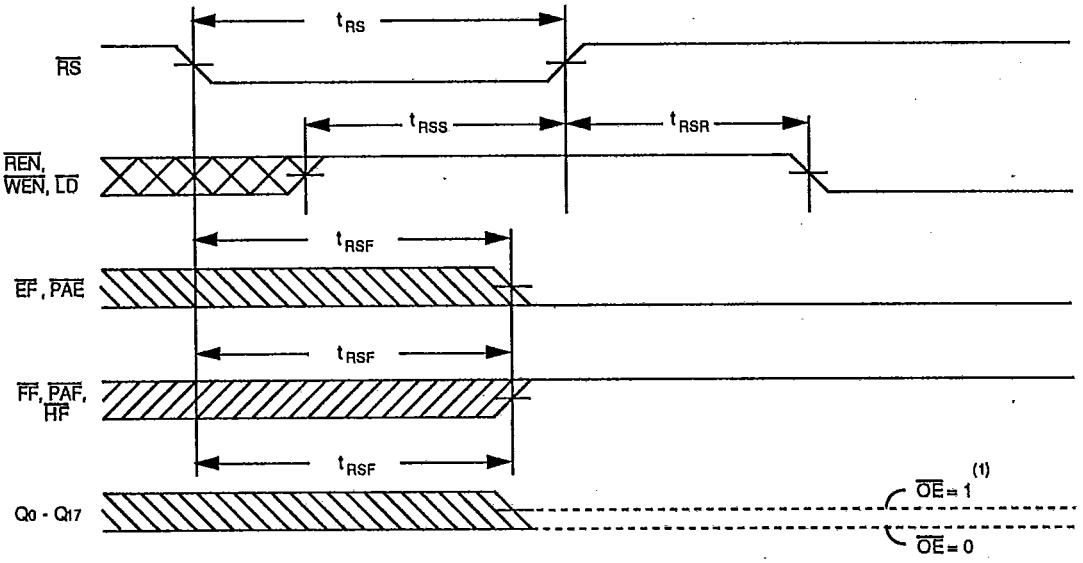

Figure 5. Reset Timing[2]

2761 drw 06

NOTES:
1. After reset, the outputs will be low if $\overline{OE}$ = 0 and tri-state if $\overline{OE}$ = 1.
2. The clocks (RCLK, WCLK) can be free-running during reset.

5

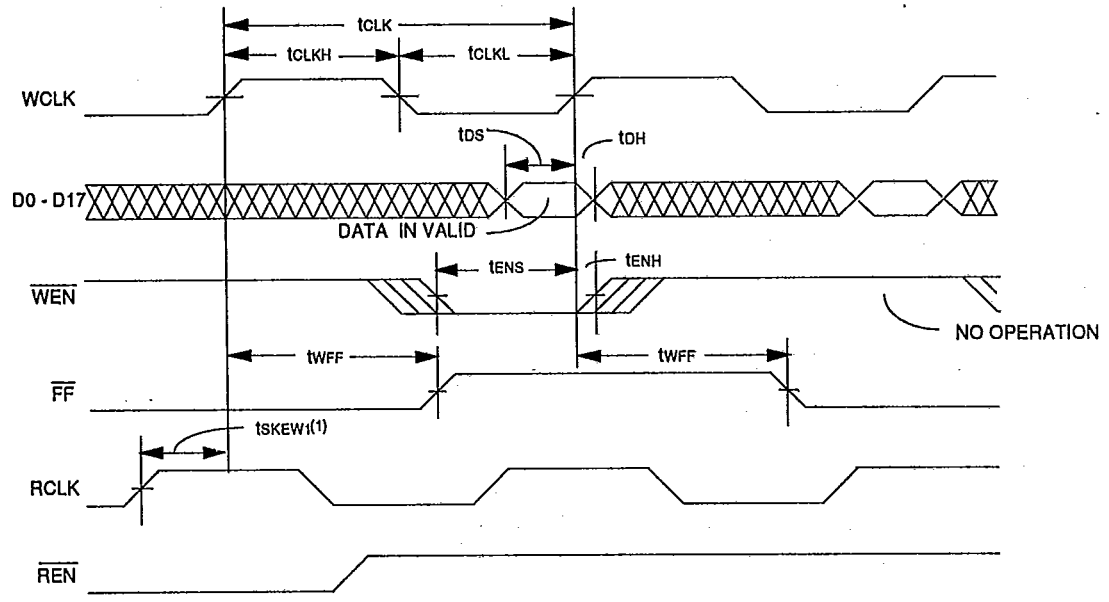

Figure 6. Write Cycle Timing

2761 drw 07

NOTE:
1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee $\overline{FF}$ will go high during the current clock cycle. If the time between therising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then $\overline{FF}$ may not change state until the next WCLK edge.

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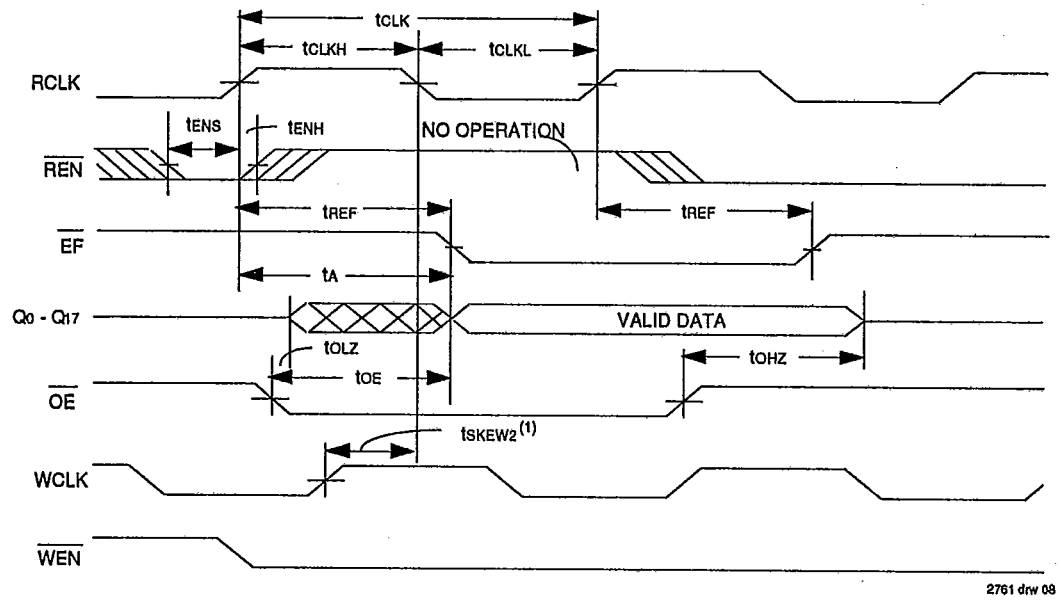

Figure 7. Read Cycle Timing

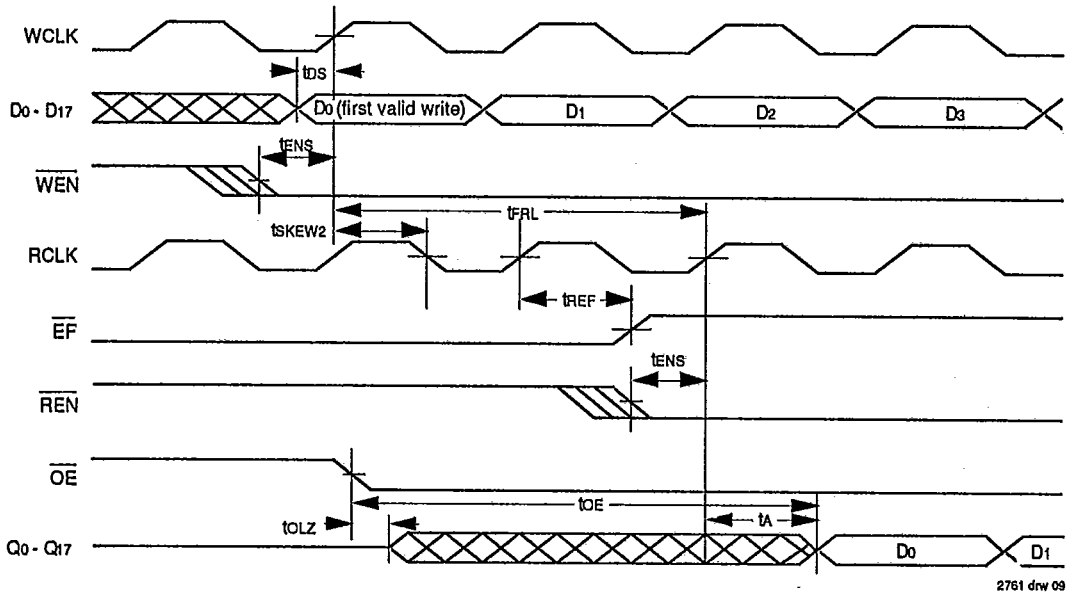

Figure 8. First Data Word Latency after Reset with Simultaneous Read and Write

NOTE:
1. When $t_{SKEW2} \geq$ minimum specification, t_{FRL} (maximum) = 1.5 * t_{CLK} + t_{SKEW2}. When t_{SKEW2} < minimum specification, t_{FRL} (maximum) = either 2.5 * t_{CLK} + t_{SKEW2} or 1.5 * tCLK + t_{SKEW2}. The Latency Timing applies only at the Empty Boundary ($\overline{EF}$ = LOW).

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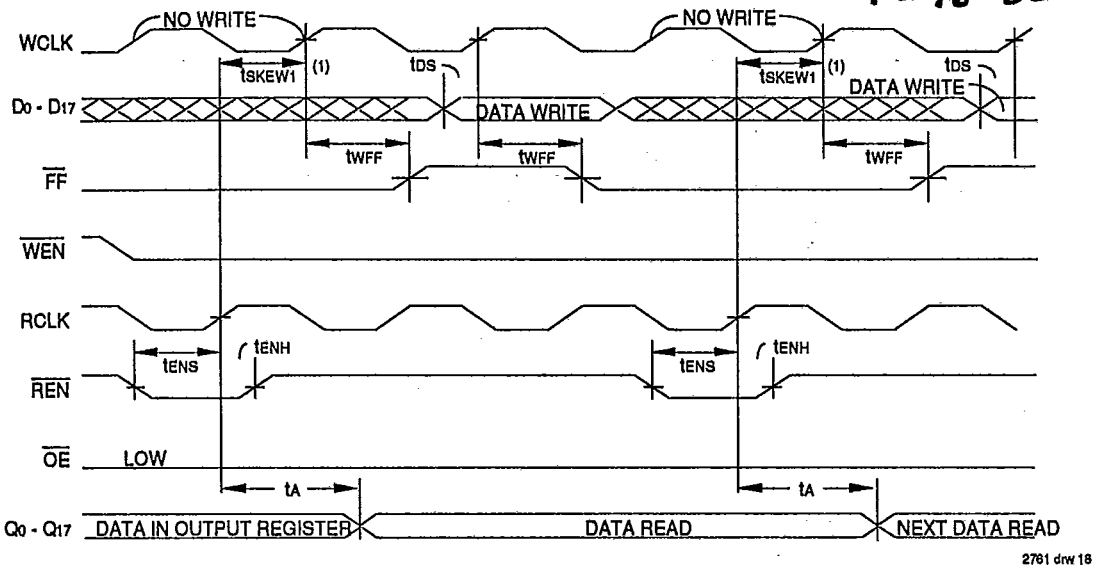

Figure 9. Full Flag Timing

NOTE:
1. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee $\overline{FF}$ will go high during the current clock cycle. If the time between therising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then $\overline{FF}$ may not change state until the next WCLK edge.

5

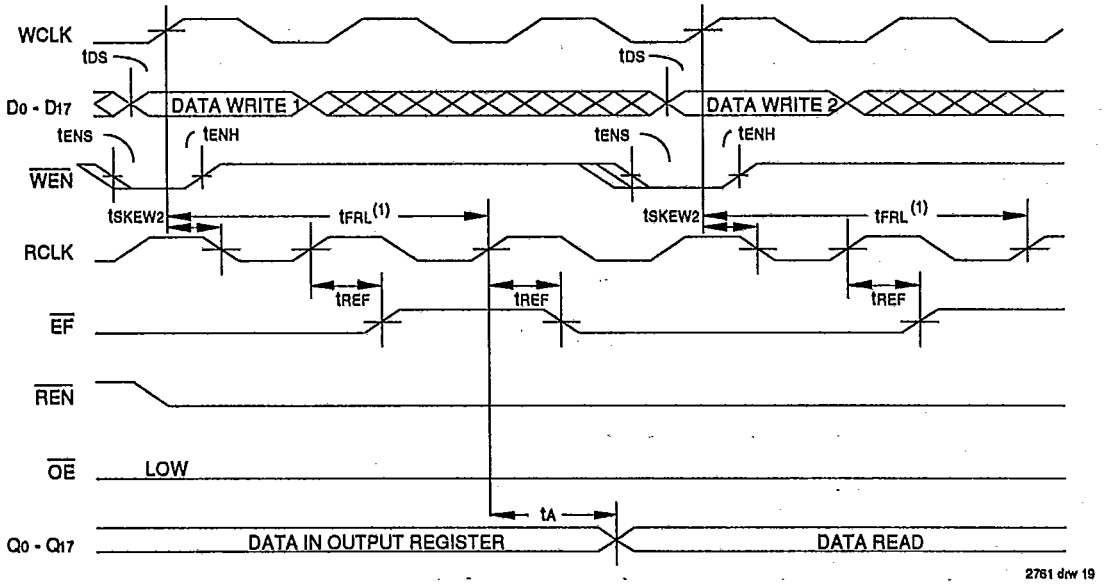

Figure 10. Empty Flag Timing

NOTE:
1. When $t_{SKEW2} \geq$ minimum specification, t_{FRL} (maximum) = 1.5 * t_{CLK} + t_{SKEW2}. When t_{SKEW2} < minimum specification, t_{FRL} (maximum) = either 2.5 * t_{CLK} + t_{SKEW2} or 1.5 * tCLK + t_{SKEW2}. The Latency Timing applies only at the Empty Boundary ($\overline{EF}$ = LOW).

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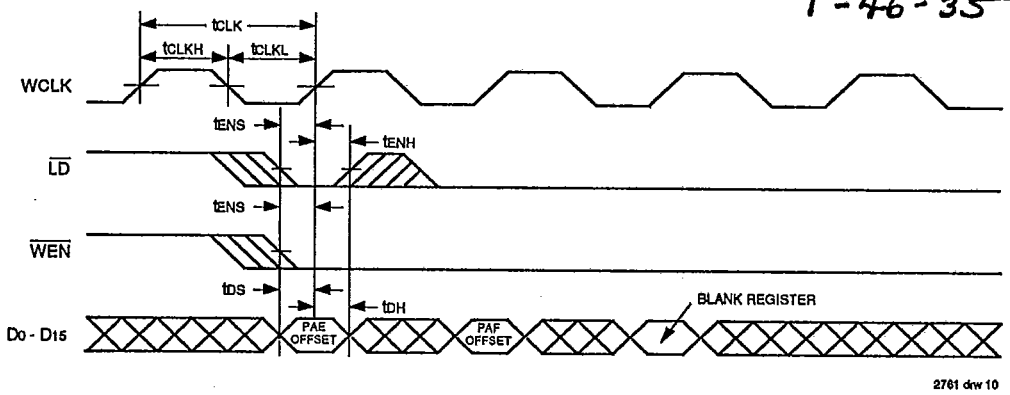


Figure 11. Write Programmable Registers

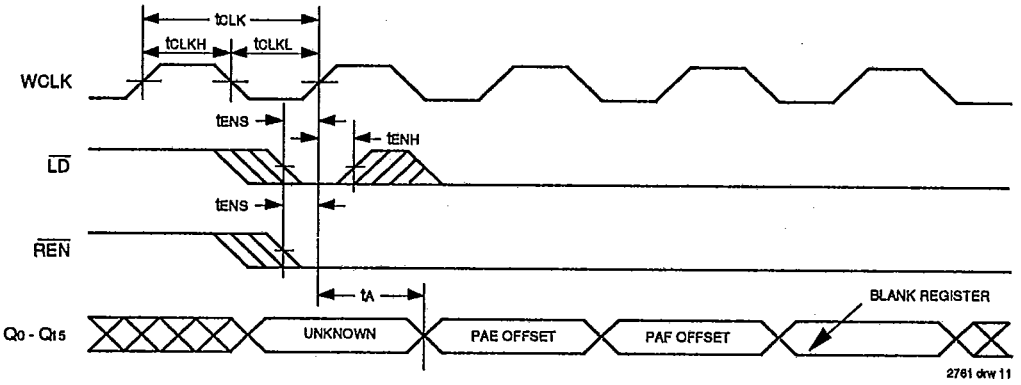
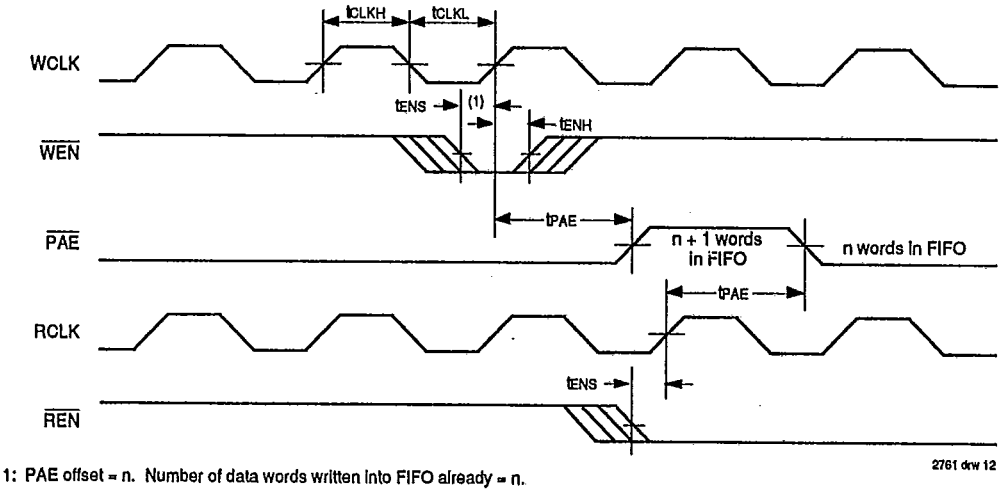


Figure 12. Read Programmable Registers



NOTE 1: PAE offset = n. Number of data words written into FIFO already = n.

Figure 13. Programmable Almost Empty Flag Timing

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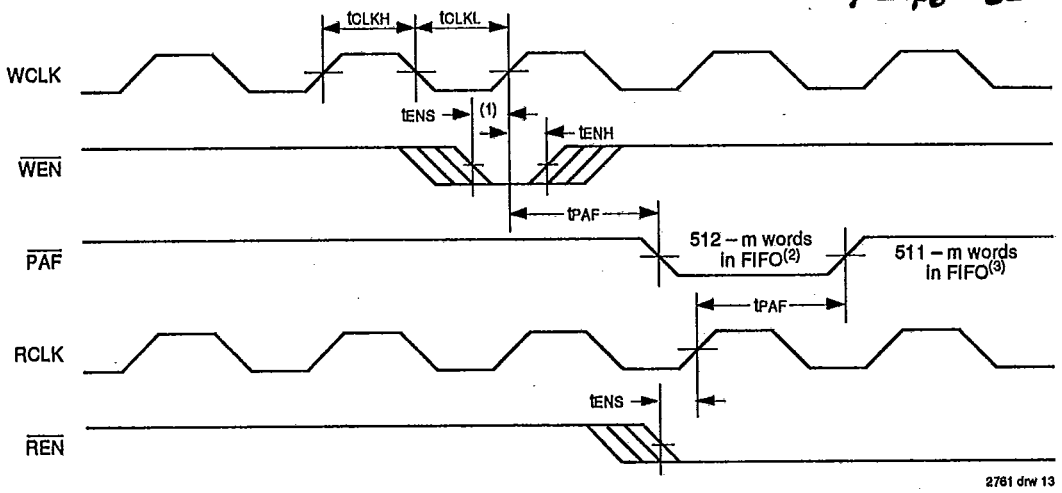

Figure 14. Programmable Almost Full Flag Timing

NOTES:
1. PAF offset = m. Number of data words written into FIFO already = 511 – m for the IDT72215L and 1023 – m for the IDT72225L.
2. 512 - m words in FIFO for IDT72215L. 1024 - m words in FIFO for IDT72225L.
3. 511 - m words in FIFO for IDT72215L. 1023 - m words in FIFO for IDT72225L.

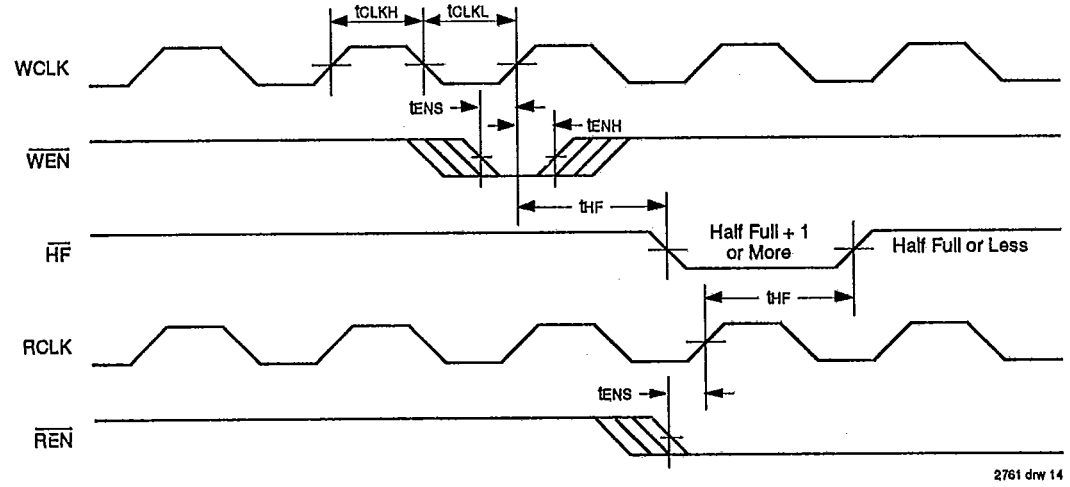

Figure 15. Half-Full Flag Timing

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OPERATING CONFIGURATIONS:

SINGLE DEVICE CONFIGURATION

A single IDT72215/72225 may be used when the application requirements are for 512/1024 words or less.

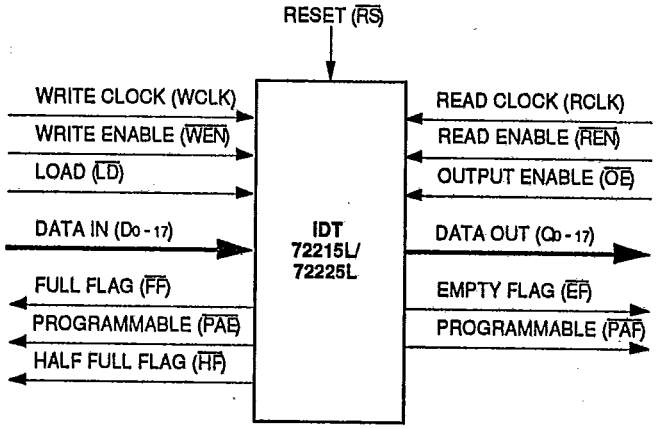

Figure 16. Block Diagram of Single 512 x 18/ 1024 x 18 Synchronous FIFO

WIDTH EXPANSION CONFIGURATION

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Asynchronous status flags ($\overline{PAE}$, $\overline{HF}$, and $\overline{PAF}$) can be detected from any one device. Synchronous status flags ($\overline{EF}$ and $\overline{FF}$) should be gated through an AND gate because the flag deassertions may vary among different FIFOs by one cycle. Figure 17 demonstrates a 36-word width by using two IDT72215L/72225Ls. Any word width can be attained by adding additional IDT72215L/72225Ls. Please see the Application Note AN-83 "Width Expansion of SyncFIFOs (Clocked FIFOs).

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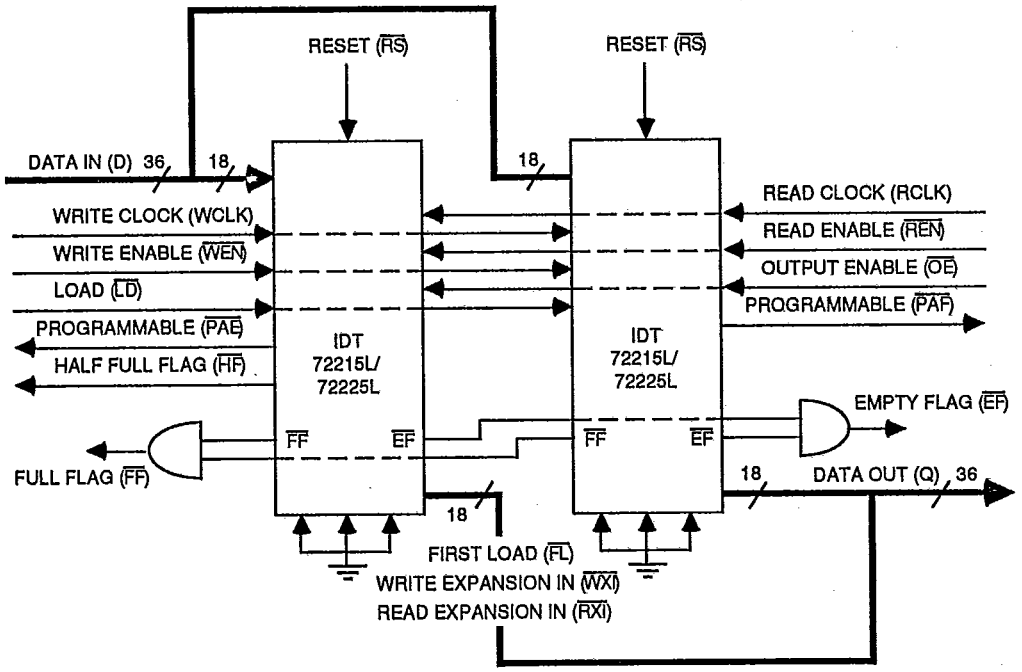

Figure 17. Block Diagram of 512 x 36/ 1024 x 36 Synchronous FIFO Memory Used in a Width Expansion Configuration

NOTE:
1. Flag detection is accomplished by monitoring the flag signals on either (any) device used in width expansion configuration. Do not connect any output control signals together.

DEPTH EXPANSION

The IDT72215L/72225L can be adapted to applications when the requirements are for greater than 512/1024 words. Depth expansion is possible by using expansion logic to direct the flow of data. A typical application would have the expansion logic alternate data accesses from one device to the next in a sequential manner. Please contact IDT Applications Engineering for details.

The 72215LB/72225LB Depth Expandable versions of this part incorporate an on-chip depth expansion technique. Please see the 72215LB/72225LB data sheet for details. The 72215LB/72225LB version will supersede this part.