Integrated Device Technology, Inc.

16-BIT CMOS MULTILEVEL PIPELINE REGISTERS

IDT73200
IDT73201

FEATURES:

- IDT73200: Eight 16-bit high-speed pipeline registers
- IDT73201: Seven 16-bit high-speed pipeline registers plus a direct feed-through path
- 10ns access time
- Programmable multilevel register configurations
- Powerful instruction set: transfer, hold, load directly
- Functionally replaces four Am29520s
- Read/Write buffer for 32-bit RISC/CISC microprocessors
- Use as temporary address storage or programmable pipeline registers for DSP products
- Coefficient storage for FIR filters
- Three-state outputs
- TTL-compatible
- Available in 48-pin plastic and ceramic DIP and 52-pin surface mount PLCC
- Military product compliant to MIL-STD-883, Class B
- Speeds available:
  Commercial: L10/12/15
  Military: L12/15/20

DESCRIPTION:

The IDT73200 and IDT73201 are mutilevel pipeline registers. With IDT's high-performance CMOS technology, the IDT73200 and IDT73201 have access times of 10ns.

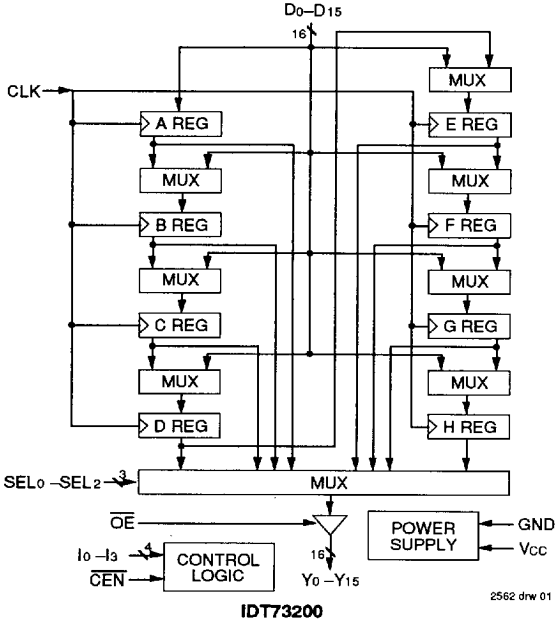
The IDT73200 contains eight 16-bit registers which can be configured as one 8-level, two 4-level, four 2-level or eight 1-level pipeline registers.

The IDT73201 contains seven 16-bit registers and a direct feed-through path. The seven registers can be configured as one 7-level, a 4-level plus a 3-level, three 2-level or seven 1-level pipeline registers.

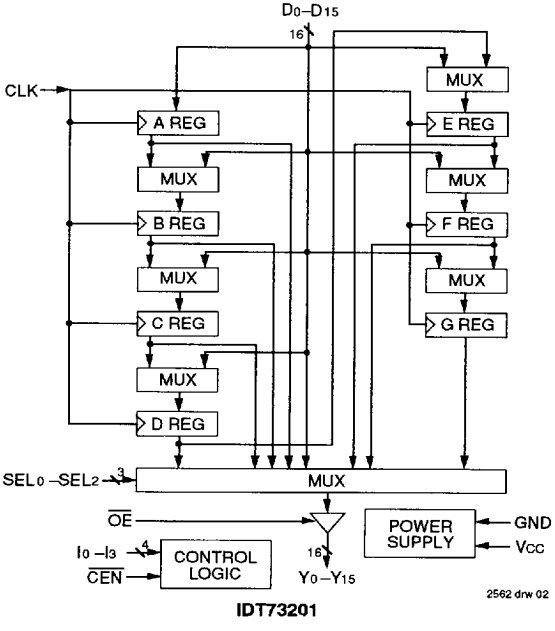
An eight-to-one output multiplexer allows data to be read from any one of the registers or from the feed-through path on the IDT73201. Three input control pins (SEL_0–SEL_2) select which of the multiplexer inputs are directed to the output (Y_0–Y_{15}).

These pipeline registers are ideal for high throughput, vector-oriented operations used in digital signal processing (DSP). The IDT73200 and IDT73201 can also be used as quick access scratch-pad registers for general purpose computing and as Read/Write buffers for RISC/CISC microprocessors.

FUNCTIONAL BLOCK DIAGRAMS



IDT73200



IDT73201

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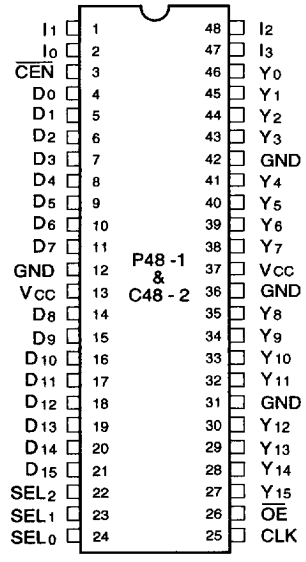
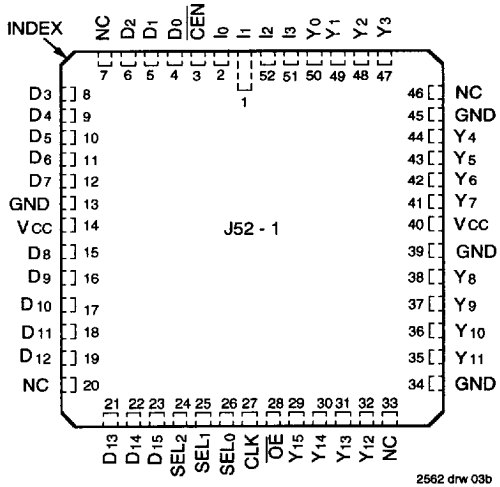
PIN CONFIGURATIONS



2562 drw 03a

DIP
TOP VIEW



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PLCC
TOP VIEW

PIN DESCRIPTIONS

Pin Name	I/O	Description
$D_0 - D_{15}$	I	Sixteen-bit data input port.
$Y_0 - Y_{15}$	O	Sixteen-bit data output port.
$I_0 - I_3$	I	Four control pins to select the register operation performed.
$SEL_0 - SEL_2$	I	Three control pins to select the register appearing at the output.
CLK	I	Clock input.
$\overline{CEN}$	I	Clock enable control pin. When this pin is low, the instruction I_0–I_3 is performed on the registers. When high, no register operation occurs.
$\overline{OE}$	I	Output enable control pin. When this pin is high, the output port Y is in a high impedance state. When low, the output port Y is active.
V_{CC}		Power supply pin, 5V.
GND		Ground pins, 0V.

2562 tbl 01

IDT73200 OUTPUT SELECTION

SEL_2	SEL_1	SEL_0	Y Output
0	0	0	$A \rightarrow Y_0 - Y_{15}$
0	0	1	$B \rightarrow Y_0 - Y_{15}$
0	1	0	$C \rightarrow Y_0 - Y_{15}$
0	1	1	$D \rightarrow Y_0 - Y_{15}$
1	0	0	$E \rightarrow Y_0 - Y_{15}$
1	0	1	$F \rightarrow Y_0 - Y_{15}$
1	1	0	$G \rightarrow Y_0 - Y_{15}$
1	1	1	$H \rightarrow Y_0 - Y_{15}$

2562 tbl 02

IDT73201 OUTPUT SELECTION

SEL_2	SEL_1	SEL_0	Y Output
0	0	0	$A \rightarrow Y_0 - Y_{15}$
0	0	1	$B \rightarrow Y_0 - Y_{15}$
0	1	0	$C \rightarrow Y_0 - Y_{15}$
0	1	1	$D \rightarrow Y_0 - Y_{15}$
1	0	0	$E \rightarrow Y_0 - Y_{15}$
1	0	1	$F \rightarrow Y_0 - Y_{15}$
1	1	0	$G \rightarrow Y_0 - Y_{15}$
1	1	1	$D_0 - D_{15} \rightarrow Y_0 - Y_{15}$

2562 tbl 03

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IDT73200 INSTRUCTION TABLE

I_3	I_2	I_1	I_0	Mnemonic	Function	Pipeline Levels
0	0	0	0	LDA	$D_0 - D_{15} \rightarrow A$	1
0	0	0	1	LDB	$D_0 - D_{15} \rightarrow B$	1
0	0	1	0	LDC	$D_0 - D_{15} \rightarrow C$	1
0	0	1	1	LDD	$D_0 - D_{15} \rightarrow D$	1
0	1	0	0	LDE	$D_0 - D_{15} \rightarrow E$	1
0	1	0	1	LDF	$D_0 - D_{15} \rightarrow F$	1
0	1	1	0	LDG	$D_0 - D_{15} \rightarrow G$	1
0	1	1	1	LDH	$D_0 - D_{15} \rightarrow H$	1
1	0	0	0	LSHAH	$D_0 - D_{15} \rightarrow A \rightarrow B \rightarrow C \rightarrow D \rightarrow E \rightarrow F \rightarrow G \rightarrow H$	8
1	0	0	1	LSHAD	$D_0 - D_{15} \rightarrow A \rightarrow B \rightarrow C \rightarrow D$	4
1	0	1	0	LSHEH	$D_0 - D_{15} \rightarrow E \rightarrow F \rightarrow G \rightarrow H$	4
1	0	1	1	LSHAB	$D_0 - D_{15} \rightarrow A \rightarrow B$	2
1	1	0	0	LSHCD	$D_0 - D_{15} \rightarrow C \rightarrow D$	2
1	1	0	1	LSHEF	$D_0 - D_{15} \rightarrow E \rightarrow F$	2
1	1	1	0	LSHGH	$D_0 - D_{15} \rightarrow G \rightarrow H$	2
1	1	1	1	HOLD	Hold All Registers	—

2562 tbl 04

IDT73201 INSTRUCTION TABLE

I_3	I_2	I_1	I_0	Mnemonic	Function	Pipeline Levels
0	0	0	0	LDA	$D_0 - D_{15} \rightarrow A$	1
0	0	0	1	LDB	$D_0 - D_{15} \rightarrow B$	1
0	0	1	0	LDC	$D_0 - D_{15} \rightarrow C$	1
0	0	1	1	LDD	$D_0 - D_{15} \rightarrow D$	1
0	1	0	0	LDE	$D_0 - D_{15} \rightarrow E$	1
0	1	0	1	LDF	$D_0 - D_{15} \rightarrow F$	1
0	1	1	0	LDG	$D_0 - D_{15} \rightarrow G$	1
0	1	1	1	HOLD	Hold All Registers	—
1	0	0	0	LSHAG	$D_0 - D_{15} \rightarrow A \rightarrow B \rightarrow C \rightarrow D \rightarrow E \rightarrow F \rightarrow G$	7
1	0	0	1	LSHAD	$D_0 - D_{15} \rightarrow A \rightarrow B \rightarrow C \rightarrow D$	4
1	0	1	0	LSHEG	$D_0 - D_{15} \rightarrow E \rightarrow F \rightarrow G$	3
1	0	1	1	LSHAB	$D_0 - D_{15} \rightarrow A \rightarrow B$	2
1	1	0	0	LSHCD	$D_0 - D_{15} \rightarrow C \rightarrow D$	2
1	1	0	1	LSHEF	$D_0 - D_{15} \rightarrow E \rightarrow F$	2
1	1	1	0	LDG	$D_0 - D_{15} \rightarrow G$	1
1	1	1	1	HOLD	Hold All Registers	—

2562 tbl 05

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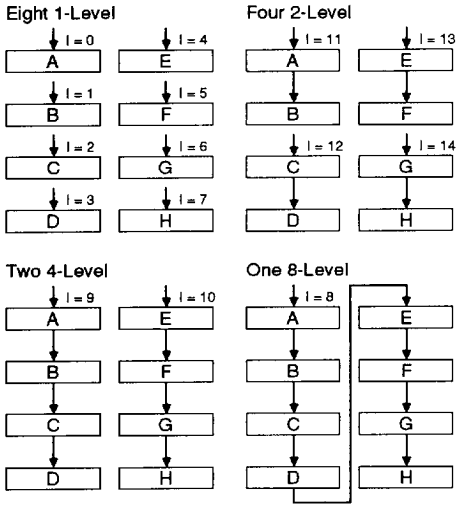
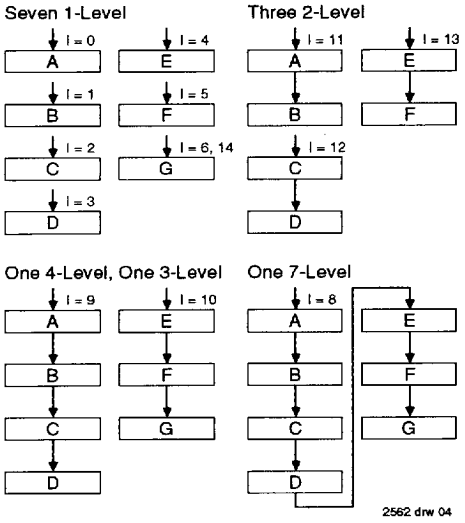
IDT73200 PIPELINE CONFIGURATIONS



IDT73201 PIPELINE CONFIGURATIONS



ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Military	Unit
V_{CC}	Power Supply Voltage	-0.5 to +7.0	-0.5 to +7.0	V
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to V_{CC} + 0.5	–0.5 to V_{CC} + 0.5	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +155	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2562 tbl 06

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE: 2562 tbl 07

1. This parameter is sampled at initial characterization and is not 100% tested.

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DC ELECTRICAL CHARACTERISTICS

Commercial: T_A = 0°C to +70°C, V_{CC} = 5V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Max	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level		—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_I = V_{CC}	—	±1	µA
I_{IL}	Input LOW Current		V_I = GND	—	±1	
I_{OZH}	High Impedance Output Current	V_{CC} = Max.	V_O = V_{CC}	—	±1	µA
I_{OZL}	(3-State Output pins)		V_O = GND	—	±1	
I_{OS}	Short Circuit Current	V_{CC} = Max.[2], V_O = GND		–20	–200	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = –6mA MIL. I_{OH} = –8mA COM'L.	2.4	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12mA MIL. I_{OL} = 16mA COM'L.	—	0.4	V

2562 tbl 08

NOTES:
1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the application device type.
2. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} = V_{CC} or GND		—	2	10	mA
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs High	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	1.5	mA/input
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max. Outputs Disabled One Bit Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.10	0.20	mA/MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max. Outputs Disabled f_{CP} = 10MHz One Bit Toggling f_i = 5MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.0	12.0[5]	mA
			V_{IN} = 3.4V V_{IN} = GND	—	3.5	13.5	

2562 tbl 09

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current (I_{CCL}, I_{CCH} and I_{CCZ})
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i

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AC ELECTRICAL CHARACTERISTICS

Commerical: T_A = 0°C to +70°C, V_{CC} = 5V ±5%; Military: T_A = –55°C to +125°C, V_{CC} = 5V ±10%

	Commercial						Military						
	73200L10 73201L10		73200L12 73201L12		73200L15 73201L15		73200L12 73201L12		73200L15 73201L15		73200L20 73201L20		
Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit
CLK to Y_0–Y_{15} Propagation Delay[2]	2.5	10	2.5	12	2.5	15	2.5	12	2.5	15	2.5	20	ns
SEL_0–SEL_2 to Y_0–Y_{15} Propagation Delay[2]	2.5	10	2.5	12	2.5	15	2.5	12	2.5	15	2.5	20	ns
D_0–D_{15} to CLK Set-up Time	3	—	3	—	4	—	3	—	4	—	5	—	ns
D_0–D_{15} to CLK Hold Time	0	—	1	—	2	—	1	—	2	—	3	—	ns
I_0–I_3 to CLK Set-up Time	3	—	4	—	5	—	4	—	5	—	6	—	ns
I_0–I_3 to CLK Hold Time	1.5	—	2	—	2	—	2	—	2	—	3	—	ns
$\overline{CEN}$ to CLK Set-up Time	3	—	4	—	5	—	4	—	5	—	6	—	ns
$\overline{CEN}$ to CLK Hold Time	1.5	—	4	—	5	—	4	—	5	—	6	—	ns
$\overline{OE}$ Enable Time	—	7	—	9	—	10	—	9	—	10	—	13	ns
$\overline{OE}$ Disable Time	—	6	—	8	—	9	—	8	—	9	—	13	ns
CLK Pulse Width HIGH[3]	5	—	5	—	5	—	5	—	5	—	6	—	ns
CLK Pulse Width LOW[3]	5	—	5	—	5	—	5	—	5	—	6	—	ns
CLK Period	10	—	12	—	15	—	12	—	15	—	20	—	ns
Data In to Data Out [1,2] Flowthrough Prop. Delay	2.5	10	2.5	12	2.5	15	2.5	12	2.5	15	2.5	20	ns

2562 tbl 10

NOTES:
1. 73201 only.
2. Minimum propagation delays are guaranteed, but not production tested.
3. Minimum pulse widths are guaranteed, but not production tested.

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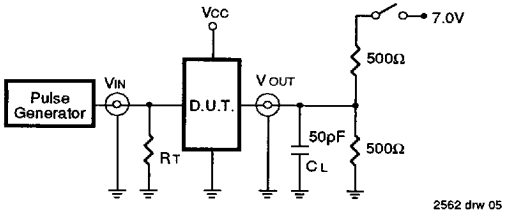
TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



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SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

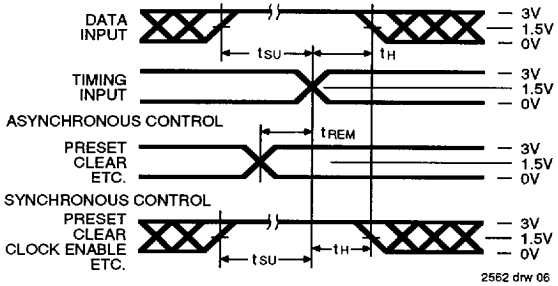
2562 lnk 11

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.

R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

SET-UP, HOLD AND RELEASE TIMES



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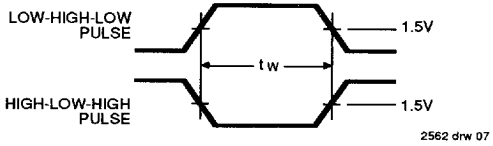
PULSE WIDTH



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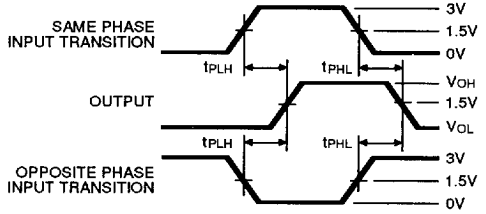
PROPAGATION DELAY



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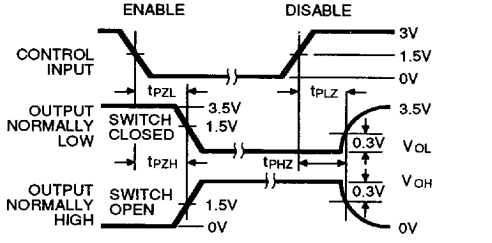
ENABLE AND DISABLE TIMES



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NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns

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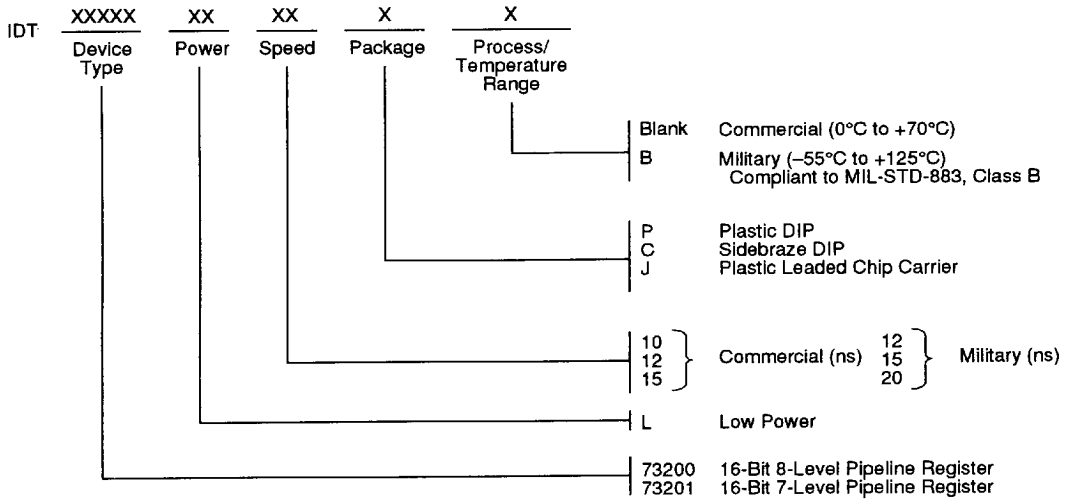
ORDERING INFORMATION



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