Integrated Device Technology, Inc.

16-BIT CMOS CASCADABLE ALU

IDT7381
IDT7383

T-49-11

FEATURES:

- High-performance 16-bit Arithmetic Logic Unit (ALU)
- 20ns to 55ns clocked ALU operations
- Ideal for radar, sonar or image processing applications
- IDT7381:
  - — 54/74S381 instruction set (8 functions)
  - — Replaces Gould S614381 or Logic Devices L4C381
  - — Cascadable with or without carry look-ahead
- IDT7383:
  - — 32 advanced ALU functions
  - — Cascadable without carry look-ahead
- Pipeline or flow-through modes
- Internal feedback path for accumulation
- Three-state outputs
- TTL-compatible
- Produced with advanced submicron CEMOS™ high-performance technology
- Available in 68-lead PGA, 68-pin surface mount PLCC and 68 pin fine-pitch Flatpack (7383 only)
- Military product compliant to MIL-STD-883, Class B
- Speeds available:
  Commercial: L20/25/30/40/55
  Military: L25/30/35/45/65

DESCRIPTION:

The IDT7381 and IDT7383 are high-speed cascadable Arithmetic Logic Unit (ALUs). Both three-bus devices have two input registers, ultra-fast 16-bit ALUs and 16-bit output registers. With IDT's high-performance CEMOS technology, the IDT7381/7383 can do arithmetic or logic operations in 20ns. The IDT7381 functionally replaces four 54/74S381 four-bit ALUs in a 68-pin package.

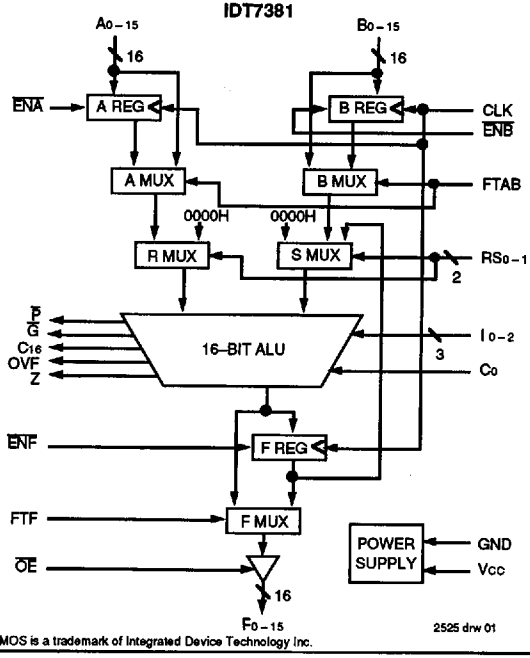
The two input operands, A and B, can be clocked or fed through for flexible pipelining. The F output can also be set into clocked or flow-through mode. An output enable is provided for three-state control of the output port on a bus.

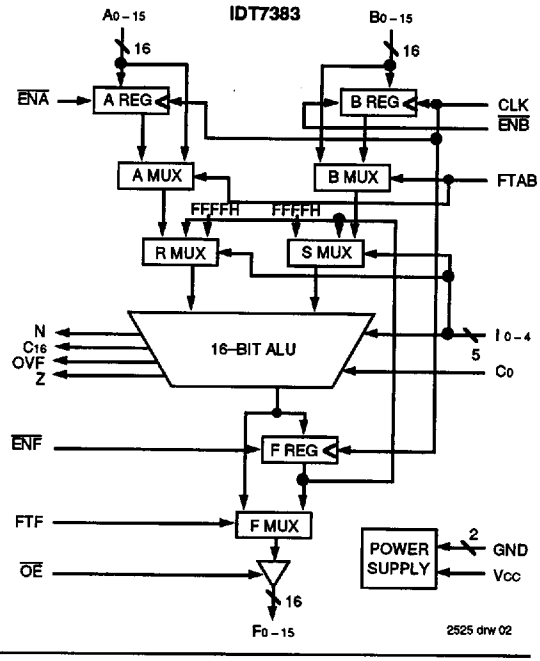
The IDT7381 has three function pins to select 1 of 8 arithmetic or logic operations. The two R and S selection pins determine whether A, B, F or 0 are fed into the ALU. This ALU has carry-out, propagate and generate outputs for cascading using carry look-ahead.

The IDT7383 has five function pins to select 1 of 32 arithmetic or logic operations. This ALU has a carry-out pin for cascading.

The IDT7381 and IDT7383 are available in 68-pin PLCC or PGA packages. Military grade product is manufactured in compliant with the latest revision of MIL-STD-883, Class B, for high reliability systems.

FUNCTIONAL BLOCK DIAGRAM





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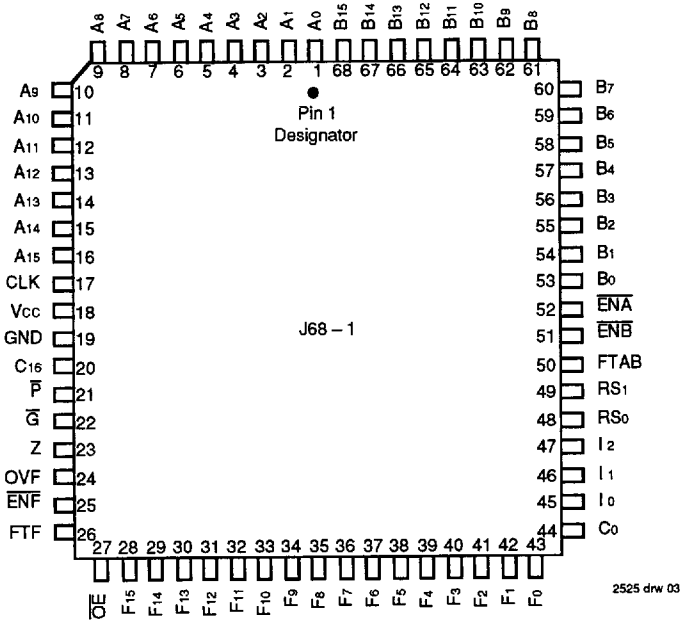
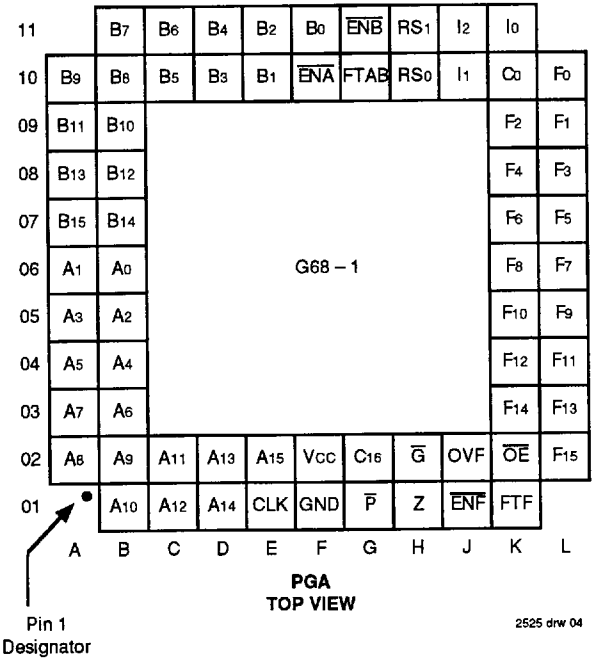
PIN CONFIGURATION

IDT7381



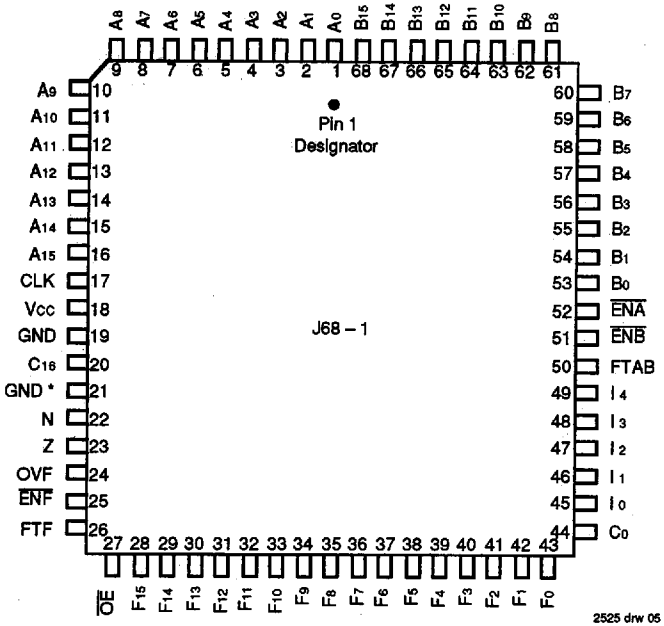
PLCC
TOP VIEW



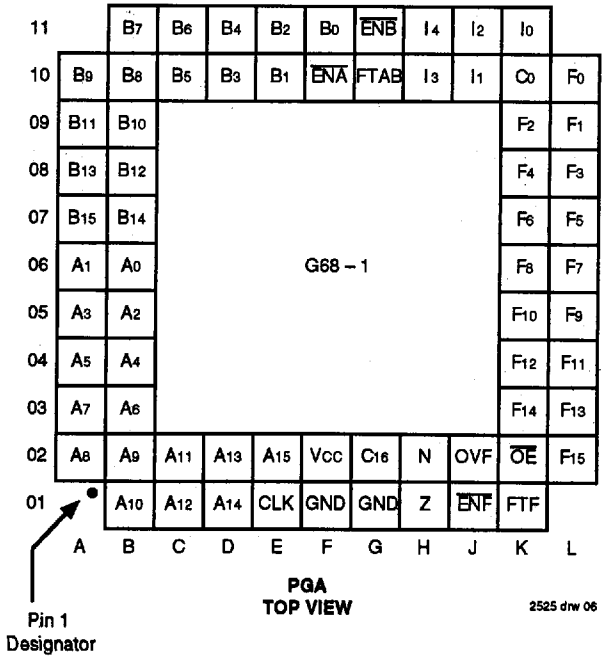
PGA
TOP VIEW

8

IDT7383

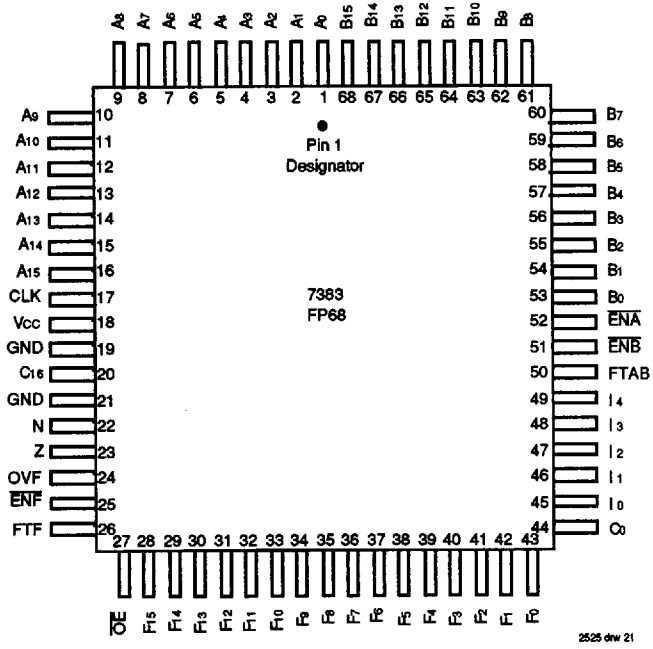


PLCC
TOP VIEW



PGA
TOP VIEW

IDT7383



FLATPACK
TOP VIEW

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PIN DESCRIPTIONS

IDT7381 AND IDT7383 PIN DESCRIPTION

Pin Name	I/O	Description
A_0 - A_{15}	I	Sixteen–bit data input port.
B_0 - B_{15}	I	Sixteen–bit data input port.
$\overline{ENA}$	I	Register enable for the A input port; active low pin.
$\overline{ENB}$	I	Register enable for the B input port; active low pin.
FTAB	I	Flow–through control pin. When this pin is high, both register A and B are transparent.
F_0 – F_{15}	O	Sixteen–bit data output port.
$\overline{ENF}$	I	Register enable for the F output port; active low pin.
FTF	I	Flow–through control pin. When this pin is high, the F register is transparent.
CLK	I	Clock input.
$\overline{OE}$	I	Output enable control pin. When this pin is high, the output port F is in a high impedance state. When low, the output port F is active.
C_0	I	Carry input. This pin receives arithmetic carries from less significant ALU components in a cascade configuration.
C_{16}	O	Carry output. This pin produces arithmetic carries to more significant ALU components in a cascaded configuration.
OVF	O	This pin indicates a two's complement arithmetic overflow, when high.
Z	O	This pin indicates a zero output result, when high.
V_{CC}		Power supply pin, 5V.
GND		Ground pin, 0V. There are two ground pins on the IDT7383.

2525 tbl 01

IDT7381 PINS

Pin Name	I/O	Description
RS_0 – RS_1	I	Two control pins used to select input operands for the R and S multiplexers.
I_0 - I_2	I	Three control pins to select the ALU function performed.
$\overline{P}$	O	Indicates the carry propagate output state to the ALU.
$\overline{G}$	O	Indicates the carry generate output state to the ALU.

2525 tbl 02

IDT7383 PINS

Pin Name	I/O	Description
I_0 – I_4	I	Five control pins to select the ALU function performed.
N	O	The sign bit of an ALU operation.

2525 tbl 05

IDT7381 R AND S MUX TABLE

RS_1	RS_0	R Mux	S Mux
0	0	A	F
0	1	A	0
1	0	0	B
1	1	A	B

2525 tbl 03

IDT7381 ALU FUNCTION TABLE

I_2	I_1	I_0	Function
0	0	0	F = 0
0	0	1	$F = \overline{R} + S + C_0$
0	1	0	$F = R + \overline{S} + C_0$
0	1	1	$F = R + S + C_0$
1	0	0	F = R xor S
1	0	1	F = R or S
1	1	0	F = R and S
1	1	1	F = all 1's

2525 tbl 04

IDT7383 ALU FUNCTION TABLE

I_4	I_3	I_2	I_1	I_0	Function
0	0	0	0	0	F = A + B + Co
0	0	0	0	1	F = A or B
0	0	0	1	0	F = A + $\overline{B}$ + Co
0	0	0	1	1	F = $\overline{A}$ + B + Co
0	0	1	0	0	F = A + Co
0	0	1	0	1	F = $\overline{A}$ or F
0	0	1	1	0	F = A – 1 + Co
0	0	1	1	1	F = $\overline{A}$ + Co
0	1	0	0	0	F = A + F + Co
0	1	0	0	1	F = A or F
0	1	0	1	0	F = A + $\overline{F}$ + Co
0	1	0	1	1	F = $\overline{A}$ + F + Co
0	1	1	0	0	F = F + B + Co
0	1	1	0	1	F = $\overline{A}$ or B
0	1	1	1	0	F = F + $\overline{B}$ + Co
0	1	1	1	1	F = $\overline{F}$ + B + Co
1	0	0	0	0	F = A xor B
1	0	0	0	1	F = A and B
1	0	0	1	0	F = $\overline{A}$ and B
1	0	0	1	1	F = A xnor B
1	0	1	0	0	F = A xor F
1	0	1	0	1	F = A and F
1	0	1	1	0	F = $\overline{A}$ and F
1	0	1	1	1	F = all 1's + Co
1	1	0	0	0	F = B + Co
1	1	0	0	1	F = A and $\overline{B}$
1	1	0	1	0	F = $\overline{B}$ + Co
1	1	0	1	1	F = B – 1 + Co
1	1	1	0	0	F = F + Co
1	1	1	0	1	F = A or $\overline{B}$
1	1	1	1	0	F = F – 1 + Co
1	1	1	1	1	F = $\overline{F}$ + Co

2525 tbl 06

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to Ground	–0.5 to V_{CC} + 0.5	–0.5 to V_{CC} + 0.5	V
V_{CC}	Power Supply Voltage	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2525 tbl 07

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Under no circumstances should an input of an I/O Pin be greater than V_{CC} + 0.5V.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE: 2525 tbl 09

1. This parameter is sampled at initial characterization and is not production tested.

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DC ELECTRICAL CHARACTERISTICS

Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.7V		—	—	10	µA
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.5V		—	—	–10	µA
I_{OS}[3]	Short Circuit Current	V_{CC} = Max., V_{OUT} = GND		–20	—	–100	mA
I_{OZ}	Off State (High Impedance) Output Current	V_{CC} = Max.	V_O = 0.5V	—	–0.1	–20	µA
			V_O = 2.7V	—	–0.1	20	
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –4mA	2.4	—	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4mA MIL.	—	—	0.5	V
			I_{OL} = 8mA COM'L.				

2525 tbl 08

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

Commercial: T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%; Military: T_A = –55°C to +125°C, V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
I_{CCQC}	Quiescent Power Supply Current	V_{CC} = Max. V_{IN} =0V or V_{CC}	COM'L.	—	2	10	mA
			MIL.	—	2	15	
I_{CCQT}[3]	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V	COM'L.	—	0.5	2	mA
			MIL.	—	0.5	2.5	
I_{CCD1}	Dynamic Power Supply Current	Mode: FTAB = FTF = 1 V_{CC} = Max. Outputs Disabled f_i = 10MHz 50% Duty Cycle V_{IL} = 0V, V_{IH} = V_{CC}	COM'L.	—	10	35	mA
			MIL.	—	10	55	
I_{CCD2}	Dynamic Power Supply Current	Mode: FTAB = FTF = 1 V_{CC} = Max. Outputs Disabled f_i = 20MHz 50% Duty Cycle V_{IL} = 0V, V_{IH} = V_{CC}	COM'L.	—	30	60	mA
			MIL.	—	30	80	

2525 tbl 10

NOTES:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Output Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Input Frequency
   N_i = Number of Inputs at f_i
   All currents are in milliamps and all frequencies are in megahertz.

AC ELECTRICAL CHARACTERISTICS — COMMERCIAL (V_{CC} = 5V ± 5%, T_A = 0°C to +70°C)

Maximum Combinational Propagation Delays

From Input	IDT7381L20 IDT7383L20				IDT7381L25 IDT7383L25				IDT7381L30 IDT7383L30				Unit
	F_{0-15}	$\overline{P}, \overline{G}, N$	Z,OVF	C_{16}	F_{0-15}	$\overline{P}, \overline{G}, N$	Z,OVF	C_{16}	F_{0-15}	$\overline{P}, \overline{G}, N$	Z,OVF	C_{16}	
FTAB = 0, FTF = 0													
CLK	11	20	20	20	13	22	26	22	20	28	30	28	ns
C_0	—	—	14	14	—	—	16	16	—	—	20	20	ns
I_{0-4}, RS_0, RS_1	—	18	20	18	—	22	22	22	—	28	28	28	ns
FTAB = 0, FTF = 1													
CLK	20	20	20	20	27	22	26	22	33	28	30	28	ns
C_0	18	—	14	14	22	—	16	16	28	—	20	20	ns
I_{0-4}, RS_0, RS_1 (1)	20	18	20	18	22	22	22	22	28	28	28	28	ns
FTAB = 1, FTF = 0													
A_0–A_{15}, B_0–B_{15}	—	16	20	17	—	18	25	22	—	24	30	28	ns
CLK	11	—	—	—	13	—	—	—	19	—	—	—	ns
C_0	—	—	14	14	—	—	16	16	—	—	20	20	ns
I_{0-4}, RS_0, RS_1 (1)	—	18	20	18	—	22	22	22	—	28	28	28	ns
FTAB = 1, FTF = 1													
A_0–A_{15}, B_0–B_{15}	20	16	20	17	26	18	25	22	32	24	30	28	ns
C_0	18	—	14	14	22	—	16	16	28	—	20	20	ns
I_{0-4}, RS_0, RS_1 (1)	20	18	20	18	22	22	22	22	28	28	28	28	ns

NOTE:
1. Minimum propagation delays are guaranteed to be greater than or equal to 3ns although not production tested.

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Maximum Combinational Propagation Delays

From Input	IDT7381L40 IDT7383L40				IDT7381L55 IDT7383L55				Unit
	F_{0-15}	$\overline{P}, \overline{G}, N$	Z, OVF	C_{16}	F_{0-15}	$\overline{P}, \overline{G}, N$	Z, OVF	C_{16}	
FTAB = 0, FTF = 0									
CLK	26	30	44	32	32	38	53	36	ns
C_0	—	—	28	20	—	—	34	22	ns
I_{0-4}, RS_0, RS_1	—	32	34	35	—	42	42	42	ns
FTAB = 0, FTF = 1									
CLK	46	30	44	32	56	38	53	36	ns
C_0	30	—	28	20	37	—	34	22	ns
I_{0-4}, RS_0, RS_1 (1)	40	32	34	35	55	42	42	42	ns
FTAB = 1, FTF = 0									
A_0–A_{15}, B_0–B_{15}	—	30	40	32	—	36	46	37	ns
CLK	26	—	—	—	32	—	—	—	ns
C_0	—	—	28	20	—	—	34	22	ns
I_{0-4}, RS_0, RS_1 (1)	—	32	34	35	—	42	42	42	ns
FTAB = 1, FTF = 1									
A_0–A_{15}, B_0–B_{15}	40	30	40	32	55	36	46	37	ns
C_0	30	—	28	20	37	—	34	22	ns
I_{0-4}, RS_0, RS_1 (1)	40	32	34	35	55	42	42	42	ns

NOTE:
1. Minimum propagation delays are guaranteed to be greater than or equal to 3ns although not production tested.

2525 tb 12

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AC ELECTRICAL CHARACTERISTICS — COMMERCIAL (Vcc = 5V ± 5%, TA = 0°C to +70°C) - (Cont'd.)

Minimum Set-up and Hold Times Relative to Clock (CLK)

Input	IDT7381L20 IDT7383L20		IDT7381L25 IDT7383L25		IDT7381L30 IDT7383L30		IDT7381L40 IDT7383L40		IDT7381L55 IDT7383L55		Unit
	Set-up	Hold	Set-up	Hold	Set-up	Hold	Set-up	Hold	Set-up	Hold	
FTAB = 0, FTF = X											
A_0–A_{15}, B_0–B_{15}	5	0	6	0	6	0	6	0	8	0	ns
C_0 (2)	12	0	16	0	16	0	16	0	21	0	ns
I_{0-4}, RS_0, RS_1 (1) (2)	15	0	24	0	29	0	32	0	44	0	ns
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	5	0	6	0	6	0	6	0	8	0	ns
FTAB = 1, FTF = 0											
A_0–A_{15}, B_0–B_{15}	14	0	16	0	25	0	28	0	35	0	ns
C_0	12	0	16	0	16	0	16	0	21	0	ns
I_{0-4}, RS_0, RS_1 (1)	15	0	24	0	29	0	32	0	44	0	ns
$\overline{ENF}$	5	0	6	0	6	0	6	0	8	0	ns

2525 tbl 13

Minimum Clock Cycle Times and Pulse Widths

Parameter	IDT7381L20 IDT7383L20	IDT7381L25 IDT7383L25	IDT7381L30 IDT7383L30	IDT7381L40 IDT7383L40	IDT7381L55 IDT7383L55	Unit
Clock LOW Time	5	6	8	10	14	ns
Clock HIGH Time	5	6	8	10	14	ns
Clock Period	18	20	25	34	43	ns

2525 tbl 14

Maximum Output Enable/Disable Times

Parameter	IDT7381L20 IDT7383L20	IDT7381L25 IDT7383L25	IDT7381L30 IDT7383L30	IDT7381L40 IDT7383L40	IDT7381L55 IDT7383L55	Unit
Enable Time	8	10	15	18	20	ns
Disable Time	8	10	15	18	20	ns

2525 tbl 15

NOTES:
1. For IDT7381, pins I_0 – I_2, RS_0, RS_1 apply. For IDT7383, pins I_0 – I_4 apply.
2. Only for FTF = 0.

AC ELECTRICAL CHARACTERISTICS — MILITARY (Vcc = 5V ± 10%, TA = –55°C to +125°C)

Maximum Combinational Propagation Delays

From Input	IDT7381L25 IDT7383L25				IDT7381L30 IDT7383L30				IDT7381L35 IDT7383L35				Unit
	F0–15	P, G, N	Z,OVF	C16	F0–15	P, G, N	Z,OVF	C16	F0–15	P, G, N	Z,OVF	C16	
FTAB = 0, FTF = 0													
CLK	14	24	24	24	26	28	34	28	27	32	45	32	ns
C0	—	—	18	18	—	—	22	22	—	—	30	23	ns
I0–4, RS0, RS1 (1)	—	22	24	22	—	28	28	28	—	34	34	34	ns
FTAB = 0, FTF = 1													
CLK	25	24	24	24	34	28	34	28	45	32	40	32	ns
C0	21	—	18	18	26	—	22	22	30	—	30	23	ns
I0–4, RS0, RS1 (1)	25	22	24	22	30	28	28	28	40	34	34	34	ns
FTAB = 1, FTF = 0													
A0–A15, B0–B15	—	20	25	22	—	28	28	28	—	30	35	32	ns
CLK	14	—	—	—	26	—	—	—	27	—	—	—	ns
C0	—	—	18	18	—	—	22	22	—	—	30	23	ns
I0–4, RS0, RS1 (1)	—	22	24	22	—	28	28	28	—	34	34	34	ns
FTAB = 1, FTF = 1													
A0–A15, B0–B15	25	22	25	22	30	28	28	28	40	30	30	32	ns
C0	21	—	18	18	26	—	22	22	30	—	30	23	ns
I0–4, RS0, RS1 (1)	25	22	24	22	30	28	28	28	40	34	34	34	ns

NOTE:
1. Minimum propagation delays are guaranteed to be greater than or equal to 3ns although not production tested.

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Maximum Combinational Propagation Delays

From Input	IDT7381L45 IDT7383L45				IDT7381L65 IDT7383L65				Unit
	F0–15	P, G, N	Z, OVF	C16	F0–15	P, G, N	Z, OVF	C16	
FTAB = 0, FTF = 0									
CLK	28	34	50	34	37	44	63	45	ns
C0	—	—	32	23	—	—	42	25	ns
I0–4, RS0, RS1 (1)	—	38	38	38	—	48	48	48	ns
FTAB = 0, FTF = 1									
CLK	56	34	50	34	68	44	63	45	ns
C0	32	—	32	23	42	—	42	25	ns
I0–4, RS0, RS1 (1)	46	38	38	38	66	48	48	48	ns
FTAB = 1, FTF = 0									
A0–A15, B0–B15	—	32	46	36	—	44	56	44	ns
CLK	28	—	—	—	37	—	—	—	ns
C0	—	—	32	23	—	—	42	25	ns
I0–4, RS0, RS1 (1)	—	38	38	38	—	48	48	48	ns
FTAB = 1, FTF = 1									
A0–A15, B0–B15	45	32	46	36	65	44	56	44	ns
C0	32	—	32	23	42	—	42	25	ns
I0–4, RS0, RS1 (1)	46	38	38	38	66	48	48	48	ns

NOTE:
1. Minimum propagation delays are guaranteed to be greater than or equal to 3ns although not production tested.

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AC ELECTRICAL CHARACTERISTICS — MILITARY (Vcc = 5V ± 10%, TA = –55°C to +125°C) - (Cont'd)

Minimum Set-up and Hold Times Relative to Clock (CLK)

Input	IDT7381L25 IDT7383L25		IDT7381L30 IDT7383L30		IDT7381L35 IDT7383L35		IDT7381L45 IDT7383L45		IDT7381L65 IDT7383L65		Unit
	Set-up	Hold	Set-up	Hold	Set-up	Hold	Set-up	Hold	Set-up	Hold	
FTAB = 0, FTF = X											
A_0–A_{15}, B_0–B_{15}	7	0	8	0	8	0	8	0	10	0	ns
C_0 (2)	14	0	18	0	19	0	20	0	25	0	ns
I_{0-4}, RS_0, RS_1 (1) (2)	19	0	30	0	32	0	36	0	50	0	ns
$\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$	7	0	8	0	8	0	8	0	10	0	ns
FTAB = 1, FTF = 0											
A_0–A_{15}, B_0–B_{15}	14	0	27	0	30	0	33	0	43	0	ns
C_0	14	0	18	0	19	0	20	0	25	0	ns
I_{0-4}, RS_0, RS_1 (1)	19	0	30	0	34	0	36	0	50	0	ns
$\overline{ENF}$	7	0	8	0	8	0	8	0	10	0	ns

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Minimum Clock Cycle Times and Pulse Widths

Parameter	IDT7381L25 IDT7383L25	IDT7381L30 IDT7383L30	IDT7381L35 IDT7383L35	IDT7381L45 IDT7383L45	IDT7381L65 IDT7383L65	Unit
Clock LOW Time	8	12	13	15	20	ns
Clock HIGH Time	8	12	13	15	20	ns
Clock Period	20	26	30	38	52	ns

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Maximum Output Enable/Disable Times

Parameter	IDT7381L25 IDT7383L25	IDT7381L30 IDT7383L30	IDT7381L35 IDT7383L35	IDT7381L45 IDT7383L45	IDT7381L65 IDT7383L65	Unit
Enable Time	14	18	19	20	22	ns
Disable Time	14	18	19	20	22	ns

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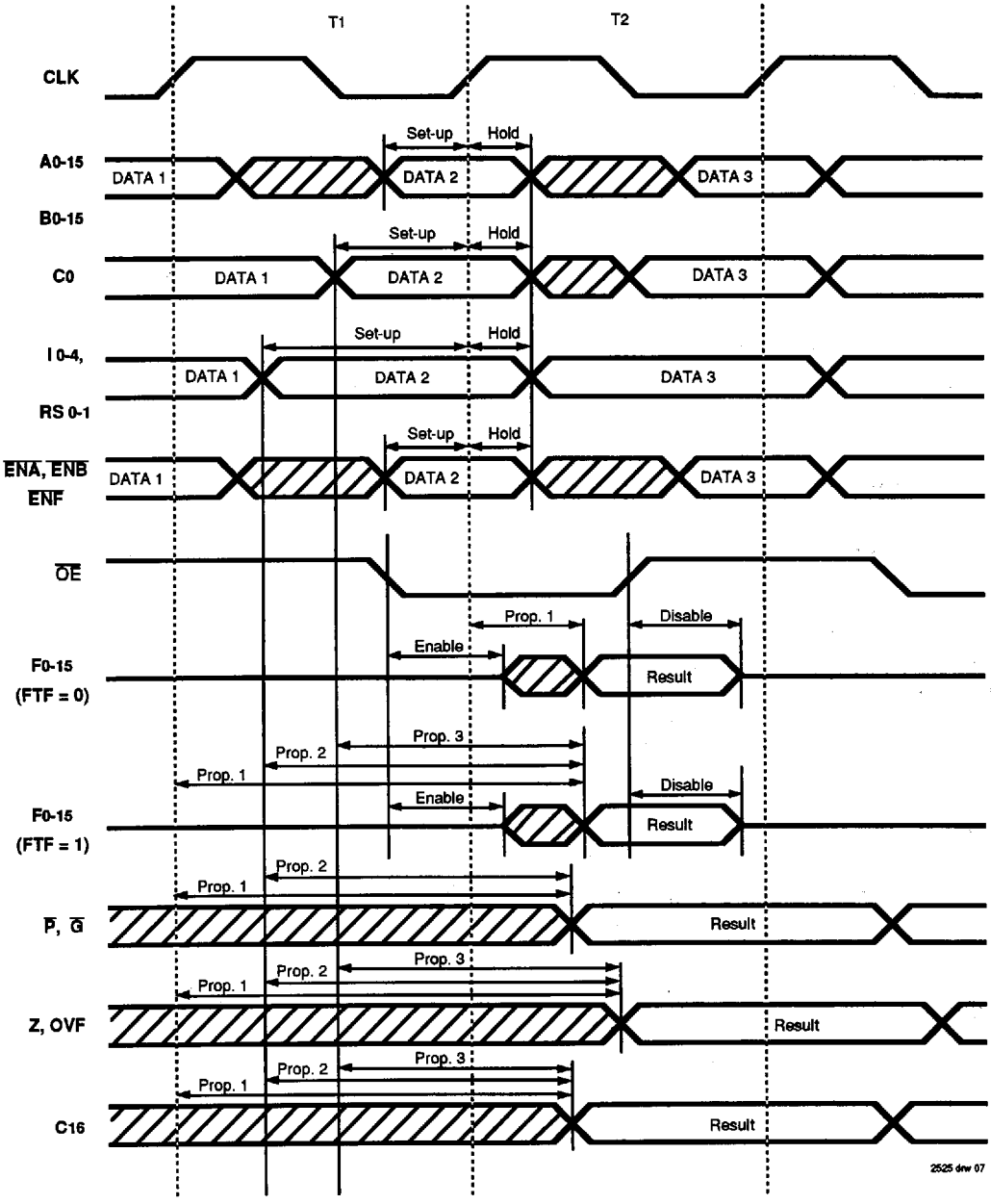
NOTES:
1. For IDT7381, pins I_0 – I_2, RS_0, RS_1 apply. For IDT7383, pins I_0 – I_4 apply.
2. Only for FTF = 0.

WAVEFORMS FOR FTAB = 0, FTF = X



Prop. 1: Propagation delay with respect to the CLK.
Prop. 2: Propagation delay with respect to b_{-4}, RS_{0-2}.
Prop. 3: Propagation delay with respect to C_0.

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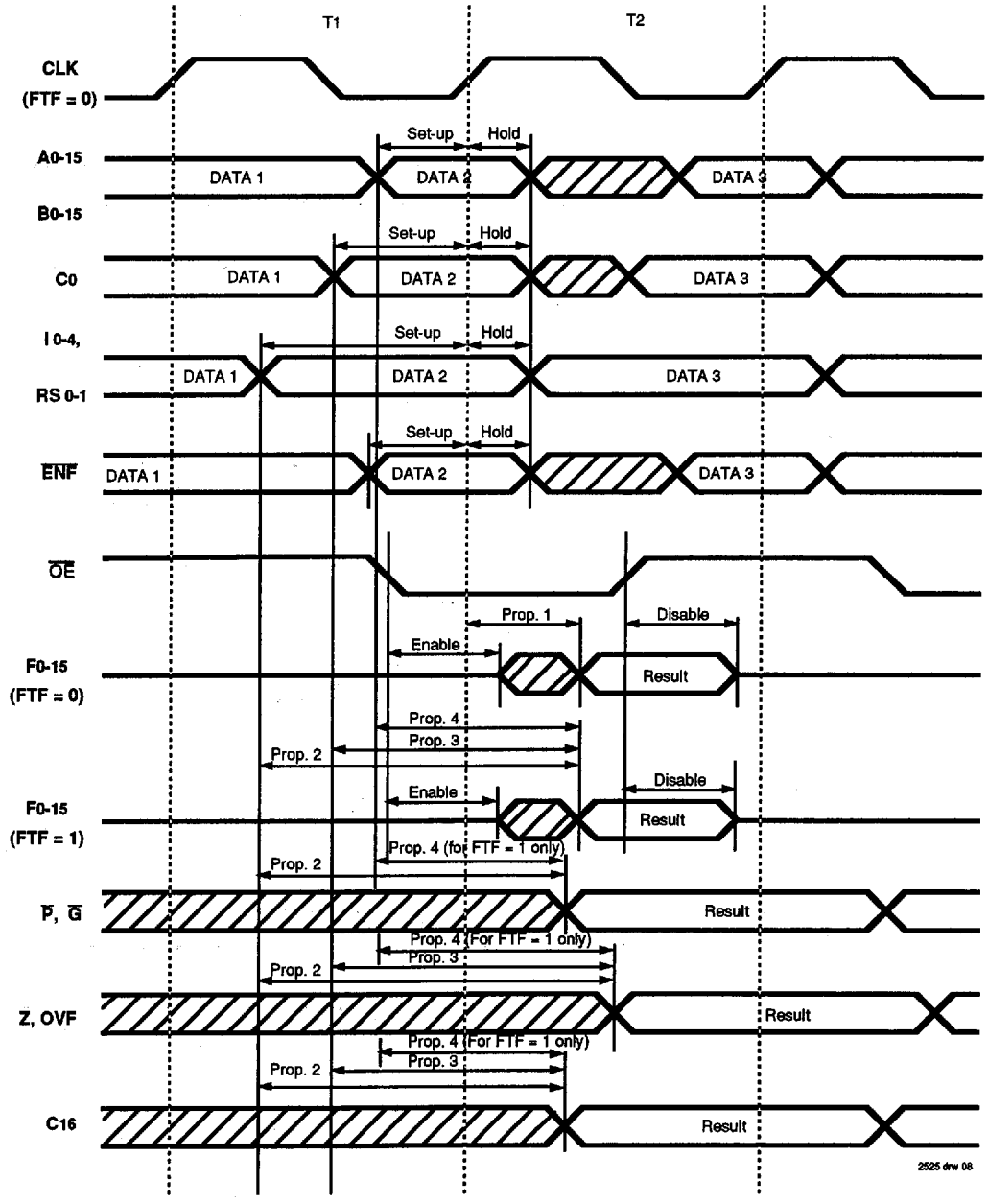
WAVEFORMS FOR FTAB = 1, FTF = X



Prop. 1: Propagation delay with respect to the CLK.
Prop. 2: Propagation delay with respect to b_{-4}, $RS0_{-2}$.
Prop. 3: Propagation delay with respect to C_0.
Prop. 4: Propagation delay with respect to A, B.

PROPAGATION DELAY CALCULATIONS FOR TWO IDT7381/7383s

From Input	To Output		To Set PUT Time
	F_{0-15}	Flags [2]	Relative to Clock (CLK)
FTAB = 0, FTF = 0			
CLK	As in 16-bit case	(Clk → C_{16}) + (C_0 → flag)	....
C_0	....	(C_0 → C_{16}) + (C_0 → flag)	(C_0 → C_{16}) + (C_0 set–up time)
I_{0-4}, RS_{0-1} [1]	....	(I_{0-4}, RS_{0-1} → C_{16}) + (C_0 → flag)	(I_{0-4}, RS_{0-1} → C_{16}) + (C_0 set–up time)
A_{0-15}, B_{0-15}	....	....	As in 16-bit case
ENA, ENB, ENF	....	....	As in 16-bit case
FTAB = 0, FTF = 1			
CLK	(Clk → C_{16}) + (C_0 → F_{0-15})	(Clk → C_{16}) + (C_0 → flag)	....
C_0	(C_0 → C_{16}) + (C_0 → F_{0-15})	(C_0 → C_{16}) + (C_0 → flag)	(C_0 → C_{16}) + (C_0 set–up time)
I_{0-4}, RS_{0-1} [1]	(I_{0-4}, RS_{0-1} → C_{16}) + (C_0 → F_{0-15})	(I_{0-4}, RS_{0-1} → C_{16}) + (C_0 → flag)	(I_{0-4}, RS_{0-1} → C_{16}) + (C_0 set–up time)
A_{0-15}, B_{0-15}	....	....	As in 16-bit case
ENA, ENB, ENF	....	....	As in 16-bit case
FTAB = 1, FTF = 0			
CLK	As in 16-bit case	....	....
C_0	....	(C_0 → C_{16}) + (C_0 → flag)	(C_0 → C_{16}) + (C_0 set–up time)
I_{0-4}, RS_{0-1} [1]	....	(I_{0-4}, RS_{0-1} → C_{16}) + (C_0 → flag)	(I_{0-4}, RS_{0-1} → C_{16}) + (C_0 set–up time)
A_{0-15}, B_{0-15}	....	(A_{0-15}, B_{0-15} → C_{16}) + (C_0 → flag)	As in 16-bit case
ENA, ENB, ENF	....	....	As in 16-bit case
FTAB = 0, FTF = 1			
CLK	Don't care condition	Don't care condition	....
C_0	(C_0 → C_{16}) + (C_0 → F_{0-15})	(C_0 → C_{16}) + (C_0 → flag)	....
I_{0-4}, RS_{0-1} [1]	(I_{0-4}, RS_{0-1} → C_{16}) + (C_0 → F_{0-15})	(I_{0-4}, RS_{0-1} → C_{16}) + (C_0 → flag)	....
A_{0-15}, B_{0-15}	(A_{0-15}, B_{0-15} → C_{16}) + (C_0 → F_{0-15})	(A_{0-15}, B_{0-15} → C_{16}) + (C_0 → flag)	....
ENA, ENB, ENF	....	....	....

NOTES:
1. For IDT7381, pins I_{0-2}, RS_{0-2} apply. For IDT7383, pins I_{0-4} apply.
2. Flags are $\overline{P}$, $\overline{G}$, OVF, Z, C_{16} for IDT7381. Flags are N, OVF, Z C_{16} for IDT7383.

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CASCADING THE IDT7381/3

Some applications require 32-bit or wider input operands. Cascading is the hardware solution. It provides a high speed alternative in handling more than 16-bit wide operands.

This section is divided in three parts:

1. Cascading the IDT7381
2. Cascading the IDT7383
3. Time delay considerations

1. Cascading the IDT7381

Cascading to 32-bit wide operands takes only two IDT7381s and no external hardware. However, cascading to data widths greater than 32-bit can be done in two ways: without external hardware (slow method) or by using a carry look ahead generator like FCT182 (fast method).

a) Cascading the IDT7381 without a carry-look-ahead generator: (Figures 2 and 3)

1. Connect the C_{16} output of the least significant device into the Co input of the next most significant device.
2. Common lines to all devices are: RS_{0-1}, I_{0-2}, Clk, FTF, FTAB, $\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$.
3. Take OVF, C_{16}, $\overline{P}$, $\overline{G}$ of the most significant device as valid.
4. The system's zero flag (Z) is obtained by ANDing all zero flag results.

b) Cascading three or more IDT7381s with carry-look-ahead (CLA) generator: (Figure 4)

1. Connect the $\overline{P}$ and $\overline{G}$ outputs of each device to the CLA generator's corresponding inputs.
2. Take the CLA generator outputs into the Co inputs of each device (except for the least significant one).
3. Common lines to all devices are: RS_{0-1}, I_{0-2}, Clk, FTF, FTAB, $\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$.
4. Take OVF, C_{16}, $\overline{P}$, $\overline{G}$ of the most significant device as valid.
5. Carry-in to the system should be connected to the Co input of the least significant device and also to the CLA generator.

2. Cascading the IDT7383

(Figures 5 and 6)

1. Connect the C_{16} output of the least significant device into the Co input of the next most significant device.
2. Common lines to all devices are: I_{0-4}, Clk, FTF, FTAB, $\overline{ENA}$, $\overline{ENB}$, $\overline{ENF}$.
3. Take OVF, C_{16}, N of the most significant device as valid.
4. The system's zero flag (Z) is obtained by ANDing all zero flag results.

3. Time Delay Considerations

Once cascading has taken place, time delays may become critical in high performance systems. Our main interest here is focused on "propagation delays", i.e. calculating the time required for an input signal to propagate through several cascaded devices up to a specific output in another device within the cascaded system.

Propagation Delay

The propagation delay *for two devices* between the input and output of interest (input to output delay) is done as follows:

1. Calculate delay between the input and C_{16} in the first device.
2. Calculate delay between Co and the output in the second device.
3. Add both results.

The following table is an example on how to build a propagation delay table for all inputs in a 32-bit IDT7381/3 cascaded system.

Propagation delay calculations can be extended to *n–cascaded* devices as the sum of the delays in all devices between the input and output of interest. That is:

$(Input)_1 \rightarrow (C_{16})_1 = t_1$

...

$(Co)_i \rightarrow (C_{16})_i = t_i$

$(Co)_{i+1} \rightarrow (C_{16})_{i+1} = t_{i+1}$

...

$(Co)_n \rightarrow (Output)_n = t_n$

Where the subscript i denotes the device number and the arrow (→) represents the delay in between. Notice that i + 1 is the immediate upper device from device i. Adding the delays t_i we get:

Propagation delay = $t_1 + t_2 + ... + t_i + t_{i+1} + ... + t_n$

Total Delay

As seen from Figure 11, the propagation delay is within the IDT7381/3 devices only. A complete analysis should also include the delay associated with the transmission line Li (which depends on the line length and its impedance). This line delay should then be added to the propagation delay to obtain the total delay for the cascaded system:

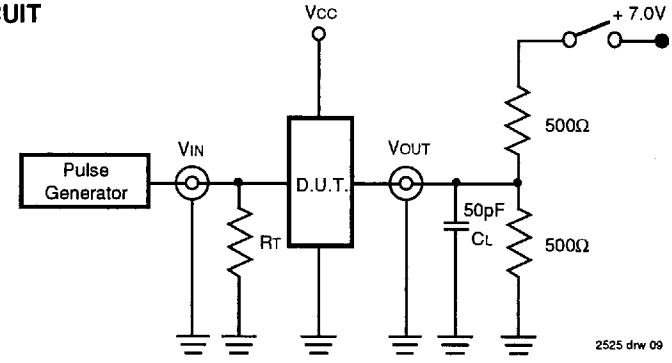
Total delay = Propagation delay + Transmission line delay

CMOS TESTING CONSIDERATIONS

There are certain testing considerations which must be taken into account when testing high-speed CMOS devices in an automatic environment. These are:

1) Proper decoupling at the test head is necessary. Placement of the capacitor set and the value of capacitors used is critical in reducing the potential erroneous failures resulting from large V_{CC} current changes. Capacitor lead length must be short and as close to the DUT power pins as possible.
2) All input pins should be connected to a voltage potential during testing. If left floating, the device may begin to oscillate causing improper device operation and possible latchup.
3) Definition of input levels is very important. Since many inputs may change coincidentally, significant noise at the device pins may cause the V_{IL} and V_{IH} levels not to be met until the noise has settled. To allow for this testing/board induced noise, IDT recommends using $V_{IL} \leq 0V$ and $V_{IH} \geq 3V$ for AC tests.
4) Device grounding is extremely important for proper device testing. The use of multi-layer performance boards with radial decoupling between power and ground planes is required. The ground plane must be sustained from the performance board to the DUT interface board. All unused interconnect pins must be properly connected to the ground pin. Heavy gauge stranded wire should be used for power wiring and twisted pairs are recommended to minimize inductance.

TEST LOAD CIRCUIT



DEFINITIONS:
C_L = Load capacitance: includes jig and probe capacitance
R_L = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator

Figure 1. AC Test Load Circuit

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	1V/ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

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Test	Switch
Disable Low	Closed
Enable Low	
All other Outputs	Open

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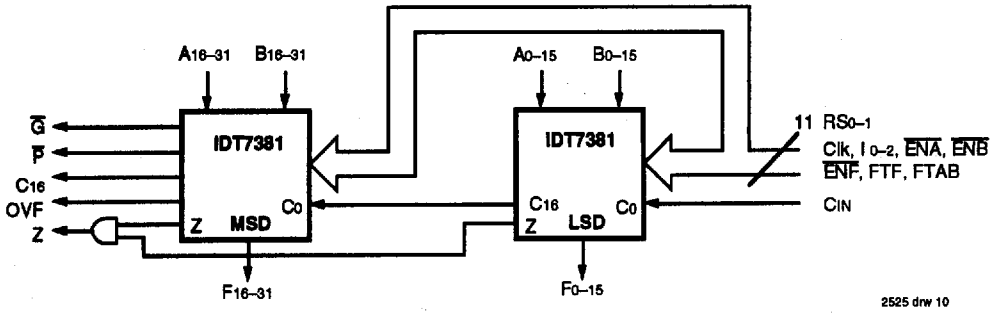

Figure 2. Cascading Two IDT7381s to 32 Bits

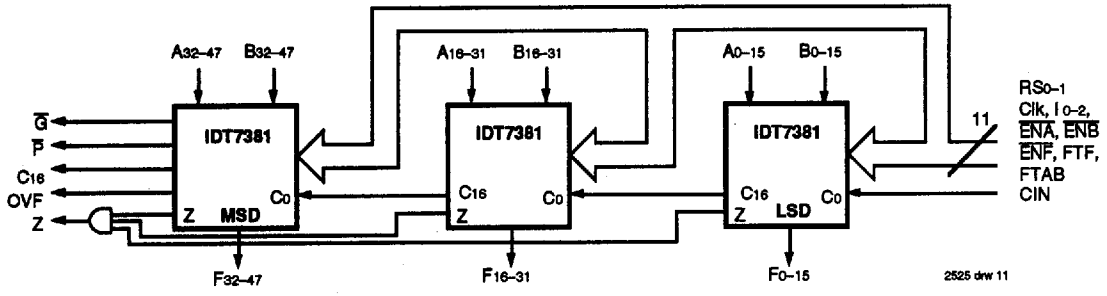

Figure 3. Cascading Three IDT7381s to 48 Bits Wide without a Carry-lookahead Generator

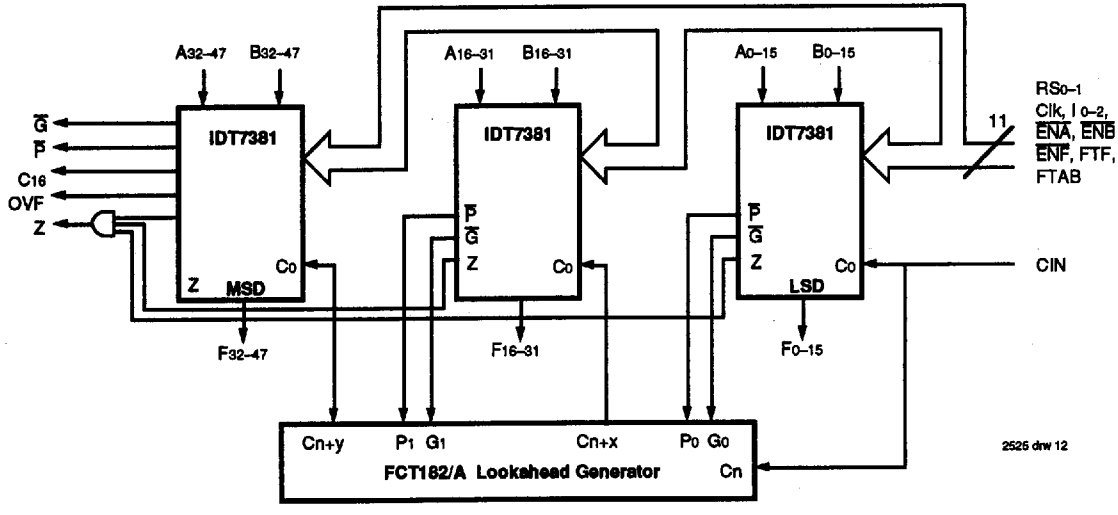

Figure 4. Cascading Three IDT7381s to 48 Bits Wide with a Carry-lookahead Generator

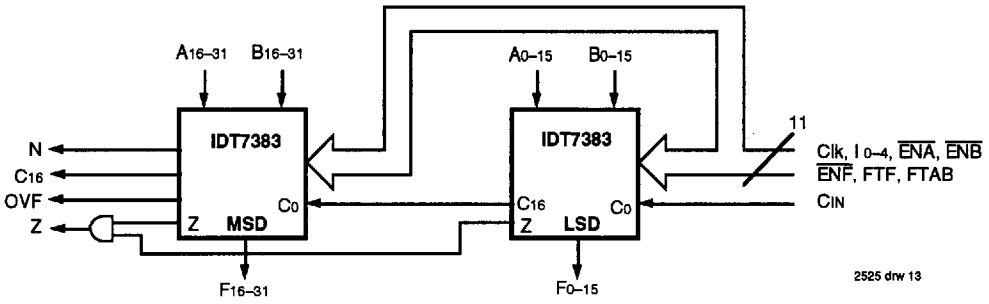

Figure 5. Cascading Two IDT7383s to 32 Bits

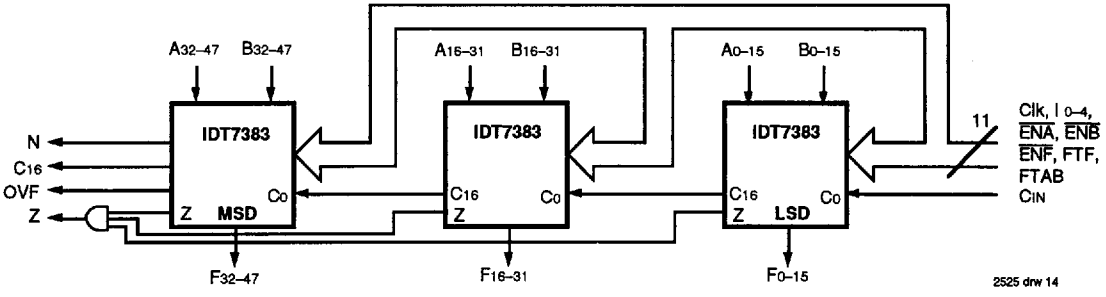

Figure 6. Cascading Three IDT7383s to 48 Bits

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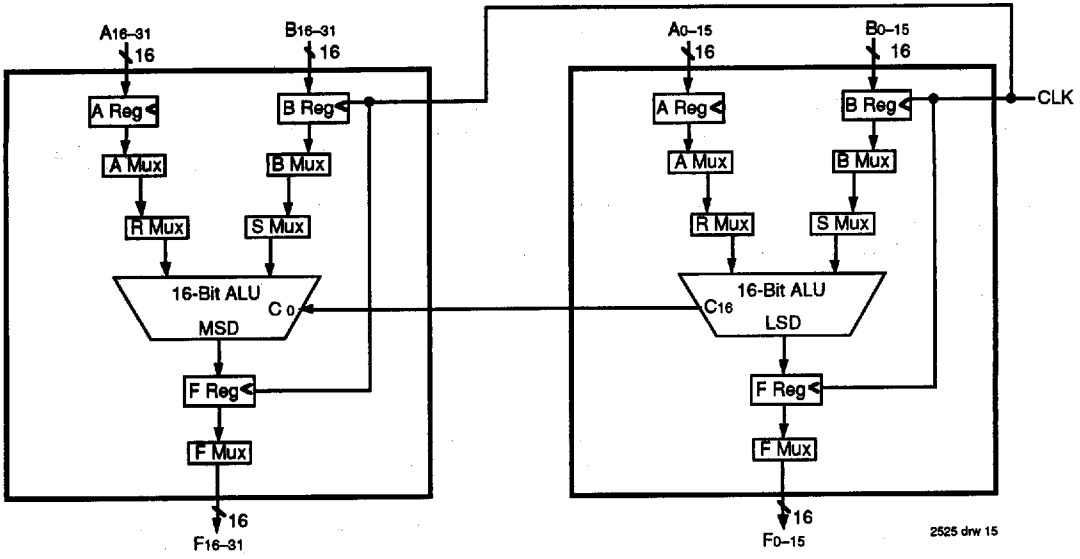

Figure 7. 32-Bit Configuration for FTAB = 0, FTF = 0

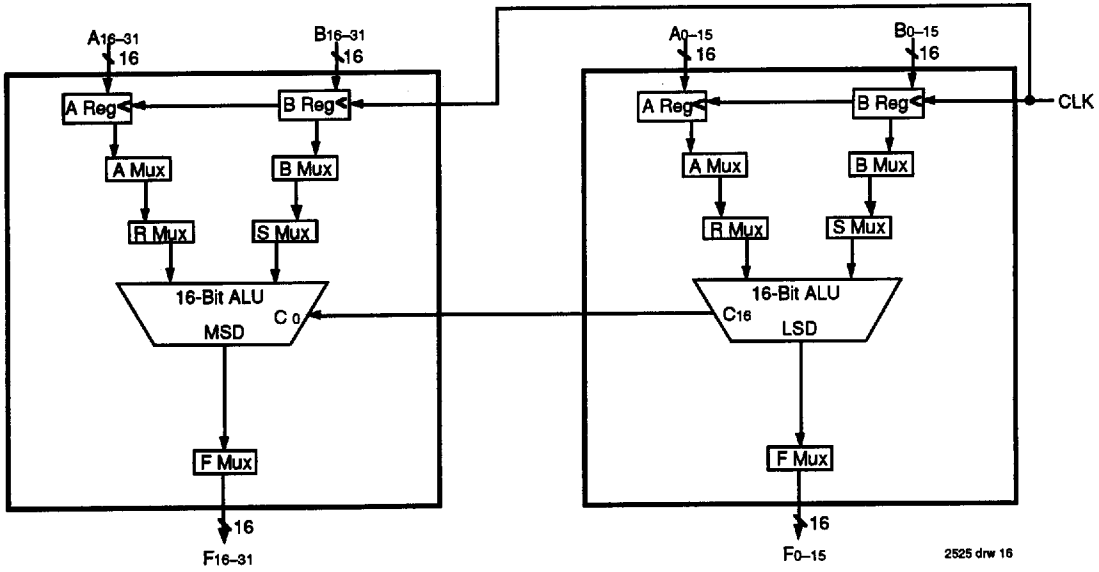

Figure 8. 32-Bit Configuration for FTAB = 0, FTF = 1

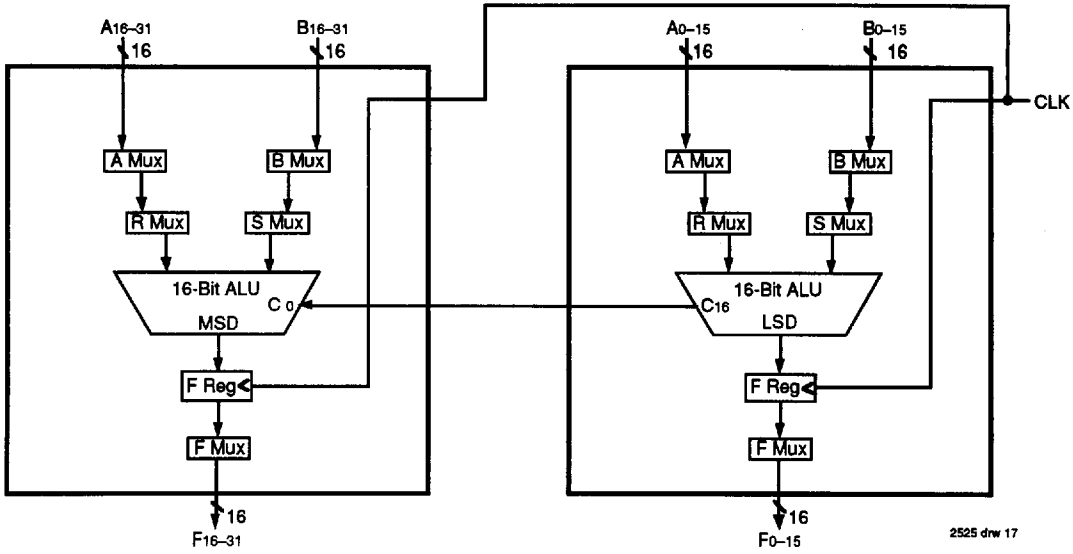

Figure 9. 32-Bit Configuration for FTAB = 1, FTF = 0

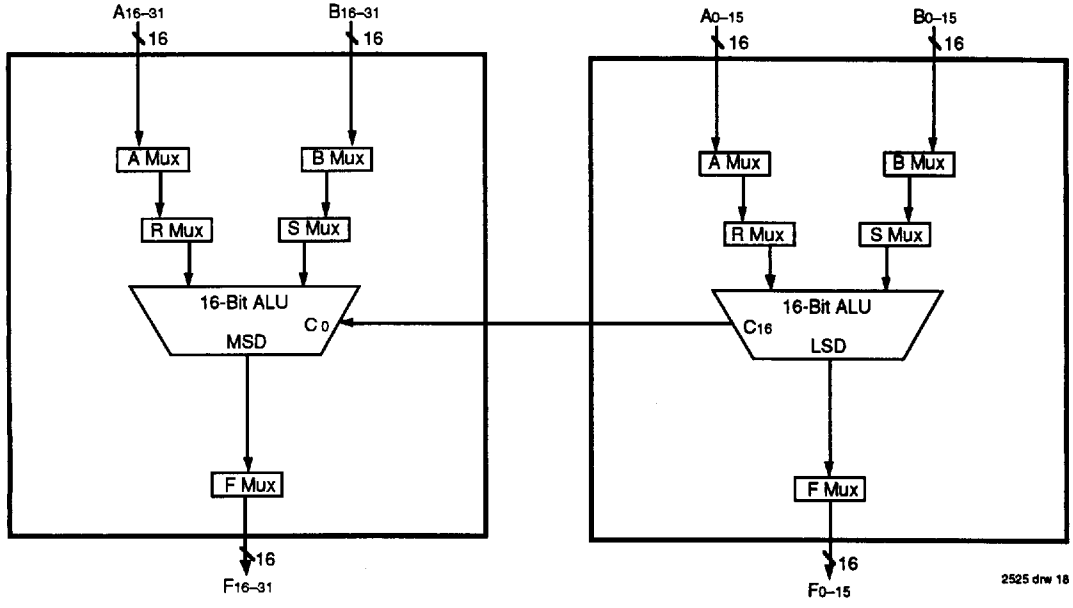

Figure 10. 32-Bit Configuration for FTAB = 1, FTF = 1

8

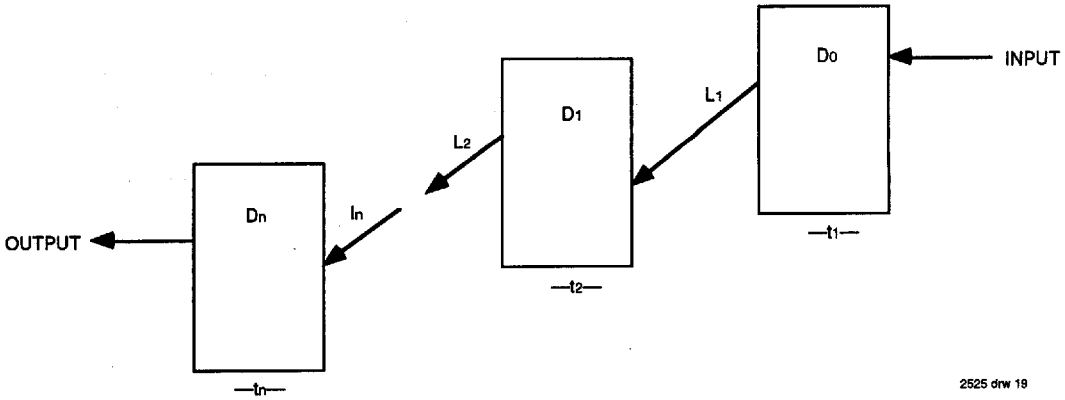

Figure 11. Propagation Delay = t1 + t2 + . . . + tn N-Cascaded Devices