



3.3V CMOS 18-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS

IDT74ALVCF162835A

FEATURES:

- 0.5 MICRON CMOS Technology
- Typical $t_{SK(0)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015;
> 200V using machine model (C = 200pF, R = 0)
- 0.635mm pitch SSOP, 0.50mm pitch TSSOP,
and 0.40mm pitch TVSOP packages
- Extended commercial range of -40°C to $+85^{\circ}\text{C}$
- $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$, Normal Range
- $V_{CC} = 2.7\text{V}$ to 3.6V , Extended Range
- $V_{CC} = 2.5\text{V} \pm 0.2\text{V}$
- CMOS power levels ($0.4\mu\text{W}$ typ. static)
- Rail-to-Rail output swing for increased noise margin

Drive Features for ALVCF162835A:

- Balanced Output Drivers: $\pm 18\text{mA}$
- Low switching noise

APPLICATIONS:

- SDRAM Modules
- PC Motherboards
- Workstations

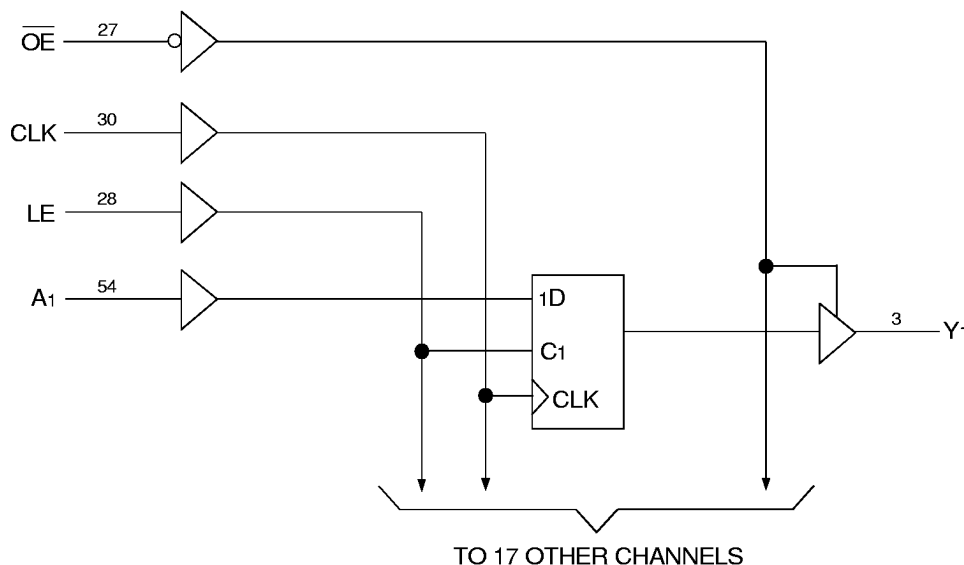
DESCRIPTION:

This 18-bit universal bus driver is built using advanced dual metal CMOS technology. Data flow from A to Y is controlled by the output-enable ($\overline{\text{OE}}$) input. The device operates in the transparent mode when the latch-enable (LE) input is high. The A data is latched if the clock (CLK) input is held at a high or low logic level. If LE is low, the A data is stored in the latch flip-flop on the low-to-high transition of CLK. When $\overline{\text{OE}}$ is high, the outputs are in the high-impedance state.

The ALVCF162835A has series resistors in the device output structure which will reduce switching noise in 128MB and 256MB SDRAM modules. Designed with a drive capability of $\pm 18\text{mA}$, the ALVCF162835A is a mid-way drive between the ALVC162835 ($\pm 12\text{mA}$) and ALVC16835 ($\pm 24\text{mA}$).

The ALVCF162835A is a faster version of the ALVCF162835 or ALVC162835. It is suitable for PC133 applications and particularly SDRAM Modules clocked at 133 MHz.

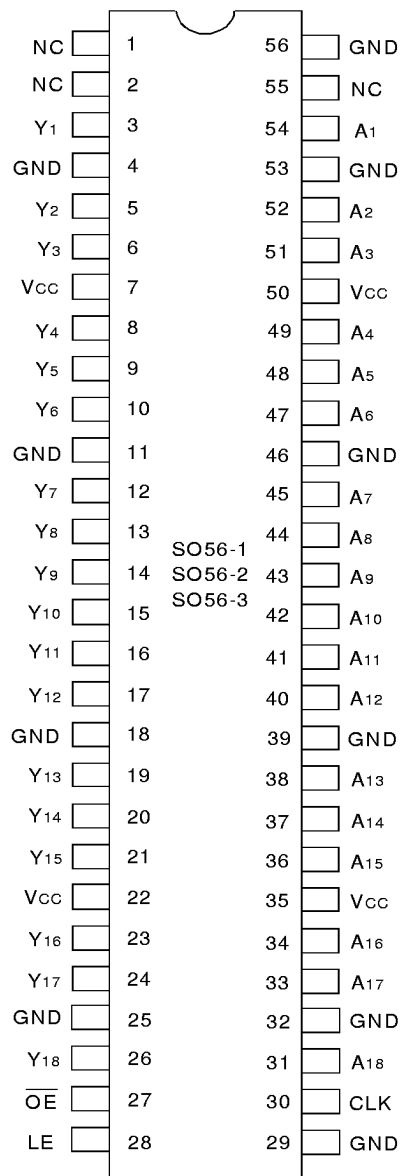
Functional Block Diagram



EXTENDED COMMERCIAL TEMPERATURE RANGE

MAY 1999

PIN CONFIGURATION



SSOP/
TSSOP/ TVSOP
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}$	3-State Output Enable Inputs (Active LOW)
CLK	Register Input Clock
LE	Latch Enable (Transparent HIGH)
Ax	Data Inputs
Yx	3-State Outputs

ABSOLUTE MAXIMUM RATING (1)

Symbol	Description	Max.	Unit
$V_{TERM}^{(2)}$	Terminal Voltage with Respect to GND	- 0.5 to + 4.6	V
$V_{TERM}^{(3)}$	Terminal Voltage with Respect to GND	- 0.5 to $V_{CC} + 0.5$	V
TSTG	Storage Temperature	- 65 to + 150	°C
I _{OUT}	DC Output Current	- 50 to + 50	mA
I _{IK}	Continuous Clamp Current, $V_I < 0$ or $V_I > V_{CC}$	± 50	mA
I _{OK}	Continuous Clamp Current, $V_O < 0$	- 50	mA
I _{CC}	Continuous Current through each V _{CC} or GND	± 100	mA

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NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC} terminals.
- All terminals except V_{CC}.

CAPACITANCE ($T_A = +25^\circ\text{C}$, $f = 1.0\text{MHz}$)

Symbol	Parameter ⁽¹⁾	Conditions	Min.	Typ.	Max.	Unit
C _{IN}	Input Capacitance	$V_{IN} = 0V$	4	5	6	pF
C _{OUT}	Output Capacitance	$V_{OUT} = 0V$	—	7	9	pF
C _{I/O}	I/O Port Capacitance	$V_{IN} = 0V$	—	7	9	pF

NOTE:

- As applicable to the device type.

FUNCTION TABLE⁽¹⁾

Inputs				Outputs
$\overline{OE}$	LE	CLK	Ax	Yx
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H
L	L	H	X	$Y_0^{(2)}$
L	L	L	X	$Y_0^{(3)}$

NOTES:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedance
↑ = LOW-to-HIGH Transition
- Output level before indicated steady-state input conditions were established, provided that CLK is HIGH before LE went LOW.
- Output level before the indicated steady-state input conditions were established.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
V_{IH}	Input HIGH Voltage Level	$V_{CC} = 2.3\text{V}$ to 2.7V		1.7	—	—	V
		$V_{CC} = 2.7\text{V}$ to 3.6V		2	—	—	
V_{IL}	Input LOW Voltage Level	$V_{CC} = 2.3\text{V}$ to 2.7V		—	—	0.7	V
		$V_{CC} = 2.7\text{V}$ to 3.6V		—	—	0.8	
I_{IH}	Input HIGH Current	$V_{CC} = 3.6\text{V}$	$V_I = V_{CC}$	—	—	± 5	μA
I_{IL}	Input LOW Current	$V_{CC} = 3.6\text{V}$	$V_I = \text{GND}$	—	—	± 5	
I_{OZH} I_{OZL}	High Impedance Output Current (3-State Output pins)	$V_{CC} = 3.6\text{V}$	$V_O = V_{CC}$	—	—	± 10	μA
			$V_O = \text{GND}$	—	—	± 10	μA
V_{IK}	Clamp Diode Voltage	$V_{CC} = 2.3\text{V}$, $I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
V_H	Input Hysteresis	$V_{CC} = 3.3\text{V}$		—	100	—	mV
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	$V_{CC} = 3.6\text{V}$ $V_{IN} = \text{GND}$ or V_{CC}		—	0.1	40	μA
ΔI_{CC}	Quiescent Power Supply Current Variation	One input at $V_{CC} - 0.6\text{V}$, other inputs at V_{CC} or GND		—	—	750	μA

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NOTE:1. Typical values are at $V_{CC} = 3.3\text{V}$, $+25^{\circ}\text{C}$ ambient.**OUTPUT DRIVE CHARACTERISTICS**

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	$V_{CC} = 2.3\text{V}$ to 3.6V	$I_{OH} = -0.1\text{mA}$	$V_{CC} - 0.2$	—	V
		$V_{CC} = 2.3\text{V}$	$I_{OH} = -6\text{mA}$	1.9	—	
			$I_{OH} = -8\text{mA}$	1.7	—	
		$V_{CC} = 2.7\text{V}$	$I_{OH} = -6\text{mA}$	2.2	—	
			$I_{OH} = -12\text{mA}$	2	—	
		$V_{CC} = 3.0\text{V}$	$I_{OH} = -8\text{mA}$	2.4	—	
			$I_{OH} = -18\text{mA}$	2	—	
V_{OL}	Output LOW Voltage	$V_{CC} = 2.3\text{V}$ to 3.6V	$I_{OL} = 0.1\text{mA}$	—	0.2	V
		$V_{CC} = 2.3\text{V}$	$I_{OL} = 6\text{mA}$	—	0.4	
			$I_{OL} = 8\text{mA}$	—	0.55	
		$V_{CC} = 2.7\text{V}$	$I_{OL} = 6\text{mA}$	—	0.4	
			$I_{OL} = 12\text{mA}$	—	0.6	
		$V_{CC} = 3.0\text{V}$	$I_{OL} = 8\text{mA}$	—	0.55	
			$I_{OL} = 18\text{mA}$	—	0.8	

NOTE:1. V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$.

OPERATING CHARACTERISTICS, $T_A = 25^\circ\text{C}$

Symbol	Parameter	Test Conditions	Vcc = 2.5V $\pm$ 0.2V	Vcc = 3.3V $\pm$ 0.3V	Unit
			Typical	Typical	
CPD	Power Dissipation Capacitance Outputs enabled	CL = 0pF, f = 10Mhz	30	35	pF
CPD	Power Dissipation Capacitance Outputs disabled		12.5	14	pF

SWITCHING CHARACTERISTICS⁽¹⁾

Symbol	Parameter	Vcc = 2.5V $\pm$ 0.2V		Vcc = 2.7V		Vcc = 3.3V $\pm$ 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
fCLOCK		150	—	150	—	150	—	MHz
tPLH tPHL	Propagation Delay Ax to Yx	1	4	—	4.6	1	3.5	ns
tPLH tPHL	Propagation Delay LE to Yx	1.3	5.5	—	5.4	1.3	4.6	ns
tPLH tPHL	Propagation Delay CLK to Yx	1.4	5.9	—	5.6	1.4	3.5	ns
tpZH tpZL	Output Enable Time $\overline{\text{OE}}$ to Yx	1.4	5.9	—	6	1.1	5	ns
tpHZ tpLZ	Output Disable Time $\overline{\text{OE}}$ to Yx	1	4.7	—	4.6	1.3	4.2	ns
tw	Pulse Duration, LE HIGH	3.3	—	3.3	—	3.3	—	ns
tw	Pulse Duration, CLK HIGH or LOW	3.3	—	3.3	—	3.3	—	ns
tsu	Setup Time, data before CLK $\uparrow$	1.8	—	1.5	—	1	—	ns
tsu	Setup Time, data before LE $\downarrow$, CLK HIGH	1.9	—	1.6	—	1.5	—	ns
tsu	Setup Time, data before LE $\downarrow$, CLK LOW	1.3	—	1.1	—	1	—	ns
th	Hold Time, data after CLK $\uparrow$	0.6	—	0.6	—	0.6	—	ns
th	Hold Time, data after LE $\downarrow$, CLK HIGH or LOW	1.4	—	1.7	—	1.4	—	ns
tSK(o)	Output Skew ⁽²⁾	—	—	—	—	—	500	ps

NOTES:

1. See test circuits and waveforms. $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.
2. Skew between any two outputs of the same package and switching in the same direction.

SWITCHING CHARACTERISTICS FROM 0°C TO 65°C , CL = 50pF

Symbol	Parameter	Vcc = 3.3V $\pm$ 0.15V		Unit
		Min.	Max.	
tPLH tPHL	Propagation Delay CLK to Yx	1.8	3.5	ns

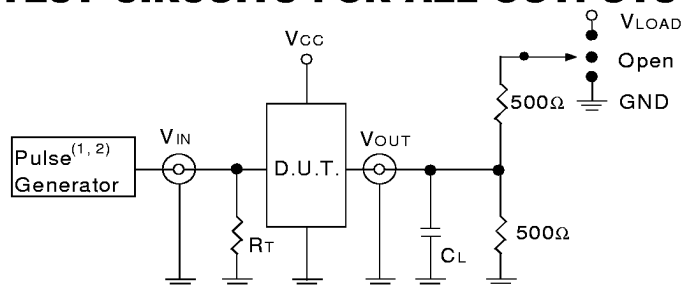
TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	Vcc(1) = 3.3V±0.3V	Vcc(1) = 2.7V	Vcc(2) = 2.5V±0.2V	Unit
V _{LOAD}	6	6	2 x V _{cc}	V
V _{IH}	2.7	2.7	V _{cc}	V
V _T	1.5	1.5	V _{cc} / 2	V
V _{LZ}	300	300	150	mV
V _{HZ}	300	300	150	mV
C _L	50	50	30	pF

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TEST CIRCUITS FOR ALL OUTPUTS



DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

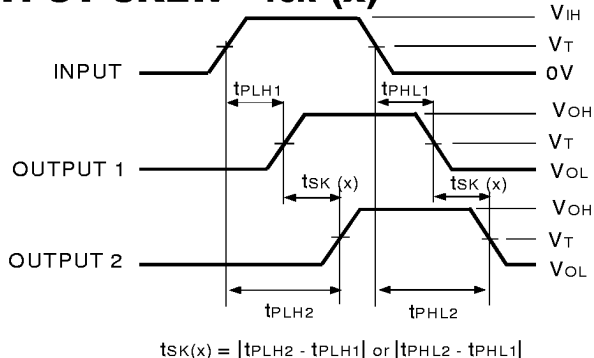
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other tests	Open

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OUTPUT SKEW - t_{SK} (x)

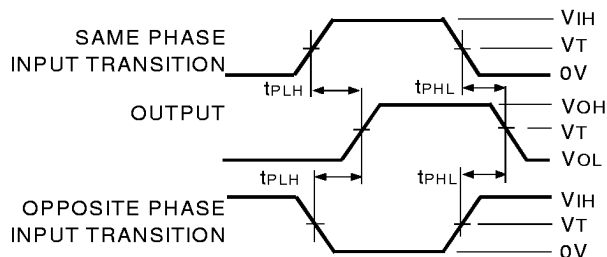


ALVC Link

NOTES:

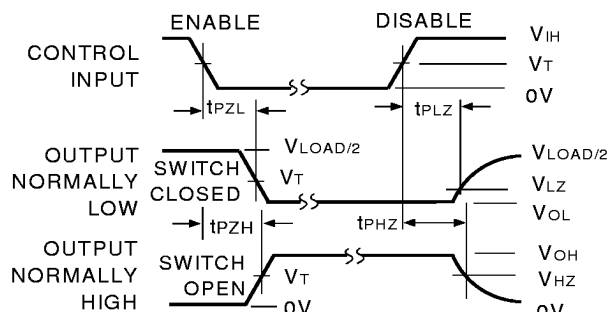
1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.

PROPAGATION DELAY



ALVC Link

ENABLE AND DISABLE TIMES

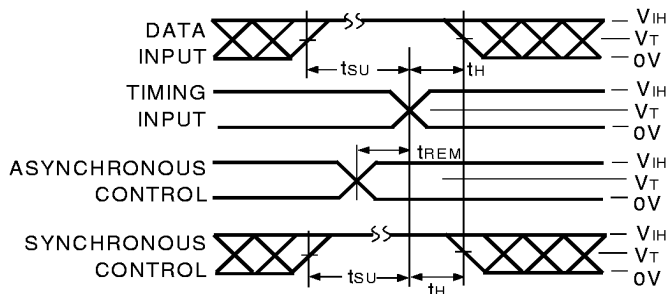


ALVC Link

NOTE:

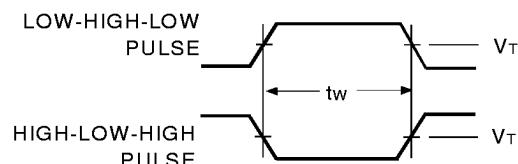
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES



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PULSE WIDTH



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ORDERING INFORMATION

IDT	XX	ALVC	X	XXX	XXX	XX	
	Temp. Range		Bus-Hold	Family	Device Type	Package	
						PV	Shrink Small Outline Package (SO56-1)
						PA	Thin Shrink Small Outline Package (SO56-2)
						PF	Thin Very Small Outline Package (SO56-3)
						835	18-Bit Universal Bus Driver with 3-State Outputs
						F162	Double-Density with Resistors, $\pm 18\text{mA}$
						Blank	No Bus-hold
						74	-40°C to $+85^{\circ}\text{C}$

**CORPORATE HEADQUARTERS**

2975 Stender Way
Santa Clara, CA 95054

for SALES:

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fax: 408-492-8674
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