



3.3V CMOS 18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS AND BUS-HOLD

IDT74ALVCH162601

FEATURES:

- 0.5 MICRON CMOS Technology
- Typical $t_{SK(0)}$ (Output Skew) < 250ps
- ESD > 2000V per MIL-STD-883, Method 3015;
> 200V using machine model (C = 200pF, R = 0)
- 0.635mm pitch SSOP, 0.50mm pitch TSSOP,
and 0.40mm pitch TVSOP packages
- Extended commercial range of -40°C to $+85^{\circ}\text{C}$
- $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$, Normal Range
- $V_{CC} = 2.7\text{V}$ to 3.6V , Extended Range
- $V_{CC} = 2.5\text{V} \pm 0.2\text{V}$
- CMOS power levels ($0.4\mu\text{W}$ typ. static)
- Rail-to-Rail output swing for increased noise margin

Drive Features for ALVCH162601:

- High Output Drivers: $\pm 24\text{mA}$ (A port)
- Balanced Output Drivers: $\pm 12\text{mA}$ (B port)

APPLICATIONS:

- 3.3V High Speed Systems
- 3.3V and lower voltage computing systems

DESCRIPTION:

This 18-bit universal bus transceiver is built using advanced dual metal CMOS technology. The ALVCH162601 combines D-type latches

and D-type flip-flops to allow data flow in transparent, latched, clocked, and clock-enabled modes.

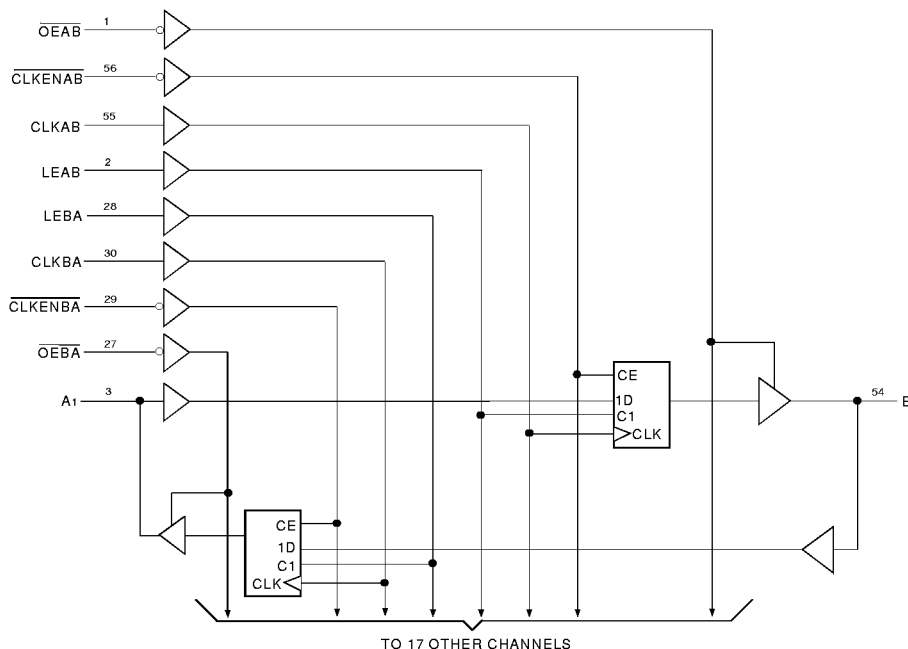
Data flow in each direction is controlled by output-enable ($\overline{\text{OEAB}}$ and $\overline{\text{OEBA}}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. The clock can be controlled by the clock-enable ($\overline{\text{CLKENAB}}$ and $\overline{\text{CLKENBA}}$) inputs. For A-to-B data flow, the device operates in the transparent mode when LEAB is high. When LEAB is low, the A data is latched if CLKAB is held at a high or low logic level. If LEAB is low, the data is stored in the latch/flip-flop on the low-to-high transition of CLKAB. When $\overline{\text{OEAB}}$ is low, the outputs are active. When $\overline{\text{OEAB}}$ is high, the outputs are in the high-impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{\text{OEBA}}$, LEBA, CLKBA and $\overline{\text{CLKENBA}}$.

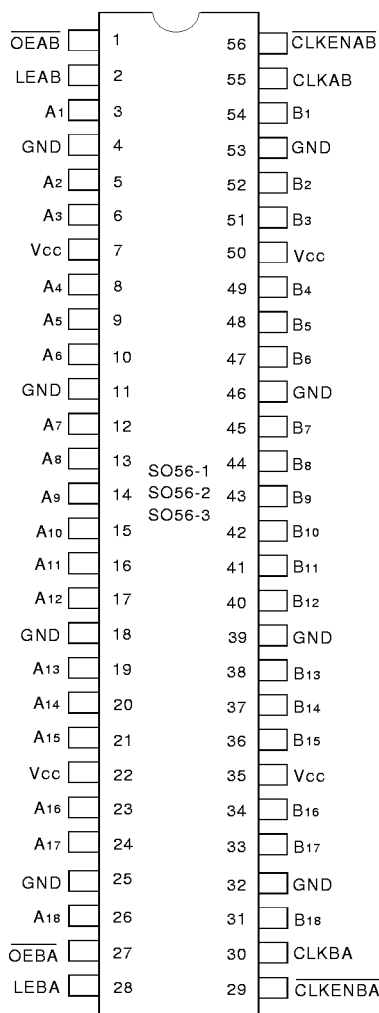
The ALVCH162601 has series resistors in the device output structure of the "B" port which will significantly reduce line noise when used with light loads. This driver has been designed to drive $\pm 12\text{mA}$ at the designated threshold levels. The "A" port has a $\pm 24\text{mA}$ driver.

The ALVCH162601 has "bus-hold" which retains the inputs' last state whenever the input goes to a high impedance. This prevents floating inputs and eliminates the need for pull-up/down resistors.

Functional Block Diagram



PIN CONFIGURATION



SSOP/
TSSOP/TVSOP
TOP VIEW

PIN DESCRIPTION

Pin Names	Description
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
Ax	A-to-B Data Inputs or B-to-A 3-State Outputs ⁽¹⁾
Bx	B-to-A Data Inputs or A-to-B 3-State Outputs ⁽¹⁾
$\overline{CLKENAB}$	A-to-B Clock Enable Input (Active LOW)
$\overline{CLKENBA}$	B-to-A Clock Enable Input (Active LOW)

NOTE:

- These pins have "Bus-Hold." All other pins are standard inputs, outputs, or I/Os.

ABSOLUTE MAXIMUM RATING (1)

Symbol	Description	Max.	Unit
$V_{TERM}^{(2)}$	Terminal Voltage with Respect to GND	- 0.5 to + 4.6	V
$V_{TERM}^{(3)}$	Terminal Voltage with Respect to GND	- 0.5 to $V_{CC} + 0.5$	V
TSTG	Storage Temperature	- 65 to + 150	°C
I _{OUT}	DC Output Current	- 50 to + 50	mA
I _{IK}	Continuous Clamp Current, $V_I < 0$ or $V_I > V_{CC}$	± 50	mA
I _{OK}	Continuous Clamp Current, $V_O < 0$	- 50	mA
I _{CC}	Continuous Current through each V _{CC} or GND	± 100	mA

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NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC} terminals.
- All terminals except V_{CC}.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	5	7	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	7	9	pF
C _{I/O}	I/O Port Capacitance	V _{IN} = 0V	7	9	pF

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NOTE:

- As applicable to the device type.

FUNCTION TABLE(1, 2)

Inputs					Outputs
$\overline{CLKENAB}$	$\overline{OEAB}$	LEAB	CLKAB	Ax	Bx
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B ₀
H	L	L	X	X	B ₀
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	L	L or H	X	B ₀

NOTES:

- A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, CLKBA and $\overline{CLKENBA}$.
- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High-Impedance
↑ = LOW-to-HIGH Transition
B₀ = Output level before the indicated steady-state input conditions were established

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition: TA = – 40°C to +85°C

Symbol	Parameter	Test Conditions		Min.	Typ. ⁽¹⁾	Max.	Unit
VIH	Input HIGH Voltage Level	VCC = 2.3V to 2.7V		1.7	—	—	V
		VCC = 2.7V to 3.6V		2	—	—	
VIL	Input LOW Voltage Level	VCC = 2.3V to 2.7V		—	—	0.7	V
		VCC = 2.7V to 3.6V		—	—	0.8	
IiH	Input HIGH Current	VCC = 3.6V	VI = VCC	—	—	± 5	μA
IiL	Input LOW Current	VCC = 3.6V	VI = GND	—	—	± 5	
IoZH	High Impedance Output Current (3-State Output pins)	VCC = 3.6V	VO = VCC	—	—	± 10	μA
			VO = GND	—	—	± 10	μA
VIK	Clamp Diode Voltage	VCC = 2.3V, IIN = – 18mA		—	– 0.7	– 1.2	V
VH	Input Hysteresis	VCC = 3.3V		—	100	—	mV
IcCL	Quiescent Power Supply Current	VCC = 3.6V		—	0.1	40	μA
IcCH		VIN = GND or VCC					
IcCZ							
ΔIcc	Quiescent Power Supply Current Variation	One input at VCC – 0.6V, other inputs at VCC or GND		—	—	750	μA

NOTE:

1. Typical values are at VCC = 3.3V, +25°C ambient.

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BUS-HOLD CHARACTERISTICS

Symbol	Parameter ⁽¹⁾	Test Conditions		Min.	Typ. ⁽²⁾	Max.	Unit
IBHH	Bus-Hold Input Sustain Current	VCC = 3.0V	VI = 2.0V	– 75	—	—	μA
IBHL			VI = 0.8V	75	—	—	
IBHH	Bus-Hold Input Sustain Current	VCC = 2.3V	VI = 1.7V	– 45	—	—	μA
IBHL			VI = 0.7V	45	—	—	
IBHHO	Bus-Hold Input Overdrive Current	VCC = 3.6V	VI = 0 to 3.6V	—	—	± 500	μA
IBHLO							

NOTES:

1. Pins with Bus-hold are identified in the pin description.
2. Typical values are at VCC = 3.3V, +25°C ambient.

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OUTPUT DRIVE CHARACTERISTICS (A PORT)

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = 2.3V to 3.6V	I _{OH} = −0.1mA	V _{CC} − 0.2	—	V
		V _{CC} = 2.3V	I _{OH} = −6mA	2	—	
		V _{CC} = 2.3V	I _{OH} = −12mA	1.7	—	
		V _{CC} = 2.7V		2.2	—	
		V _{CC} = 3.0V		2.4	—	
		V _{CC} = 3.0V	I _{OH} = −24mA	2	—	
V _{OL}	Output LOW Voltage	V _{CC} = 2.3V to 3.6V	I _{OL} = 0.1mA	—	0.2	V
		V _{CC} = 2.3V	I _{OL} = 6mA	—	0.4	
			I _{OL} = 12mA	—	0.7	
		V _{CC} = 2.7V	I _{OL} = 12mA	—	0.4	
		V _{CC} = 3.0V	I _{OL} = 24mA	—	0.55	

NOTE:

- V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = −40°C to +85°C.

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OUTPUT DRIVE CHARACTERISTICS (B PORT)

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} = 2.3V to 3.6V	I _{OH} = −0.1mA	V _{CC} − 0.2	—	V
		V _{CC} = 2.3V	I _{OH} = −4mA	1.9	—	
			I _{OH} = −6mA	1.7	—	
		V _{CC} = 2.7V	I _{OH} = −4mA	2.2	—	
			I _{OH} = −8mA	2	—	
		V _{CC} = 3.0V	I _{OH} = −6mA	2.4	—	
			I _{OH} = −12mA	2	—	
V _{OL}	Output LOW Voltage	V _{CC} = 2.3V to 3.6V	I _{OL} = 0.1mA	—	0.2	V
		V _{CC} = 2.3V	I _{OL} = 4mA	—	0.4	
			I _{OL} = 6mA	—	0.55	
		V _{CC} = 2.7V	I _{OL} = 4mA	—	0.4	
			I _{OL} = 8mA	—	0.6	
		V _{CC} = 3.0V	I _{OL} = 6mA	—	0.55	
			I _{OL} = 12mA	—	0.8	

NOTE:

- V_{IH} and V_{IL} must be within the min. or max. range shown in the DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE table for the appropriate V_{CC} range. T_A = −40°C to +85°C.

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OPERATING CHARACTERISTICS, $T_A = 25^\circ\text{C}$

Symbol	Parameter	Test Conditions	Vcc = 2.5V ± 0.2V	Vcc = 3.3V ± 0.3V	Unit
			Typical	Typical	
CPD	Power Dissipation Capacitance Outputs enabled	CL = 0pF, f = 10MHz	41	50	pF
CPD	Power Dissipation Capacitance Outputs disabled		6	6	pF

SWITCHING CHARACTERISTICS (A AND B PORTS)⁽¹⁾

Symbol	Parameter	Vcc = 2.5V ± 0.2V		Vcc = 2.7V		Vcc = 3.3V ± 0.3V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
fMAX		140	—	150	—	150	—	MHz
tPLH tPHL	Propagation Delay Ax to Bx	1.3	4.8	—	5.2	1.6	4.5	ns
tPLH tPHL	Propagation Delay Bx to Ax	1	4.3	—	4.6	1	4.1	ns
tPLH tPHL	Propagation Delay LEAB to Bx	1	5.5	—	5.9	1.5	5.1	ns
tPLH tPHL	Propagation Delay LEBA to Ax	1	5	—	5.3	1	4.7	ns
tPLH tPHL	Propagation Delay CLKAB to Bx	1.5	6.1	—	6.3	1.6	5.5	ns
tPLH tPHL	Propagation Delay CLKBA to Ax	1.3	5.6	—	5.8	1.4	5	ns
tPZH tPZL	Output Enable Time OEAB to Bx	1.6	6.1	—	6.7	1.6	5.7	ns
tPZH tPZL	Output Enable Time OEBA to Ax	1.1	5.5	—	6.1	1.1	5.2	ns
tPHZ tPLZ	Output Disable Time OEAB to Bx	1.8	5.7	—	5.3	1.8	4.8	ns
tPHZ tPLZ	Output Disable Time OEBA to Ax	1.3	5.2	—	4.8	1.6	4.4	ns
tsu	Setup Time, data before CLK↑	2.3	—	2.4	—	2.1	—	ns
tsu	Setup Time, data before LE↓, CLK HIGH	2	—	1.6	—	1.6	—	ns
tsu	Setup Time, data before LE↓, CLK LOW	1.3	—	1.2	—	1.1	—	ns
tsu	Setup Time, $\overline{\text{CLKEN}}$ before CLK↑	2	—	2	—	1.7	—	ns
th	Hold Time, data after CLK↑	0.7	—	0.7	—	0.8	—	ns
th	Hold Time, data after LE↓, CLK HIGH	1.3	—	1.6	—	1.4	—	ns
th	Hold Time, data after LE↓, CLK LOW	1.7	—	2	—	1.7	—	ns
th	Hold Time, $\overline{\text{CLKEN}}$ after CLK↑	0.3	—	0.5	—	0.6	—	ns
tw	Pulse Width, LE HIGH	3.3	—	3.3	—	3.3	—	ns
tw	Pulse Width, CLK HIGH or LOW	3.3	—	3.3	—	3.3	—	ns
tsk(o)	Output Skew ⁽²⁾	—	—	—	—	—	500	ps

NOTES:

- See test circuits and waveforms. $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.
- Skew between any two outputs of the same package and switching in the same direction.

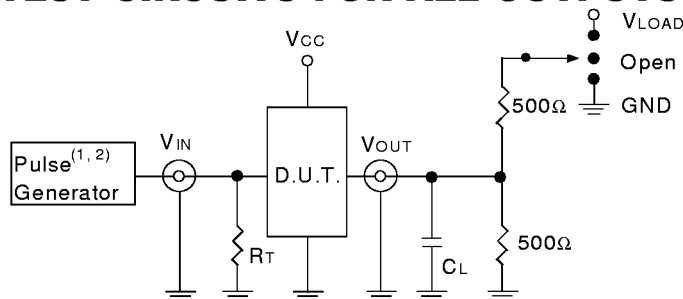
TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	V _{CC} (1)= 3.3V±0.3V	V _{CC} (1)= 2.7V	V _{CC} (2)= 2.5V±0.2V	Unit
V _{LOAD}	6	6	2 x V _{CC}	V
V _{IH}	2.7	2.7	V _{CC}	V
V _T	1.5	1.5	V _{CC} / 2	V
V _{LZ}	300	300	150	mV
V _{HZ}	300	300	150	mV
C _L	50	50	30	pF

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TEST CIRCUITS FOR ALL OUTPUTS



DEFINITIONS:

C_L = Load capacitance; includes jig and probe capacitance.
R_T = Termination resistance; should be equal to Z_{OUT} of the Pulse Generator.

NOTES:

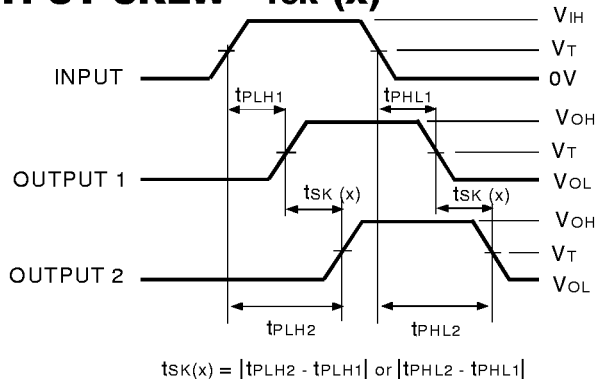
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	V _{LOAD}
Disable High Enable High	GND
All Other tests	Open

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OUTPUT SKEW - t_{SK} (x)



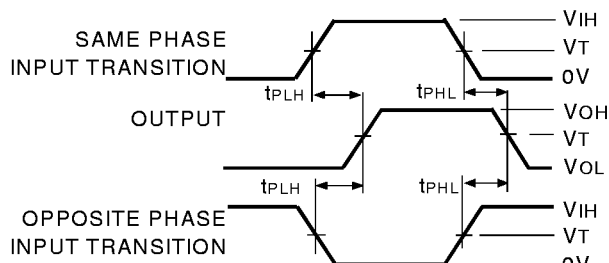
$$t_{SK}(x) = |t_{PLH2} - t_{PLH1}| \text{ or } |t_{PHL2} - t_{PHL1}|$$

ALVC Link

NOTES:

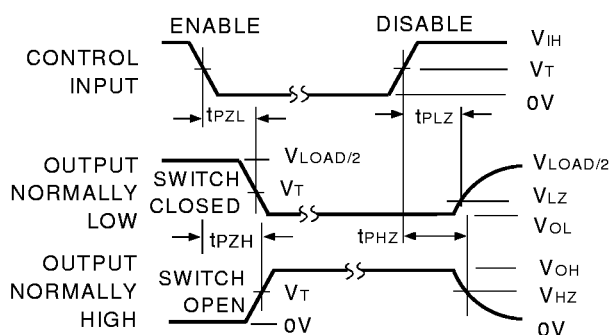
1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.

PROPAGATION DELAY



ALVC Link

ENABLE AND DISABLE TIMES

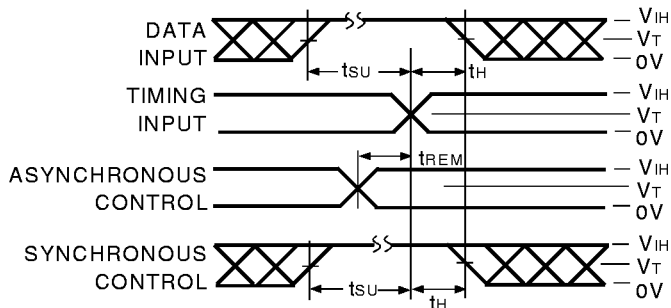


ALVC Link

NOTE:

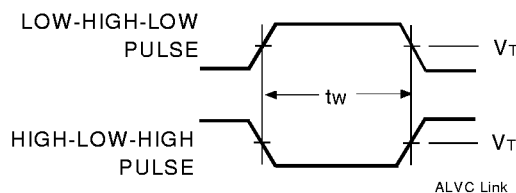
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

SET-UP, HOLD, AND RELEASE TIMES



ALVC Link

PULSE WIDTH



ALVC Link

ORDERING INFORMATION

IDT	XX	ALVC	X	XX	XXX	XX	
	Temp. Range		Bus-Hold	Family	Device Type	Package	
						PV	Shrink Small Outline Package (SO56-1)
						PA	Thin Shrink Small Outline Package (SO56-2)
						PF	Thin Very Small Outline Package (SO56-3)
					601		18-Bit Universal Bus Transceiver with 3-State Outputs
					162		Double-Density with Resistors, $\pm 24\text{mA}$ (A port) $\pm 12\text{mA}$ (B port)
					H		Bus-Hold
					74		-40°C to $+85^{\circ}\text{C}$



CORPORATE HEADQUARTERS
 2975 Stender Way
 Santa Clara, CA 95054

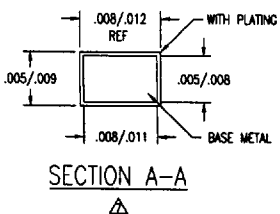
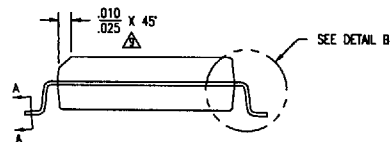
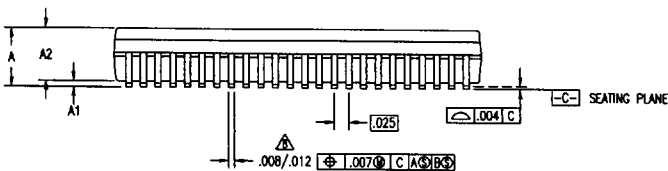
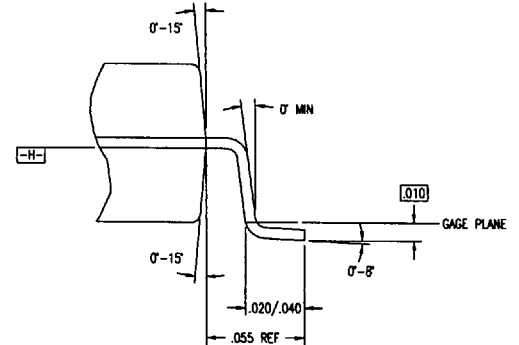
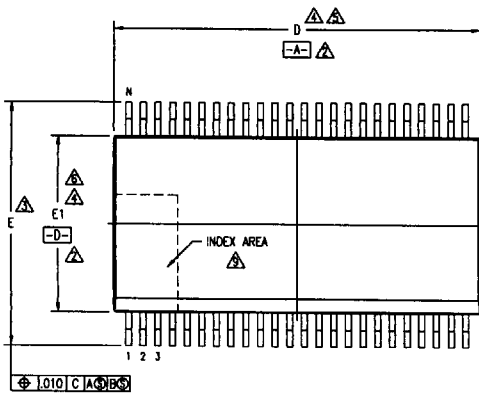
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PACKAGE DIAGRAM OUTLINES

SSOP

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
17893	00	INITIAL RELEASE	07/15/90	A. FUNCELL
22377	01	REMOVE CHAMFER FROM PACKAGE	04/15/92	T. VU
27492	02	REDRAW TO JEDEC FORMAT	02/01/95	



TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc.	
DECIMAL	ANGULAR	2075 Slender Way, Santa Clara, CA 95054	
XXX	±	PHONE: (408) 727-8118	
XXXS		FAX: (408) 482-8874	
XXXSS		TWC: 910-338-2070	
APPROVALS	DATE	TITLE	REV
DRAWN	08/15/90	PV PACKAGE OUTLINE	02
CHECKED		.300" BODY WIDTH SSOP	
		.025" PITCH	
		SIZE	
		C	
		DRAWING No.	
		PSC-4029	
DO NOT SCALE DRAWING			

PACKAGE DIAGRAM OUTLINES

SSOP (Continued)

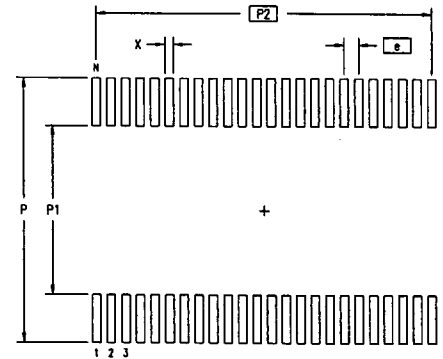
SYMBOL	DWG # S048-1			NOTE	DWG # S056-1			NOTE
	JEDEC VARIATION				JEDEC VARIATION			
	AA				AB			
	MIN	NOM	MAX		MIN	NOM	MAX	
A	.095	.102	.110		.095	.102	.110	
A1	.008	.012	.016		.008	.012	.016	
A2	.088	.090	.092		.088	.090	.092	
D	.620	.625	.630	4,5	.720	.725	.730	4,5
E	.395	.405	.420	3	.395	.405	.420	3
E1	.291	.295	.299	4,6	.291	.295	.299	4,6
N	48				56			

NOTES:

- ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
- DATUMS **-A-** AND **-B-** TO BE DETERMINED AT DATUM PLANE **-H-**
- DIMENSION E TO BE DETERMINED AT SEATING PLANE **-C-**
- DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE **-H-**
- DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 PER SIDE
- DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .015 PER SIDE
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND .010 FROM LEAD TIP
- LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .004 IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT
- THE CHAMFER ON THE PACKAGE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE ZONE INDICATED
- ALL DIMENSIONS ARE IN INCHES
- THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-118, VARIATION AA & AB

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
17893	00	INITIAL RELEASE	07/15/90	A. FUNCELL
22377	01	REMOVE CHAMFER FROM PACKAGE	04/15/92	T. WJ
27492	02	REDRAW TO JEDEC FORMAT	02/01/95	

LAND PATTERN DIMENSIONS



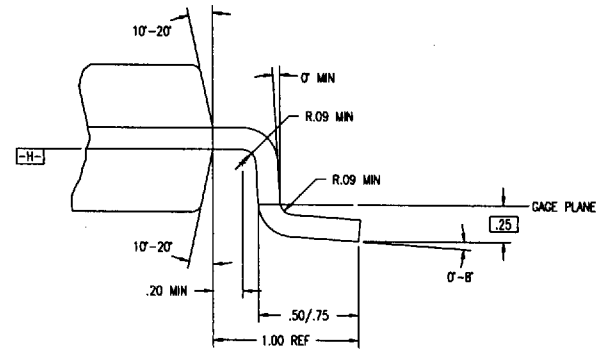
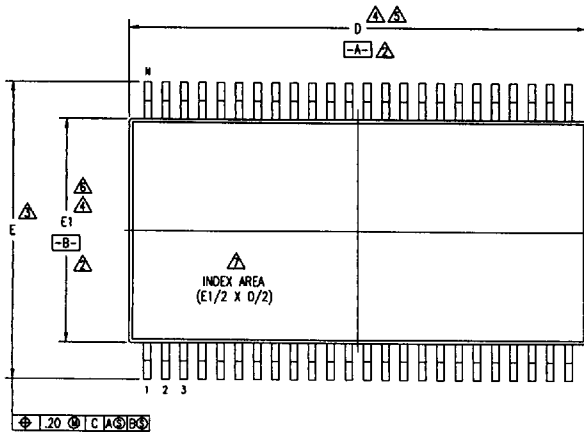
	MIN	MAX	MIN	MAX
P	.450	.458	.450	.458
P1	.282	.290	.282	.290
P2	.575 BSC		.675 BSC	
X	.010	.018	.010	.018
e	.025 BSC		.025 BSC	
N	48		56	

TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc.	
DECIMAL	ANGULAR	2075 Stoner Way, Santa Clara, CA 95054	
X.XX	±	PHONE: (408) 727-8116	
X.XXX	±	FAX: (408) 482-8874	
X.XXXX	±	TW: 810-338-2070	
APPROVALS	DATE	TITLE	REV
DRN	06/15/90	PV PACKAGE OUTLINE	
CHECKED		.300" BODY WIDTH SSOP	
		.025" PITCH	
		SIZE	REV
		C	02
		DRAWING No.	
		PSC-4029	
		DO NOT SCALE DRAWING	

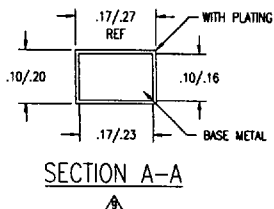
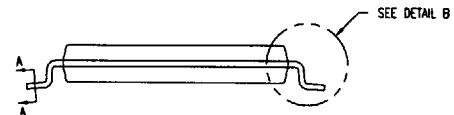
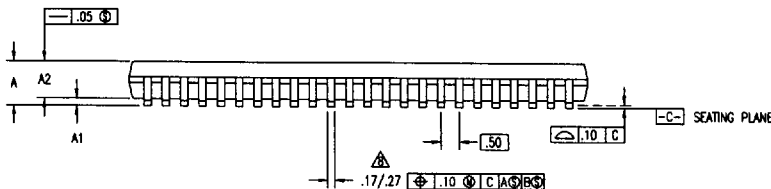
PACKAGE DIAGRAM OUTLINES

TSSOP

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
23757	00	INITIAL RELEASE	02/15/93	T. VU
26315	01	CHANGE DIMS A1 & A2	05/18/94	DG
26490	02	CHANGE DIM A1	07/21/94	T. VU
27494	03	REDRAW TO JEDEC FORMAT	03/08/95	



DETAIL B



TOLERANCES UNLESS SPECIFIED			Integrated Device Technology, Inc. 2975 Slender Way, Santa Clara, CA 95054 PHONE: (408) 727-8118 FAX: (408) 492-8674 TWC 910-336-2070	
DECIMAL	ANGULAR			
XXX.X	±			
XXXX.X				
XXXXX.X				
APPROVALS	DATE	TITLE PA PACKAGE OUTLINE		
DRAWN <i>add</i>	01/15/93	6.10 mm BODY WIDTH TSSOP		
CHECKED		.50 mm PITCH		
		SIZE	DRAWING No.	REV
		C	PSC-4039	03
DO NOT SCALE DRAWING				

PACKAGE DIAGRAM OUTLINES TSSOP (Continued)

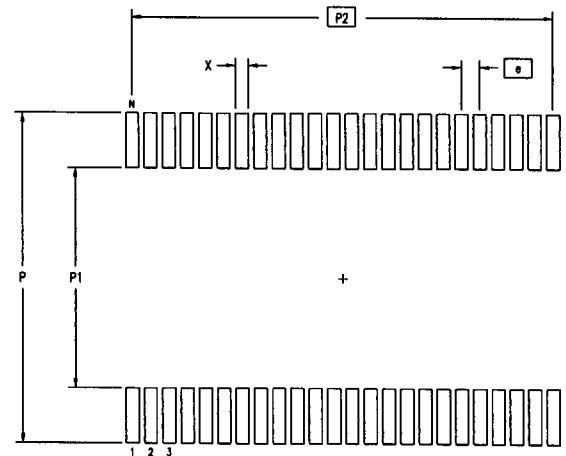
SYMBOL	DWG #		S048-2		NOTE	DWG #		S056-2		NOTE
	JEDEC VARIATION					JEDEC VARIATION				
	ED					EE				
	MIN	NOM	MAX			MIN	NOM	MAX		
A	—	—	1.10		—	—	1.10			
A1	.05	—	.15		.05	—	.15			
A2	.85	1.00	1.05		.85	1.00	1.05			
D	12.40	12.50	12.60	4,5	13.90	14.00	14.10	4,5		
E	7.95	8.10	8.25	3	7.95	8.10	8.25	3		
E1	6.00	6.10	6.20	4,6	6.00	6.10	6.20	4,6		
N	48					56				

NOTES:

- ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
- DATUMS $\square$ -A- and $\square$ -B- TO BE DETERMINED AT DATUM PLANE $\square$ -H-
- DIMENSION E TO BE DETERMINED AT SEATING PLANE $\square$ -C-
- DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE $\square$ -H-
- DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED .15 mm PER SIDE
- DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .25 mm PER SIDE
- DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
- LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .08 mm IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .10 AND .25 mm FROM THE LEAD TIP
- ALL DIMENSIONS ARE IN MILLIMETERS
- THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MQ-153, VARIATION ED & EE

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
23757	00	INITIAL RELEASE	02/15/93	T. VU
26315	01	CHANGE DIMS A1 & A2	05/18/94	DG
26490	02	CHANGE DIM A1	07/21/94	T. VU
27494	03	REDRAW TO JEDEC FORMAT	03/08/95	

LAND PATTERN DIMENSIONS



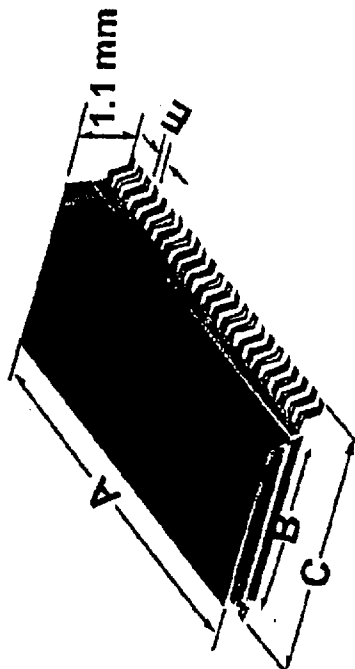
	MIN	MAX	MIN	MAX
P	8.90	9.10	8.90	9.10
P1	5.90	6.10	5.90	6.10
P2	11.50	BSC	13.50	BSC
X	.30	.40	.30	.40
e	.50	BSC	.50	BSC
N	48		56	

TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc. 2975 Slender Way, Santa Clara, CA 95054 PHONE: (408) 727-8118 FAX: (408) 482-8874 TWC: 910-338-2070	
DECIMAL	ANGULAR		
XXX.X	±		
XXX.XX			
XXX.XXX			
APPROVALS	DATE	TITLE PA PACKAGE OUTLINE	
DRAWN	01/19/93	6.10 mm BODY WIDTH TSSOP	
CHECKED		.50 mm PITCH	
		SIZE	DRAWING No.
		C	PSC-4039
			REV 03
DO NOT SCALE DRAWING			



TVSOP

The Most Compact Double Density Package

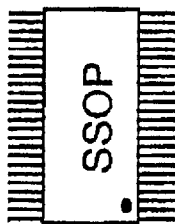


TVSOP Package	Typical Dimensions (in mm)				Area (mm ²)
	A	B	C	E	
48 Pin	9.80	4.40	6.40	0.40	63.00
56 Pin	11.30	4.40	6.40	0.40	72.30
80 Pin	17.00	6.10	8.10	0.40	137.80
100 Pin	20.80	6.10	8.10	0.40	168.50



Double Density Packaging

48-Pin



16.0 x 10.3 x 2.6 mm
pin pitch = 0.635 mm
Area = 164.8 mm²

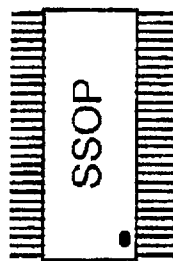


12.5 x 8.1 x 1.1 mm
pin-pitch = 0.5 mm
Area = 101.3 mm²

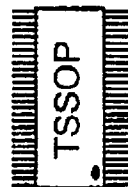


9.8 x 6.4 x 1.1 mm
pin-pitch = 0.4 mm
Area = 62.7 mm²

56-Pin



18.4 x 10.3 x 2.6 mm
pin-pitch = 0.635 mm
Area = 189.5 mm²



14.0 x 8.1 x 1.1 mm
pin-pitch = 0.5 mm
Area = 113.4 mm²



11.3 x 6.4 x 1.1 mm
pin-pitch = 0.4 mm
Area = 72.3 mm²

TVSOP	Area (mm ²)	%Smaller Than SSOP	%Smaller Than TSSOP
48 pin	63.00	61.9	38.0
56 pin	72.30	62.2	36.0